Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal
Autonomous
Department of Electronics and Communication Engineering

COURSE FILE

ACADEMIC YEAR : 2022-23

SUBJECT : Electronic Devices and Circuits

YEAR/SEM : II B.Tech I-Sem

DEPARTMENT : Electronics & Communication Engineering

FACULTY NAME : Mr. M. A. Vijay Kamalnath

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Dr. Kethepalli Mallikarjuna
HOD of ECE

Dr. KETHEPALLI MALLIKARJUNA
B.E, M.Tech, Ph.D, MISTE, FIETE, MIE
Professor & HOD
Department of ECE
RGM College of Engg. & Tech. (Autonomous)
NANDYAL - 518 501, Kurnool (Dist), A.P.

Dr.T. Jayachandra Prasad
Principal

Dr. T. JAYACHANDRA PRASAD
M.E,Ph.D.,
PRINCIPAL
RGM College of Engg. & Tech.,
(Autonomous)
NANDYAL-518 501, Nandyal (Dt), A.P.

R.G.M.COLLEGE OF ENGINEERING & TECHNOLOGY, NANDYAL – 518 501
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II B.Tech., I-Semester **Academic Year: 2022-23**

w.e.f: 07-10-2022

A-Section : RB2130 **B-Section : RB2010**
C-Section : RB2020 **D-Section : RB2030**

Period/ Day	Section	1 9.00 AM To 9.50 AM	2 9.50 AM To 10.40 AM	3 11.00 AM To 11.50 AM	4 11.50 AM To 12.40 PM	5 1.50 PM To 2.40 PM	6 2.40 PM To 3.30 PM	7 3.30 PM To 4.20 PM
MON	A	SS	VC&CV	MEFA	DTI	DLCD	EDC	EDC
	B	DLCD	EDC	SS	MEFA	VC&CV	DTI	SS
	C	DTI	EDC	SS	DLCD	EDCLab/BS Lab/EE Lab		
	D	DLCD	SS	EDC	VC&CV	EDCLab/BS Lab/EE Lab		
TUE	A	EDCLab/BS Lab/EE Lab			SS	EDC	VC&CV	DLCD
	B	EDCLab/BS Lab/EE Lab			DTI	SS	DLCD	EDC
	C	DLCD	MEFA	SS	VC&CV	EDC	VC&CV	DTI
	D	SS	SS	EDC	EDC	DLCD	MEFA	VC&CV
WED	A	SS	EDC	DLCD	DTI	VC&CV	SS	MEFA
	B	DLCD	DTI	MEFA	SS	VC&CV	VC&CV	EDC
	C	EDCLab/BS Lab/EE Lab			EDC	MEFA	SS	DLCD
	D	EDCLab/BS Lab/EE Lab			SS	DLCD	EDC	MEFA
THU	A	DLCD	MEFA	VC&CV	EDC	EDCLab/BS Lab/EE Lab		
	B	VC&CV	MEFA	EDC	DLCD	EDCLab/BS Lab/EE Lab		
	C	EDCLab/BS Lab/EE Lab			VC&CV	EDC	SS	DLCD
	D	EDCLab/BS Lab/EE Lab			DLCD	DLCD	MEFA	DTI
FRI	A	EDCLab/BS Lab/EE Lab			DTI	MEFA	DLCD	SS
	B	EDCLab/BS Lab/EE Lab			VC&CV	SS	MEFA	DLCD
	C	DLCD	MEFA	VC&CV	DTI	SS	EDC	MEFA
	D	EDC	DTI	DLCD	VC&CV	MEFA	VC&CV	SS
SAT	A	SS	EDC	VC&CV	MEFA	DLCD	EAA	
	B	EDC	SS	DLCD	EDC	MEFA		
	C	SS	VC&CV	EDC	MEFA	DLCD		
	D	DTI	MEFA	VC&CV	SS	EDC		

Subject	Section	Name of the Faculty
VC&CV	A	Dr.K.V.Surya Narayana Rao
EDC	A	Dr.M.Chennakesavalu
DLCD	A	Dr.K.Mallikarjuna
S&S	A	Mr.P.Chandra Sekhar
MEFA	A	Mr.K Rama Krishna
DTI	A	Mr.Shaik.Asif Basha
EDC Lab	A	Dr.MCK/Mr.KMVK/YPKR
EE Lab	A	Mr.C.Ashok Kumar
BS Lab	A	Mr.PCS/Mr.JLMK/KSR

Subject	Section	Name of the Faculty
VC&CV	B	Dr.P.Sreedevi
EDC	B	Mr.K.Vijaya Kamalnadh
DLCD	B	Mr.Y.Praveen Kumar Reddy
S&S	B	Mr.P.Chandra Sekhar
MEFA	B	Mr.Rajasekhar
DTI	B	Dr.J.Sofia Priyadarshini
EDC Lab	B	Dr.MCK/Mr.KMVK/YPKR
EE Lab	B	Mr.C.Ashok Kumar
BS Lab	B	Mr.PCS/Mr.JLMK/KSR

Subject	Section	Name of the Faculty
VC&CV	C	Dr.P.Chandra Sekhar Reddy
EDC	C	Mr.T.Tirumalesh
DLCD	C	Mr.P.Mahesh
S&S	C	Mrs.M.Hemalatha
MEFA	C	Dr.Aliya Sulthana
DTI	C	Smt.B.Indu
EDC Lab	C	Dr.AS/Dr.CV/Mr.TT
EE Lab	C	Dr.A.Suresh Kumar
BS Lab	C	Mr.D.UsenMr.SAB/BI

Subject	Section	Name of the Faculty
VC&CV	D	Dr.P.Chandra Sekhar Reddy
EDC	D	Dr.A.Sathish
DLCD	D	Miss.N.Fouzia Sulthana
S&S	D	Dr.R.Hanuma Naik
MEFA	D	Dr.Aliya Sulthana
DTI	D	Smt.B.Indu
EDC Lab	D	Dr.AS/Dr.CV/Mr.TT
EE Lab	D	Dr.A.Suresh Kumar
BS Lab	D	Mr.D.Usen/Mr.SAB/BI

Dr.Kethepalli Mallikarjuna
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R G M COLLEGE OF ENGINEERING AND TECHNOLOGY

AUTONOMOUS

ELECTRONICS AND COMMUNICATION ENGINEERING

II B.Tech, I-Sem (ECE)

L	T	C
2	1	3

(A0403203) ELECTRONIC DEVICES AND CIRCUITS

COURSE OBJECTIVES:

- To understand the basic materials used for fabrication of different semiconductor devices.
- To understand construction details, principle of operation and equivalent electrical model of each device.
- Evolution of different diodes based on doping levels.

COURSE OUTCOMES:

- Understand and analyse the principle of operation and equivalent electrical model for semiconductor devices like PN diode, Zener diode.
- Understand and analyse the principle of operation and equivalent electrical model for semiconductor devices like BJT, JFET, MOSFET.
- Apply the property of junction diode in rectifiers and regulators.
- Obtain the Q point for various biasing techniques.

MAPPING WITH COs & POs:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO11	PO11	PO11	PSO1	PSO2	PSO3
CO1	3	2											2	2	
CO2	1	3											2	3	
CO3	2		3										1	2	1
CO4		2	3										2	1	

UNIT I

Semiconductor Diode: Open circuited PN junction, Current components in a PN diode, Diode Equation and its mathematical derivation, Volt-Ampere Characteristics, Energy band diagram of PN diode, Temperature dependence of Volt-Ampere Characteristics, Diode resistance (Static and Dynamic resistance), Transition capacitance, Diffusion capacitance, Step graded and linear graded junction. Avalanche breakdown, V-I Characteristics of Zener diode, Zener breakdown.

UNIT II

Diode Applications: Diode as switch – Forward recovery and reverse recovey times of a diode, Rectifier – Half wave and Full wave rectifier, Bridge rectifier, Ripple factor, PIV. **Filters**: Inductor and Capacitor, L-Section and Π-Section Filters, Zener diode as voltage regulator, brief introduction to Clipping and Clamping circuits.

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ELECTRONICS AND COMMUNICATION ENGINEERING

UNIT III

Bipolar Junction Transistor (BJT): Transistor – Structure, Current components and their relationship, PNP and NPN transistors - Active mode of operation, Symbols and conventions, Transistor equations, Transistor as an amplifier, input and output characteristics of Common Base, Common Emitter and Common collector configurations. DC analysis of Common Base, Common Emitter and Common collector circuits.

UNIT IV

BJT Biasing: Load line and modes of operations, Operating point, Bias stability, Fixed bias, Self bias, Stabilization against variations in I_{co}, V_{BE}, β, Bias compensation, Thermal runaway, Condition for thermal stability, Problem solving. Applications: As a Switch and definitions of switching times, as an Amplifier.

UNIT V

Field-Effect Transistors (FET): Structure, principle of operation and V-I characteristics of n-channel and p-channel Junction Field Effect Transistors (JFET), Problem solving.

Metal Oxide Semiconductor Field-effect Transistor (MOSFET): Structures, MOSFET current equation and V-I characteristics. n-channel MOSFET: Enhancement mode and Depletion mode**.** p-channel MOSFET: Enhancement mode and Depletion mode. MOSFET symbols and conventions, Complementary MOSFETs (CMOSFETs) - Structure, V-I characteristics, symbols and conventions. MOSFET act as capacitor.

UNIT VI

Biasing Circuits Using MOSFETS: Different configurations using MOSFETs, load line and modes of operation, different biasing circuits (self-bias, voltage divider bias) using MOSFETs, DC Analysis of n-channel and p-channel MOSFETs (both Enhancement and Depletion modes), Problem solving. Applications: MOSFETs as switch and small signal amplifier.

TEXT BOOKS:

1) Millman's Electronic Devices And Circuits; by Jacob Millman, Christos C. Halkias, Satyabrata Jit, 4th edition, McGraw Hill Publication, June 26th 2015.
2) Electronic Devices and Circuits; by R.L. Boylestad and Louis Nashelsky, 9th Edition, Pearson, 2006.

REFERENCES:

1) Electronic Devices and Circuits; by David A Bell, Oxford Higher Education, Fifth Edition.
2) Electronic Circuits – analysis and design; Donald A Neamen, 3rd Edition, McGraw Hill (India), 2019.
3) Microelectronics; by Behzad Razavi, 2nd edition, Wiley, 2013.
4) Electronic Devices and Circuits; by Jimmie J Cathey, Schaum's outlines series, 3rd edition, McGraw-Hill (India), 2010

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LESSON PLAN

Name of the faculty: Mr. M.A.Vijay Kamalnath
Year & Semester: II -B.Tech-I Sem
Subject: Electronic Devices & Circuits (EDC)

Academic Year: 2022-23
Branch & Section: ECE-B
Total Hours: 78

Unit	Topic to be covered	No. of Periods	Total Periods Per Unit
I	**Semiconductor Diode**		15
	Introduction to EDC, PN junction materials	1	
	Open junction PN junction	1	
	Current components in a PN diode	1	
	Diode equation and it's mathematical derivation	2	
	Volt-ampere characteristics	1	
	Energy band diagram of PN diode	1	
	Temperature dependence of Volt-ampere characteristics	1	
	Diode resistance (Static & Dynamic).	2	
	Transition capacitance, Step and linear graded junction	1	
	Diffusion capacitance	1	
	Avalanche breakdown, V-I characteristics of Zener Diode, Zener breakdown	2	
	Problem solving	1	
II	**Diode Applications**		15
	Introduction, Diode as switch	1	
	Forward recovery and reverse recovery times of a diode	1	
	Rectifier-HW & FW, Bridge wave reciter, PIV.	4	
	Filters: Inductor & Capacitors,	2	
	L-Section & Pi-section Filters	2	
	Zener Diode as voltage regulator	2	
	Brief introduction to Clipping & Clamping circuits.	2	
	Problem solving	1	
III	**Bipolar Junction Transistor (BJT):**		11
	Introduction, Transistor structure	1	
	Current components & their relations	1	
	PNP & NPN transistors, Active mode of operations, Symbols & conversion,	2	
	Transistor equations	1	
	Transistor as an amplifier,	1	
	Input & output characteristics of Common Base (CB), Common Emitter (CE), and Common Collector (CC) configurations,	3	
	DC analysis of CB, CE and CC circuits	2	
IV	**BJT Biasing**		
	Load line and mode of operations	1	
	Operating point, Bias stability	1	
	Fixed Bias, Self bias	3	

	Stabilization against variation in Ico, $V_{BE,}$	1	12
	Bias compensation	1	
	Thermal runaway, condition for thermal stability	1	
	problem solving	2	
	Applications: As a switch and definition of switching time, as an amplifier	2	
V	**Field-Effect Transistor (FET):**		15
	Introduction, Structure, principle of operation	1	
	V-I characteristics of n-channel and p-channel Junction Field Effect transistors (JFET),	2	
	Problem solving.	2	
	Metal Oxide Semiconductor Field Effect Transistor (MOSFET)		
	Introduction, structure	1	
	MOSFET current equation and V-I characteristics	2	
	n-channel MOSFET: Enhancement mode and depletion mode	1	
	p-channel MOSFET: Enhancement mode and depletion mode	1	
	MOSFET Symbols and conversions	1	
	Complementary MOSFETs-Structure, V-I characteristics, symbols and conversions.	2	
	MOSFET as capacitors, Problem solving.	2	
VI	**Biasing Circuits using MOSFETS**		10
	Different configurations using MOSFETs	1	
	Load line and modes of operation	1	
	Different biasing circuits(Self-bias, voltage bias) using MOSFETs	2	
	DC analysis of n-channel MOSFETs (both enhancement & depletion modes)	2	
	Problem solving	2	
	Applications of MOSFETS as switch and small signal amplifiers	2	

Signature of the Faculty

Signature of the HOD

28/1/2023.

RGM COLLEGE OF ENGINEERING & TECHNOLOGY

(AUTONOMOUS)

NANDYAL - 518 501. Kurnool (Dist.) A.P.

EDUCATION FOR PEACE

(ESTD-1995)

ATTENDANCE REGISTER

II-I EDC (B/S)

ACADEMIC YEAR	: 2022-23	**SEM** :	I / II
COURSE	: B.TECH	**CLASS** :	II B.Tech II Sem
BRANCH / SECTION	: ECE-B		
SUBJECT & CREDITS	: ELECTRONIC DEVICES AND CIRCUITS 03		
FACULTY	: M.A. VIJAY KAMALNATH		

R.G.M. COLLEGE OF ENGINEERING

ATTENDANCE

Class : III B.Tech I Sem

Branch : ECE (B-Section)

Semister / Year

Roll No.	Name	Date	10/10/22	11/10/22	12/10/22	12/10/22	13/10/22	15/10/22	18/10/22	21/10/22	22/10/22	22/10/22	25/10/22	26/10/22
21091A0			1	2	3	4	5	6	7	8	9	10	11	12
465	Y. Jaya Sreenivas Reddy		A	1	A	A	2	3	4	5	6	A	7	8
466	P. Jaya Surya		A	1	A	A	2	3	4	5	6	A	A	7
467	P. Jithendra Reddy		A	1	2	3	4	5	6	7	8	A	9	10
468	N. Johnson Kumar		1	2	3	4	5	6	7	8	9	A	10	11
469	B. Kailashnath Reddy		A	1	2	3	4	5	6	A	7	8	9	10
470	K. Kalyani		A	1	A	A	2	3	4	5	6	7	8	9
471	Y. Kasthik Kumar Reddy		1	2	3	4	5	6	7	8	9	10	11	12
472	V. Kasthik		A	1	A	A	2	3	4	A	5	A	6	7
473	B. Kasi Eswari		1	2	3	4	5	6	7	8	9	10	11	A
474	D. Kasim Saheb		A	1	A	A	2	3	4	5	6	7	A	A
475	Nara Keerthi		A	1	2	3	4	5	6	7	8	9	10	11
476	P. Khadar Basha		A	1	2	3	4	5	6	A	7	A	A	8
477	K. Kiran Kumar Naik		1	2	3	4	5	6	7	8	9	A	A	A
478	B. Krupakar		1	2	3	4	5	6	7	8	9	10	A	11
479	M. Lakshmi Devi		1	2	3	4	5	6	7	8	9	10	11	12
480	S. Lakshmi Narasimhulu		A	1	A	A	A	A	A	2	3	4	5	6
481	B. Lavanya		A	1	2	3	4	5	6	7	8	9	10	A
482	K. Lavanya		A	1	A	A	2	3	4	A	5	6	7	8
483	K. Likhitha		1	2	3	4	5	6	7	8	9	10	11	12
484	B. Lomith Reddy		1	A	2	3	4	5	6	A	7	8	9	10
485	J. Mabu Hussain		1	2	3	4	5	6	7	A	8	9	10	11
486	B. Madhavi		1	2	3	4	5	6	7	8	A	A	9	10
487	M. Madhu		A	1	A	A	2	3	4	5	6	7	A	A
488	G. Madhusudan Reddy		1	2	3	4	5	6	7	8	9	10	11	12
489	E. Madhusudhan Goud		A	1	A	A	2	3	A	A	4	5	A	6
490	G. Madhusudhan		A	A	A	A	A	A	1	2	3	4	5	6
491	G. Guru Mahammad Basha		1	2	3	4	5	6	7	8	9	10	11	12
			AVL	AVL	AVL	AVL	AVL	AVL	AVL	AVL	AVL	AVL	AVL	AVL
Signature of Teacher														
Signature of H.O.D.														
Signature of Principal														

& TECHNOLOGY (Autonomous), NANDYAL.

REGISTER Academic Year from 2022 to 2023 Teacher MCIC

Subject & Credits EDC, 03 Dept ECE

INTERNAL / RECORD MARKS

Assignments				Internal Test		Internal Marks			Final Internal (I+A)	Remarks
Roll No.	1	2	Average (A)	1	2	75% of MAX	25%of MIN	Total (I)		
65	10	10	10	09	14				23	
66	10	9	9.5	01	05				14	
67	10	9	9.5	02	08				17	
68	10	10	10	01	02				12	
69	10	10	10	06	05				16	
70	10	9	9.5	11	13				23	
71	10	10	10	03	02				13	
72	10	10	10	05	05				15	
73	10	10	10	14	13				24	
74	10	10	10	02	02				12	
75	10	10	10	07	10				20	
76	10	10	10	10	11				21	
77	10	10	10	06	02				15	
78	10	10	10	05	05				15	
79	10	9	9.5	09	04				18	
80	10	10	10	03	02				13	
81	10	10	10	11	14				24	
82	10	10	10	14	18				27	
83	10	9	9.5	11	07				20	
84	10	10	10	05	03				15	
85	10	9	9.5	08	05				18	
86	10	10	10	13	14				24	
87	10	10	10	12	07				21	
88	10	9	9.5	13	08				22	
89	10	9	9.5	04	04				14	
90	10	9	9.5	07	07				17	
91	10	9	9.5	08	11				21	
	Abs	Abs	Abs	Abs	Abs				Abs	

7/7/23

R.G.M. COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous

ATTENDANCE REGISTER

Academic Year from...

Class : II B.Tech I Sem)

Branch : ECE (B. Section)

Roll No. 2109140	Name	Date 10/10/22	11/10/22
		1	2
493	U. Mahesh	1	2
494	Y. Mahesh	1	2
495	S. Mahitha	A	1
496	R. B. Mallikarjun	A	1
497	G. Manasa	A	1
498	M. Manasa	A	1
499	M. Manikumar Naik	1	2
4A0	V. Manikanta	A	1
4A1	P. Manisha	A	1
4A2	G. Manjula	A	1
4A3	B. Manoj Kumar Reddy	A	1
4A4	M. Manoj Kumar	A	1
4A5	K. Manoj	A	1
4A6	V. Maria Dhathri	1	2
4A7	V. Maruthi	A	
4A8	M. Meenakshi	A	1
4A9	A. Meghana	1	2
4B0	C. T. Mithunteja	A	1
4B1	S. Mohammad Abbas	A	1
4B2	S. Mahammad Irfan	1	
4B3	S. Mohammad Arif	1	2
4B4	Poluru Mounika	A	1
4B5	M. Mythili	A	1
4B6	B. Naga Sowjanya	1	2
4B7	B. Nagaudayeswara Reddy	A	1
4B8	A. Nagu Chavan	A	1
4B9	B. Nagaraju	1	2
4C0	R. G. Nagesh	A	1
4C1	B. Naveen	A	1
4C2	R. Naveen	A	1
Signature of Teacher		Avk	Avk
Signature of H.O.D.			
Signature of Principal			

Roll No.	10/11/22	11/11/22	12/11/22	14/11/22	16/11/22	17/11/22	19/11/22	19/11/22	21/11/22	24/11/22	23/11/22
	24	25	26	27	28	29	30	31	32	33	34
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	Avk	Avk	Avk	Avk	Avk	Avk	Avk	Avk	Avk	Avk	Avk

Roll No.	24/11/22	24/11/22	24/11/22	24/11/22	26/11/22	26/11/22	28/11/22	29/11/22	30/11/22	01/12/22	01/12/22
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	34	35	36	37	38	39	40	41	42	43	44
	28	29	30	31	32	33	34	35	36	37	38
	32	33	34	35	36	37	38	39	40	41	42
	25	26	27	28	29	30	A	31	32	33	34
	33	34	35	36	37	38	39	40	41	42	43
	28	29	30	31	32	33	A	34	35	36	37
	29	30	31	32	33	34	35	36	37	38	39
	A	31	32	A	A	A	A	33	34	35	36
	27	28	29	A	A	30	31	32	33	34	35
	32	33	34	35	36	37	38	39	40	41	42
	35	36	37	38	39	40	41	42	43	44	45
	29	30	31	32	33	34	35	36	37	38	39
	24	25	26	A	27	28	29	30	31	32	33
	28	29	30	A	30	31	32	33	34	35	36
	34	35	36	37	38	39	40	41	42	43	44
	31	32	33	A	A	34	35	36	37	38	39
	33	34	35	36	37	38	39	40	41	42	43
	30	31	32	33	34	35	36	37	38	39	40
	28	29	30	31	32	33	34	35	36	37	38
	26	27	28	29	30	A	A	A	31	32	33
	34	35	36	37	38	39	40	41	42	43	44
	33	34	35	36	37	38	39	40	41	A	A
	A	31	32	A	A	33	34	35	36	37	38
	28	29	30	31	32	33	34	35	36	37	38
	Avk	Avk	Avk	Avk	Avk	Avk	Avk	Avk	Avk	Avk	Avk

& TECHNOLOGY (Autonomous), NANDYAL.

REGISTER Academic Year from 2022 to 2023 Teacher MCK

Subject & Credits EDC, 03 Dept ECE

INTERNAL / RECORD MARKS

Roll No.	Assignments 1	2	Average (A)	Internal Test 1	2	Internal Marks 75% of MAX	25%of MIN	Total (I)	Final Internal (I+A)	Remarks
93	10	10	10	15	13				28	
94	10	10	10	12	06				21	
95	10	10	10	08	06				18	
96	10	9	9.5	16	13				26	
97	10	10	10	11	13				23	
98	10	9	9.5	08	04				17	
99	10	9	9.5	15	12				25	
A0	10	9	9.5	02	11				19	
A1	10	10	10	08	08				18	
A2	10	10	10	09	08				19	
A3	10	9	9.5	16	10				25	
A4	10	9	9.5	13	17				26	
A5	10	9	9.5	08	09				19	
A6	10	9	9.5	13	10				23	
A7	10	10	10	11	06				20	
A8	10	9	9.5	12	14				24	
A9	10	9	9.5	12	10				22	
B0	10	10	10	05	05				15	
B1	10	9	9.5	09	06				19	
B2	10	10	10	05	06				16	
B3	10	9	9.5	16	15				26	
B4	10	9	9.5	09	06				19	
B5	10	9	9.5	10	08				20	
B6	10	9	9.5	05	05				15	
B7	10	9	9.5	05	04				15	
B8	10	—	5	05	AB				AB	
B9	10	9.5	9.75	10	09				20	
C0	10	9	9.5	15	15				25	
C1	10	9	9.5	09	10				20	
C2	10	10	9.5	01	02				12	
	Abs	Abs	Abs	Abs	Abs				Abs	

R.G.M. COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous), NANDYAL.

ATTENDANCE REGISTER

Class : II B.Tech I Sem Academic Year from 2022 to 2023 Teacher MAVK

Branch : E.C.E (B. Section) EDC, 03 Dept. ECE

Roll No.	Name	Date 10/10/22	1
4C3	D. Nisheth	A	
4C4	P. Nishitha	1	
4C5	K. pavan Kumar Reddy	A	
4C6	S. pavan Kumar Reddy	A	
4C7	C. pavan Kumar	A	
220T4C7	K. Deveswar Reddy		
408	G. Dharma Teja		
409	K. Elizabeth Rani		
411	G. Gangothri		
413	K. Harika		
415	I. Hemanth Kumar		
417	J. Jayavardan		
422	P. Muni Teja		
428	P. Rameeja		
429	S. Ruksana		
435	K. Sreenivas		
436	N. Varun Kumar		
	Signature of Teacher	A/L	A
	Signature of H.O.D.		
	Signature of Principal		

Roll No.	03/01/23	03/01/23	04/01/23	05/01/23	06/01/23	07/01/23	09/01/23	10/01/23	11/01/23	17/01/23	18/01/23
	68	69	70	71	72	73	74	75	76	77	78
C3	63	64	65	A	66	A	67	68	69	A	70
C4	61	62	63	64	65	66	67	68	69	A	A
C5	61	62	63	64	65	66	67	68	69	A	70
C6	62	63	64	65	66	67	68	69	70	A	A
C7	57	58	A	59	60	61	62	63	A	A	64
408	47	48	49	50	51	52	53	54	55	A	56
409	42	43	44	45	46	47	48	A	49	A	50
411	45	46	47	48	49	50	51	52	53	A	A
413	47	48	49	50	51	52	53	54	55	A	56
415	46	47	48	49	50	51	52	53	54	A	A
417	48	49	A	50	51	52	53	54	A	A	A
422	48	49	50	51	52	53	54	55	A	A	A
428	48	49	50	51	52	53	54	A	A	A	55
429	A	A	43	44	45	46	A	A	A	A	47
435	48	49	50	51	52	53	54	55	56	A	57
436	42	43	44	45	A	A	46	47	48	A	A
	47	48	49	50	51	52	53	54	A	A	55
	A/L	A/L	A/L	A/L	A/L	A/L	A/L	A/L	A/L	A/L	A/L

Roll No.	19/01/23	23/01/23	24/01/23	25/01/23	29/01/23	30/01/23	31/01/23	01/02/23	02/02/23	06/02/23	07/02/23
	79	80	81	82	83	84	85	86	87	88	89
C3	71	72	73	A	74	75	76	77	78	79	80
C4	70	71	72	73	74	75	76	77	78	79	80
C5	A	71	72	73	74	75	76	77	78	79	80
C6	71	72	A	73	74	75	76	77	78	79	80
C7	A	65	66	67	68	69	70	71	72	73	74
408	57	58	59	60	61	62	63	64	65	66	67
409	51	52	53	54	55	56	57	58	59	60	61
411	A	54	55	56	57	58	59	60	61	62	63
413	57	58	59	60	61	62	63	64	65	66	67
415	55	56	57	58	59	60	61	62	63	64	65
417	55	56	57	58	59	60	61	62	63	64	A
422	56	57	58	59	60	61	62	63	64	65	66
428	A	56	57	58	59	60	61	62	63	64	65
429	A	48	49	50	51	52	53	54	55	56	57
435	58	59	60	61	62	63	64	65	66	67	68
436	49	A	50	A	A	51	A	52	53	54	55
	56	57	58	59	60	61	62	A	63	64	A
	A/L	A/L	A/L	A/L	A/L	A/L	A/L	A/L	A/L	A/L	A/L

RECORD MARKS

Internal Marks 5%of MIN	Internal Marks Total (I)	Final Internal (I+A)	Remarks
		23	
		26	
		24	
		28	
		16	
		28	
		20	
		19	
		26	
		23	
		25	
		27	
		28	
		21	
		26	
		24	
		19	
		A/L	

R.G.M. COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous), NANDYAL.

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409	K. Elizabeth Rani				
411	G. Gangothri				
413	K. Harika				
415	J. Hemanth Kumar				
417	J. Jayavardan				
422	P. Muni Teja				
428	P. Rameeja				
429	S. Ruksana				
435	K. Sreenivas				
436	N. Varun Kumar				

INTERNAL / RECORD MARKS

Roll No.	Assignments 1	2	Average (A)	Internal Test 1	2	Internal Marks 75% of MAX	25%of MIN	Total (I)	Final Internal (I+A)	Remarks
C3	10	9		13	13				23	
C4	10	9		13	16				26	
C5	10	9		12	14				24	
C6	10	10		15	19				28	
C7	10	10		07	9				16	
22407	10	10		15	19				28	
8	10	9		07	10				20	
9	10	9		08	9				19	
11	10	10		11	17				26	
13	10	10		12	13				23	
15	10	10		14	15				25	
17	10	9		12	18				27	
22	10	10		17	18				28	
28	10	10		11	08				21	
29	10	10		12	17				26	
35	10	10		12	14				24	
36	10	10		08	09				19	

LECTURE RECORD

Subject : ELECTRONIC DEVICES & CIRCUITS
Total Exams..... 02
Credits : 03
Each for..... 02 ..... hrs.
Internal Mid Exam Marks : 30
Total quizes
Internal Quiz Marks : 20
No. of Assignment..... 04

S.No.	Date	Topic Covered / Exercise Completed	Remarks	
1.	10/10/2022	Introduction to Electronic Devices & Circuits	01	01
		UNIT-I : SEMICONDUCTOR DIODE		
2.	11/10/2022	Semiconductor materials: E_g, Si, Ge & GaAs	01	02
	12/10/22	Covalent bonding & Intrinsic materials	02	04
3.	13/10/22	Open-Circuited PN junction	01	05
	15/10/22	—No bias, Forward bias & Reverse bias	01	06
4.	18/10/22	current components in a PN diode	01	07
5.	21/10/22	Diode equation and its mathematical derivation	01	08
6.	22/10/22	Volt Ampere characteristics,	01	09
7.	25/10/22	Diode Resistance (Static & Dynamic)	02	11
8.	26/10/22	Transition Capacitance	01	12
	27/10/22			
	29/10/22	Energy band diagram of PN Diode.	01	13
9.	31/10/22	Problem Solving on Resistance levels.	01	14
10.	02/11/22	Transition Capacitance step-graded Junction, Linear-graded Junction	01	15
11.	03/11/22	Diffusion capacitance.	01	16
12	05/11/22	Avalanche breakdown, V-I characteristics of Zener diode, Zener breakdown		
		UNIT-II : DIODE APPLICATIONS		
13.	07/11/22	Diode as Switch	01	17
14	07/11/22	Forward recovery & Reverse Recovery times of a diode.		
15	09/11/22	Half-Wave Rectifier	01	18
16	10/11/22	— Regulation, Ripple factor	01	19
17	12/11/22	—Average value, RMS value	02	21
18	14/11/22 to 23/11/22	→ Training classes (CC DS)	—	—
	24/11/22	Full wave Rectifier	01	22
19	26/11/22 to 27/11/22	—Ripple factor, Regulation, PIV	02	24
20	28/11/22	Filters Introduction	01	25
21	28/11/22	Inductor filter	01	26
22	29/11/22	Capacitor filter	02	28
23	29/11/22 to 30/11/22	L-section & π section Filter	02	30
24	30/11/22	CLC Filter	01	31
25	30/11/22 to 01/12/22	Zener diode as Voltage Regulator — Numerical Problems	02	32
			01	34

LECTURE RECORD

S.No.	Date	Topic Covered / Exercise Completed	Remarks	
26	07/12/22	Introduction to clippers — Series Clipper	01	35
27	03/12/22	— Parallel Clippers; Clampers	02	37
		UNIT-III : BIPOLAR JUNCTION TRANSISTOR		
28	08/12/22	Introduction (BJT, Types)	01	38
29	05/12/22	Transistor Construction - NPN & PNP	01	39
30	05/12/22	Current components & their relationships	01	40
31	15/12/22	Base width modulation or early effect	01	41
32	17/12/22	Active mode of operations, Symbols & Convention, Transistor equations	01	42
33	17/12/22	Input and output characteristics of CB configuration	01	43
34	19/12/22	Transistor as an Amplifier	01	44
35	20/12/22	Input and output characteristics of CE & CC Configuration	01	45
36	21/12/22	DC Analysis of CB, CE, and CC configuration	01	46
		UNIT-IV : BJT BIASING		
37	22/12/22	Introduction, Load line & modes operations.	01	47
38	23/12/22	operating point & stability	01	48
39	24/12/22	Bias stability, Fixed bias method	02	50
	26/12/22 to 29/12/22	Training classes (French, Spanish & German)	—	—
40	31/12/22	Fixed-bias with R_E, collector to base bias, and Self-bias method	02	52
41	31/12/22			
42	02/12/22	self-bias method & S' factor	01	53
43	02/12/22	Problem Solving	01	54
44	03/12/22	Stabilization Against I_{CO}, V_{BE}, β	01	55
45	03/12/22	Bias Compensation	01	56
46	04/12/22	— Diode, Thermistor, and Sensistor Compensation	01	57
47	05/12/22	Thermal runaway, condition for thermal stability	01	58
48	07/12/22	Applications: As a Switch definition of Switching times As an amplifier, Problem Solving	01	59

LECTURE RECORD

S.No.	Date	Topic Covered / Exercise Completed	Remarks	
		UNIT-V : UNIPOLAR TRANSISTOR		
49.	07/01/23	Introduction to Unipolar transistor	01	60
50	07/01/23	classification of FET & MOSFET	01	61
51.	09/01/23	FET: -Structure, Principle of operation V-I characteristics of n-channel	01	62
52.	10/01/23	-Structure, Principle of operation, V-I characteristics of P. channel.	01	63
53	11/01/23	Problem solving	01	64
		MOSFET:		
54.	17/01/23	Depletion mode (n-channel & p-channel) - Structure, operation, current equation	01	65
55.	18/01/23	- V-I characteristics, Problem	01	66
56.	19/01/23	Enhancement mode (n-channel & p-channel)	02	68
57.	23/01/23	- Structure, Operation, current equation		
58.	24/01/23	-VI characteristics	01	69
	25/01/23	Training program - - -		
59.	28/01/23	Complementary MOSFETs → - Structure, characteristics, Symbols & Conventions	01	70
			01	71
60.	30/01/23	MOSFET acts as capacitor	01	72
61	31/01/23	Problems solving	01	73
		UNIT-VI : BIASING CIRCUITS USING MOSFETS		
62.	01/02/23	Biasing definition and types	01	74
		Fixed bias method		
		Self bias method		
62	02/02/23	Voltage divider biasing for different configurations (MOSFET)	01	75
63	06/02/23	DC Analysis of n-channel and P-channel MOSFT (Depletion & enhancement mode) & load line concepts	01	76
64	07/02/23	Applications:	01	77
65	07/02/23	1. As a switch		
66	09/02/23	2. Small signal amplifiers Problem Solving	01	78

S.No. 45567

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

Accredited by NAAC of UGC, New Delhi with 'A' Grade:: Accredited by NBA

Affiliated to JNT University Anantapur

Nandyal - 518 501, Kurnool Dist, A.P.

(ESTD-1995)

INTERNAL EXAMINATIONS ANSWER BOOKLET

Principal
Autonomous

NAME OF THE STUDENT: P. Muni Teja Reg. No. 2 2 0 9 5 A 0 4 2 2

	1	2	3	4	5
A	1	3	2	2	
B	1	½	1½	3	
C	1				
D	1				
E	1				
Total	5	3½	3½	5	

Grand Total :(In Figures) 17

(in Words): One Seven

NAME OF THE SUBJECT: electronic devices & Components

INTERNAL EXAM : I / II

Date of Exam: 08/12/22 (FN/AN)

Course : B.Tech. / M.Tech./ MBA / MCA

Year : II nd Sem.: 3 rd

Branch: Electronics Communication engineering.

08/12/22.
Signature of the Invigilator

(Start Writing From Here)

1. a) Diffusion current :-

There are two Currents in Semi Conductors.

i) Drift Current

ii) Diffusion Current.

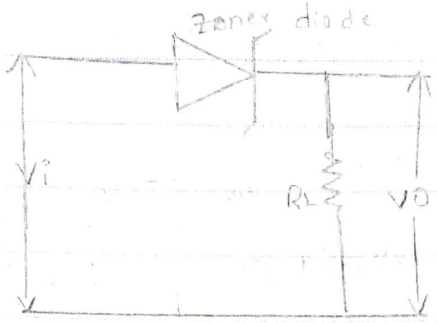
Diffusion current in $J_p = -qD_p \frac{dp}{dx}$ → (1)

Diffusion current in $J_n = -qD_n \frac{dn}{dx}$ → (2)

∴ Total diffusion Current $= +qD_p \frac{dp}{dx} + qD_n \frac{dn}{dx}$

$= -qD_p \frac{dp}{dx} - qD_n \frac{dn}{dx}$

b) Zener break down mechanism:-



The Zener breakdown mechanism is the mechanism,

This Zener breakdown mechanism occurs below 6 volts.

This Zener breakdown mechanism causes due to the collision of electrons.

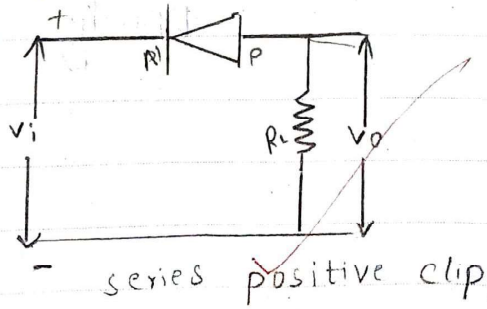
The Zener breakdown first the electrons are formed to Covalent bonds in form of structure of molecules.

c) Clipper Circuit:-

The different form of diode network is called Clipper, With this Clipper circuit we Clip "off" the input wave form (square, Sine, Sawsooth, triangle) without disturbing the Next half cycle (either positive or Negative). Two types of clippers:

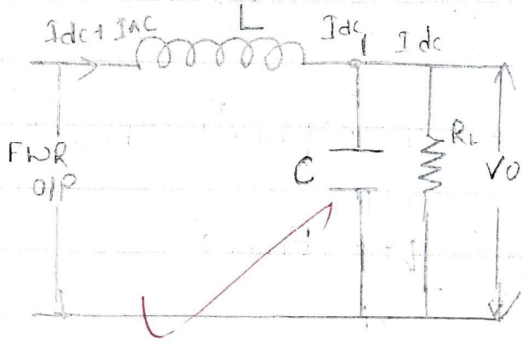
positive Clippers, (series, shunt)

Negative Clippers (series, shunt).

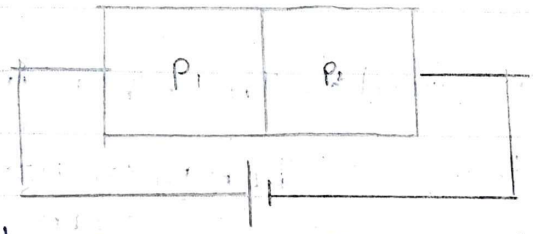


series positive clipper

d) Draw the circuit of L-C filter.

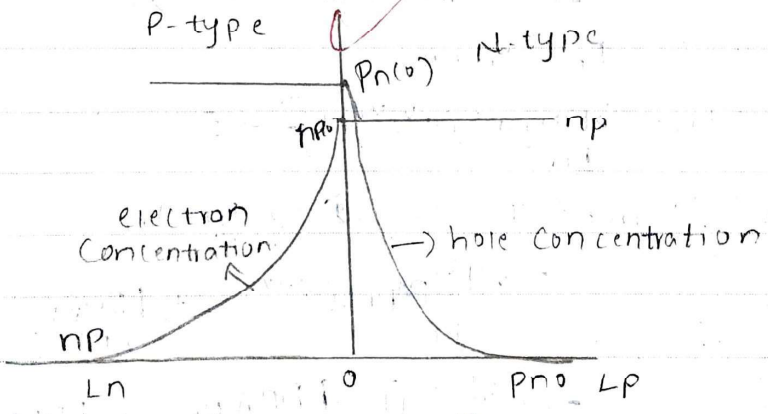


2. a) Current equation of PN junction diodes:



Consider P_2 is lower Concencentration then P_1.
Then, the P_2 in terms of P_1 is

$$P_2 = P_1 e^{-V/V_T}$$



$$P_n(0) = P_{no}\, e^{V/V_T}$$

$$n_p(0) = n_{po}\, e^{V/V_T}$$

Similarly,

$$p_{no} = P_n(0)\, e^{-V/V_T}$$

$$n_{po} = n_p(0)\, e^{-V/V_T}$$

Diffission current of $I_p = -qA_p D_p \frac{dp}{dx}$

$$= -qD_p \frac{dp}{dx}$$

$$= -qD_p \frac{p_n(0) - p_{no}}{0 - L_p}$$ (te

dx = length of semi conductor

$$= +qD_p p_{no} e^{V/\eta V_T} - p_{no}$$

$$+L_p$$

$$I_p = \frac{qD_p}{L_p} p_{no}(e^{V/\eta V_T} - 1)$$

$$I_p = J_p \times A$$

$$I_p = \frac{qD_p}{L_p} p_{no}(e^{V/\eta V_T} - 1) \times A \rightarrow (1)$$

Similarly,

Diffusion current of $J_n = -qD_n \frac{dn}{dx}$

$$= +qD_n \frac{n_p(0) - n_{po}}{0 + L_n}$$

$$= \frac{qD_n n_{po} e^{V/\eta V_T} - n_{po}}{L_n}$$

$$J_n = qD_n n_{po}(e^{V/\eta V_T} - 1)$$

$$I_n = J_n \times A$$

$$I_n = \frac{qD_n}{L_n} n_{po}(e^{V/\eta V_T} - 1) \times A \rightarrow (2)$$

Total current $I = (1) + (2) \Rightarrow I_p + I_n$

$$= \frac{qD_p A}{L_p} p_{no}(e^{V/\eta V_T} - 1) + \frac{qD_n}{L_n} n_{po} A (e^{V/\eta V_T} - 1)$$

$$= (e^{V/\eta V_T} - 1)\left(\underbrace{\frac{qD_p A}{L_p} p_{no} + \frac{qD_n}{L_n} n_{po} A}_{I_o}\right) = I_o$$

Total current $I = I_o(e^{V/\eta V_T} - 1)$

$\therefore$ Total Current $I = I_o(e^{V/\eta V_T} - 1)$

η is constant, for Ge-1 & Si-2

V_T is thermal voltage (26 v)

3

b) The Vo Diode Current:-

Given that,

$I_o = 5\ mA$

$V_T = 26\ mV$; $n = 1$ for Ge.

Voltage across diode increases to 0.75 Volts

Voltage of the diode = $0.7 + 0.75 = 1.45\ V$

Diode current equation $I = I_o\left(e^{V/nV_T} - 1\right)$ $n = 1$ for Ge,

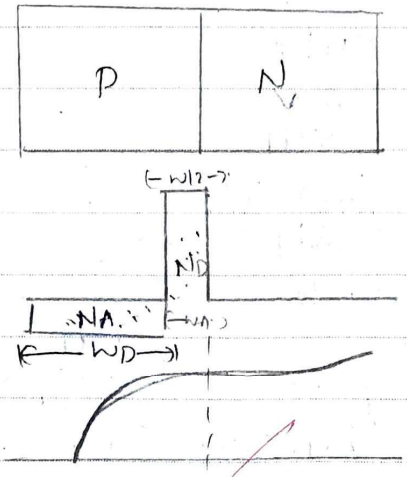
$I = 5\times10^{-3}\left(e^{1.45/1\times26} - 1\right)$

$I = 0.28\ mA$ (or) $2.86\times10^{-4}\ A$

Diode current $I = 0.28\ mA$.

$\frac{I_2}{I_1} = ?$

3.a) Expression for Space charge or transition Capacitance:-



Consider the poisonious equation,

$$\frac{d^2V}{dx^2} = \frac{\rho_v}{\epsilon}$$

$\because pV = Nq$

$N = ND$

$\because pV = NDq$

$$\frac{d^2V}{dx^2} = \frac{NDq}{\epsilon}$$

Dif Integrating with respect 'x'

$$\frac{dV}{dx} = \int \frac{NDq}{\epsilon}$$

$$\frac{dV}{dx} = \frac{NDq}{\epsilon} x$$

Again integration with respect to 'x'

$$V = \int \frac{NDq}{\epsilon} x$$

$$V = \left[\frac{NDqx^2}{\epsilon\ 2}\right]$$

$$2\epsilon V = NDqx^2$$

$\because x = W$

$2\epsilon V = NDq \cdot x^2$ $[\because x = W]$

$2\epsilon V = NDqW^2$

$$W^2 = \frac{2\epsilon V}{NDq}$$

$$W = \left(\frac{2\epsilon V}{Ndq}\right)^{1/2}$$

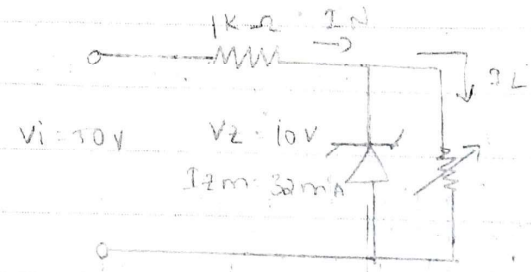
$$\boxed{W \propto V^{1/2}} \quad \because \frac{2\epsilon}{Ndq} \text{ is constant.}$$

2

By following the above equation we can get the diffusion capation

$$C_s = \frac{N\epsilon}{W}$$

b)



a)

$R_{Lmin} = \frac{R \cdot R_i}{V_z V_i}\ V - V_i$

$R_{Lmin} = \frac{V_i \cdot R}{V_z V_i} = \frac{V_i - V_z}{R \cdot V_z} = \frac{50-10}{1 \times 10} = \frac{40}{10} = 4\ \Omega$

$V_R = V_i - V_z = 50 - 10 = 40\ V$

$I_R = \frac{V_R}{R} = \frac{40}{1K} = 0.04 = 40mA$

$I_L = I_R - I_{zm} = 40 - 32 = 8\ mA$

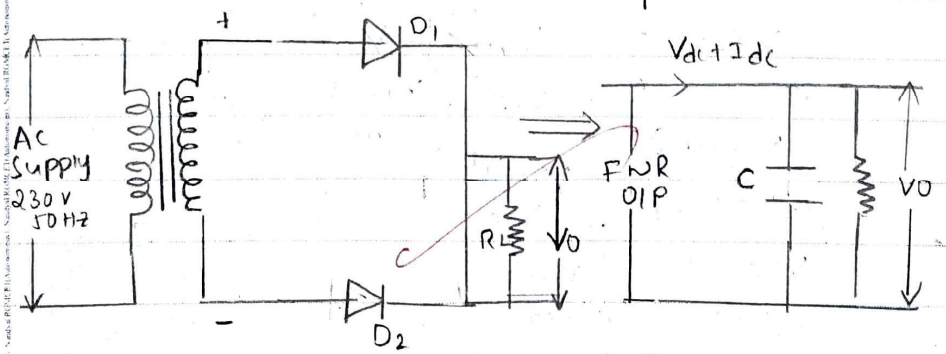
$I_L = R_L$ $\qquad R_{Lmax} = ?$

Power maximum wattage ratting of diode is power $P = V_z (I_{zm})$

$= 10 \times 32\ mA$

$= 320$ Watts. or 0.32 watts.

4. a) Full wave Rectifier with Capacitor filters:-



The output of the full wave Rectifier is given to the Capacitor filter:-

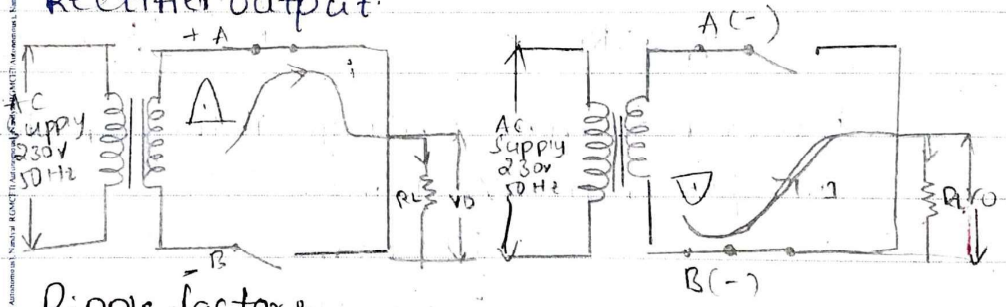
Operation:-

1. During the positive half cycle of Ac input voltage (end A positive & end B is Negative) Diode D_1 is forward bias and diode D_2 is Reverse bias. The D_1 is ON & D_2 is off.

The current flow through diode D_2 to the load Resistor (R_L)

2. During the Negative half cycle of Ac input (end B is positive, end B is Negative.) voltage the Diode D_2 is forward bias and diode D_1 is Reverse bias, The D_1 is off & D_2 is on. The current flow through the diode D_2 to load.

3. Here the Rectifier output is consists of both AC and DC Components, we removing the Ac components in this Rectifier Ouput we can use the filters. Here we use the Capacitor filter by Rc for Removing the Ac components in the Rectifier output.



Ripple factor:

$$V_{rms}^2 = V_{acrms}^2 + V_{dc}^2$$

$$V_{acrms}^2 = V_{rms}^2 - V_{dc}^2$$

$$= V_{dc}^2 \left(\frac{V_{rms}^2}{V_{dc}^2} - 1\right)$$

$$\left(\frac{V_{acrms}}{V_{dc}}\right)^2 = \frac{V_{rms}^2}{V_{dc}^2} - 1$$

2

$$\frac{V_{acrms}}{V_{dc}} = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$V_{dc} = \frac{2V_m}{\pi}$$

$$= \sqrt{\frac{\left(\frac{V_m}{\sqrt{2}}\right)^2}{\left(\frac{2V_m}{\pi}\right)^2} - 1} = \sqrt{\frac{\frac{V_m^2}{2}}{\frac{4V_m^2}{\pi^2}} - 1} = \sqrt{\frac{1}{2} \times \frac{\pi^2}{4} - 1}$$

$$\frac{V_{acrms}}{V_{dc}} = \sqrt{\frac{\pi^2}{8} - 1} = 0.48$$

Ripple factor of FWR is 0.48.

b) Voltage of $5 \sin \omega t$ of HWR

Given that $V = 5 \sin \omega t$

$V = V_m \sin \omega t$

$V_m = 5$

i) ∴ Maximum DC voltage $V_m = 5V$

ii) RMS value of HWR is $= \frac{V_m}{2}$

$V_{rms} = \frac{5}{2} = 2.5$

iii) Ripple factor of HWR $= \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$

$= \sqrt{\frac{(2.5)^2}{(1.59)^2} - 1}$

$V_{dc} = \frac{V_m}{\pi} = \frac{5}{\pi}$

$= 1.59$

$= 1.2$

Ripple factor = 1.21

iv) PIV of HWR is $V_m = 5V$

v) efficiency $= \frac{\text{DC power}}{\text{RMS power}} \times 100 = \frac{\text{RMS power}}{\text{DC power}} \times 100$

$P_{dc} = \frac{V_{dc}^2}{R_L}$

$P_{rms} = \frac{V_{rms}^2}{R_L}$

$= \frac{V_{dc}^2}{V_{rms}^2} \times 100 = \frac{V_{rms}^2}{V_{dc}^2} \times 100$

efficiency $= \frac{(1.59)^2}{(2.5)^2} \times 100$

efficiency = 40.44 %

-3-

1. e) In practice, NPN transistor more preffered than PNP?

In most of the practical issues tests NPN is more preferred than PNP because of.

In NPN transistor there is a exact values of I_E, I_C & I_B.

In NPN transistor always I_E equals to,

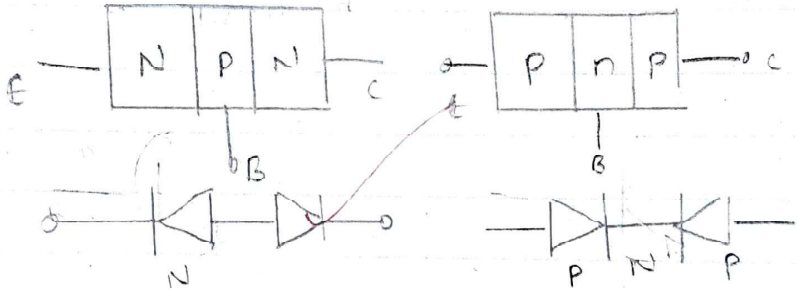
$I_E = I_B + I_C$.

But In PNP Some cases are not found this equation $I_E = I_B + I_C$.

The ~~con~~ material avalible in npn transistor is low cost Compared to pNP.

Most of the Circuits are drawn with the help of NpN transistors only.

The efficiency is more in NpN transistors.



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(ESTD-1995)

INTERNAL EXAMINATIONS ANSWER BOOKLET

Principal
RGEMCET Autonomous
NANDYAL.

NAME OF THE STUDENT: K. Lavanya Reg. No. 2 1 0 9 1 A 0 4 8 2

	1	2	3	4	5
A	1	2	3	3	
B	1	1½	2	2	
C	1				
D	1				
E	½				
Total	4½	3½	5	5	
Grand Total :(In Figures)	18				
(in Words):	One Eight				

NAME OF THE SUBJECT: EDC

INTERNAL EXAM : I / II

Date of Exam: 14-02-2023 (FN/AN)

Course : B.Tech. / M.Tech./ MBA / MCA

Year : II-Year Sem.: I-Sem

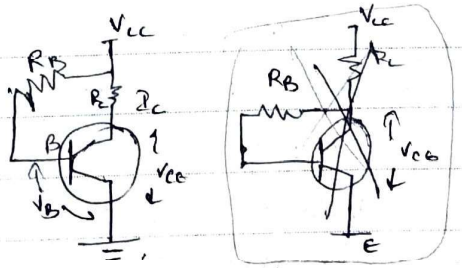
Branch: ECE-B

14/02/2023
Signature of the Invigilator

(Start Writing From Here)

Answers

1.a) Operating point :- The point which interconnects DC load line with output characteristics of transistor is called operating point. It lies in the middle of DC load line where faithful amplification is done.



~~$V_{CC} = I_B R_B$~~

Apply KVL at o/p side:

$V_{CC} - I_C R_C - V_{CE} = 0$

By $V_{CE} = 0$

$\Rightarrow I_C = \frac{V_{CC}}{R_C}$

By $I_C = 0$

$V_{CE} = V_{CC}$

Q point is deter as $\left(\frac{V_{CEQ}}{2}, \frac{I_C}{2}\right) = (V_{CEQ}, I_{CQ})$

1.b) Stability factor :- It is defined as rate of change of collector current with respect to I_{CO}, V_{BE}, β is called Stability factor

$$\Delta I_c = \frac{\partial I_c}{\partial I_{co}} \Delta I_{co} + \frac{\partial I_c}{\partial V_{BE}} \Delta V_{BE} + \frac{\partial I_c}{\partial \beta} \Delta \beta$$

$$\Delta I_c = S \Delta I_{co} + S' \Delta V_{BE} + S'' \Delta \beta$$

where $S = \frac{\partial I_c}{\partial I_{co}}$ ⇒ reverse current gain factor

$S'' = \frac{\partial I_c}{\partial \beta}$ ⇒ current gain, C_g

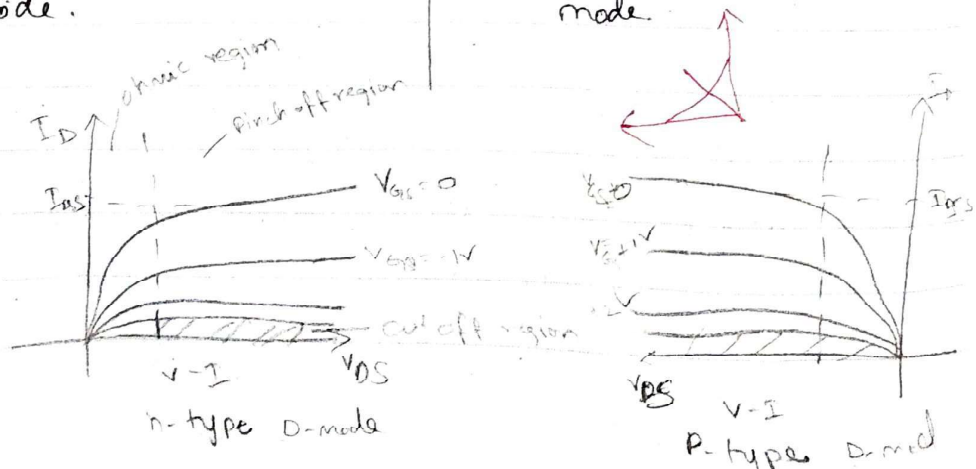
1.c) FET is defined as a semiconductor device which depends on electric field for the flow of control of current.

Because current flow in field effect transistor depends only on majority charge carriers i.e (electron in n-type & holes in P-type).

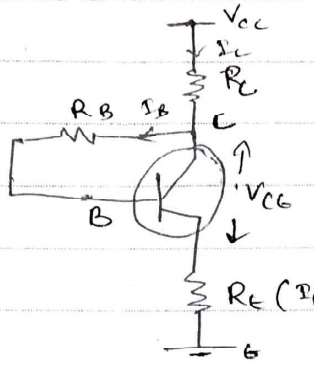
1.d)

D-MOSFET	E-MOSFET
1) In Depletion mode, channel is existed permanently	1) In Enhancement mode, there is no preexisted channel.
2) Preexisted channel	2) Channel is created at Threshold voltage.
3) There is no Threshold voltage	3) Threshold voltage is existed.
4) Depletion mode can be converted into Enhancement mode.	4) Enhancement mode can't be converted into Depletion mode.

1.e)



2. a. diagram



Apply KVL at i/p side

$$V_{CC} - I_C R_C - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0 \rightarrow (1)$$

$$V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_B R_E - I_C R_E = 0$$

diff with I_C

$$-R_C - \frac{\partial I_B}{\partial I_C} R_B - \frac{\partial I_B}{\partial I_C} R_E - R_E = 0$$

Apply KVL at o/p side

$$V_{CC} - (I_B + I_C) R_C - V_{CE} - R_E (I_B + I_C) = 0$$

$$V_{CC} - I_B R_C - I_C R_C - V_{CE} - I_B R_E - I_C R_E = 0$$

diff w.r.to I_C

$$-\frac{\partial I_B}{\partial I_C} R_C - \frac{\partial I_C}{\partial I_C} R_C - \frac{\partial I_B}{\partial I_C} R_E - R_E = 0$$

$$-\frac{\partial I_B}{\partial I_C} (R_C + R_E) -$$

$$V_{CC} - R_E (I_C + I_B) - R_B I_B - V_{BE} - R_E (I_B + I_C) = 0$$

$$V_{CC} - I_C R_C - I_B R_E - I_B R_B - V_{BE} - I_B R_E - I_C R_E = 0$$

diff w.r.to I_C

$$0 - 0 - R_C - \frac{\partial I_B}{\partial I_C} R_E - \frac{\partial I_B}{\partial I_C} (R_B) - 0 - \frac{\partial I_B}{\partial I_C} R_E - R_E = 0$$

$$-\frac{\partial I_B}{\partial I_C} (R_E + R_E + R_B) = R_C + R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_E}$$

$$S = \frac{1+\beta}{1-\left(\frac{-R_C}{R_E+R_C}\right)}$$

$$S = \frac{1+\beta}{1+\frac{R_C}{R_E+R_C}}$$

2

3.b) Given $I_{DSS} = 20mA$

$V_P = -6V$

$V_{GS} = -3V$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$= 20\times10^{-3}\left(1-\frac{3}{6}\right)^2$$

$$= 20\times10^{-3}\times(0.5)^2$$

$$= 20\times10^{-3}\times 0.25$$

$$= 5\ mA$$

2

2.b) Given $V_{CC} = 22V$

$R_1 = 39k\Omega$

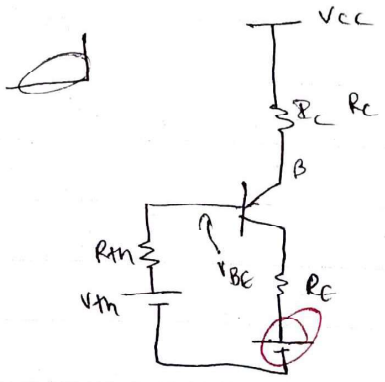
$R_2 = 3.9k\Omega$

$\beta = 140$

$R_E = 1.5k\Omega$

$R_C = 10k\Omega$

circuit is reduced to



Apply KVL at i/p

$$V_{CC} - I_C R_C - V_{CE} - (I_C + I_B) R_E = 0$$

~~$V_{th} - R_{th}(I_B) - V_{BE}$~~

$$I_C = \frac{V_{CC}}{R_C}$$

$$= \frac{22}{10\,k\Omega} = 2.2\,mA$$

$$I_C = \beta I_B$$

$$I_B = \frac{I_C}{\beta} = \frac{2.2\,mA}{140}$$

$$= 1.57 \times 10^{-5}$$

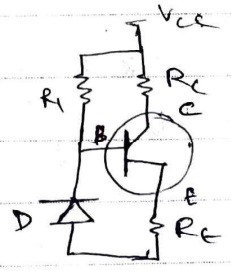
$$V_{CC} - I_C R_C - V_{CE} - I_C R_E - I_B R_E = 0$$

$$22 - (2.2 \times 10^{-3}) \times (10 \times 10^3) - (2.2 \times 10^{-3})(1.5 \times 10^3) - (1.57 \times 10^{-5})(1.5 \times 10^3) = V_{CE}$$

$$V_{CE} = 22 - 22 - 3.3 - 0.023$$

$$V_{CE} = -3.323\ V$$

3.a) Given Diode compensation Technique



Placing Diode in the place of Resistor in Self Biasing Technique

Here the diode is kept in reverse biasing so reverse saturation current flows i.e I_o and remaing current flows Through Base i.e I_B

$$I = I_o + I_B$$

$$I_B = I - I_o$$

Acc to formula

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$= \beta(I - I_O) + (1+\beta) I_{CO}$$

β is more when compared to 1

So '1' is negligible

$$= \beta(I - I_O) + (\beta) I_{CO}$$

$$= \beta I - \beta I_O + \beta(I_{CO})$$

$$I_C = \beta I_B + \beta(I_{CO} - I_O)$$

when the Transistor is made of same materials then reverse current I_O is equal to reverse saturation current I_{CO}

So

$$I_C = \beta I + \beta(I_{CO} - I_{CO})$$

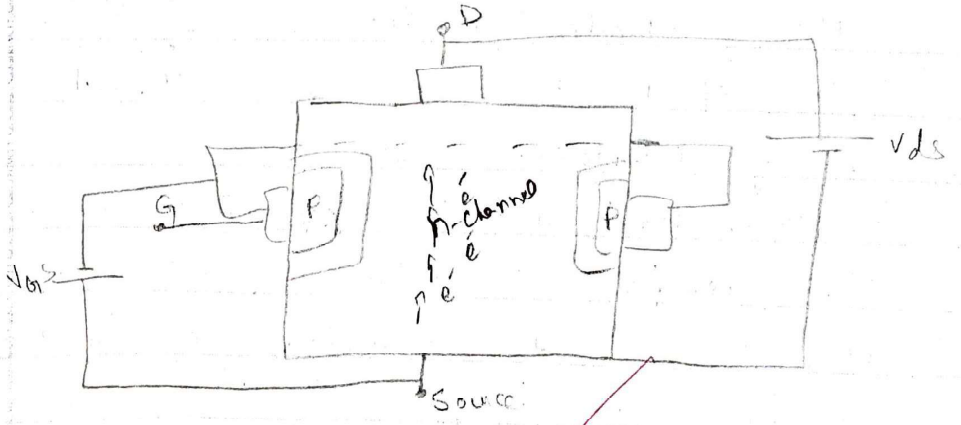
$$I_C = \beta I + 0$$

$$\boxed{I_C = \beta I}$$

3

Here I_C has no effect from reverse saturation current I_{CO} & I_O Because they are Cancelled.

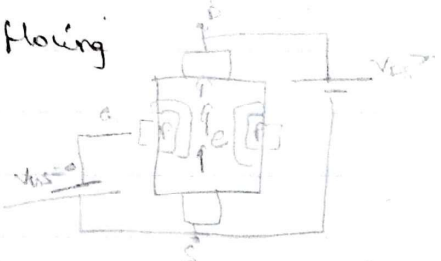
4.a) Let us consider n-~~type~~ channel J-Fet for drawing V-I characteristic & Transfer Characteristics



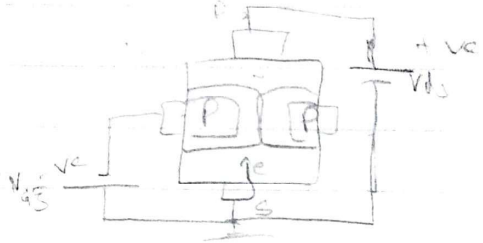
physical structure.

Case (i) :- If $V_{GS} = 0V$ & $V_{DS} = 0$ no current flows throug Transistor.

Case (ii) If $V_{DS} > 0$ V_{DS} is increased & $V_{GS} = 0$ then charge carries are attracted by '+' of Vds and moves from source to drain & current starts flowing in the Transistor

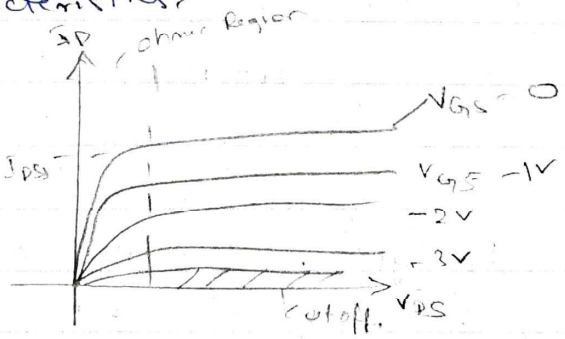


Case (iii) If $V_{DS} > 0$ & $V_{GS} > -Ve$ then the depletion layer penetrates into the n-channel & channel width is reduced Ofhere is no channel for flow of electrons from source to drain so current flowing through the conductor decreases and goes to cutOff Region



From Above Cases we can draw Drain & Transfer Characteristics.

Drain characteristics:-



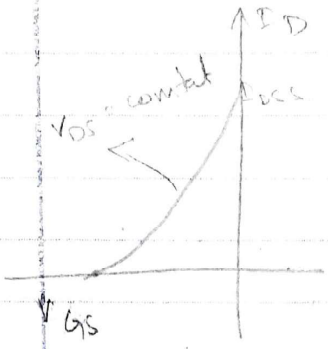
From the above graph we can get drain Resistance.

Drain Resistance (rd) :- It is defined as the rate of change of o/p voltage V_{DS}

with respect to o/p current I_{DS} by keeping V_{GS} constant.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_{DS}} \quad \Big| \; V_{GS} = \text{constant}$$

Transfer characteristics:-



From the Transfer curve we can drive g_m:-

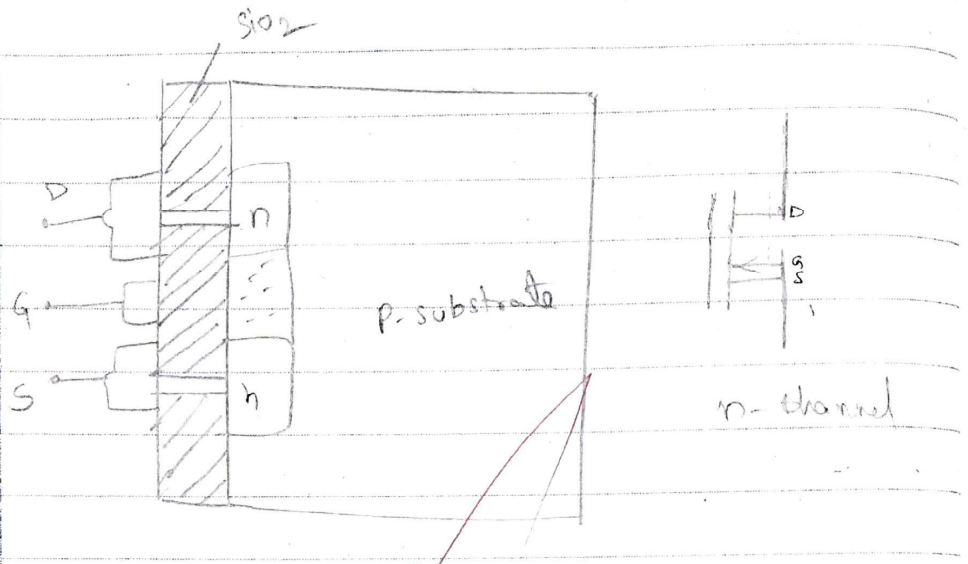
Conductance (g_m):- It is defined as the ratio of change of o/p current with respect to input voltage at constant o/p voltage is called (g_m) conductance

gain conductance $g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big|_{V_{DS} = \text{constant}}$

Amplification factor (μ):- It is defined as the product of drain Resistance and gain conductance

$$\mu = r_d \times g_m$$

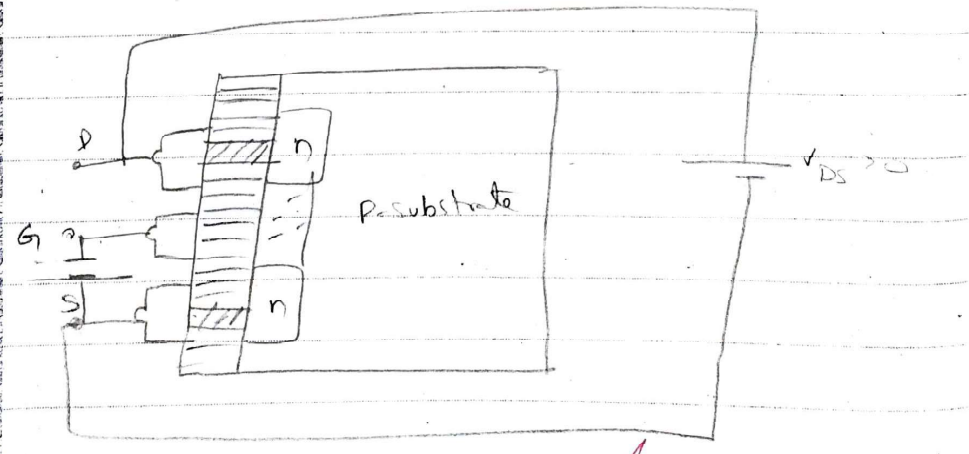
4.b) The N-type / channel MOSFET has pre-existed channel and gate is separated by SiO_2 (semi oxide silicon di-oxide and has p- substrate. It has hight input impedance. Input Resistance is very low



Working conditions:-

Case -(i) If $V_{DS} = 0$ and $V_{GS} = 0$ no charge moves and Transistor is in off conduction and no current flows through Transistor

Case -(ii) If $V_{DS} > 0$ & $V_{GS} = 0$, current flows through the Transistor and Transistor is in on condition. charge carrier moves through Channel from Soure to Drain



Case (iii) If $V_{DS} > 0$ & $V_{GS} >$ -ve ; the width of channel decreases and charge carriers can't move from source to drain. The current flowing Through transistor decreases

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ASSIGNMENT-1

1. Write a short note on P-N junction diode with no bias, forward bias and reverse bias.

2. Derive diode equation expression with current components model.

3. Write an Energy diagram on P-N junction diode and necessary diagram.

4. Write a short note on Junction capacitance?

5. Consider a Ge PN junction at 300^0K with doping concentration $N_A = 1.5 * 10^{18}$ cm^{-3} in the P-type and n-type of the junction respectively. Determine the contact potential across the junction. Assume that intrinsic carrier concentration of Germanium, $n_i = 2.5*10^{13}$ cm^{-3} at 300^0 K.

6. Determine the DC resistance levels for the figure.1 at
   a) I_D =2mA b) I_D = 2mA c) V_D = -10V.

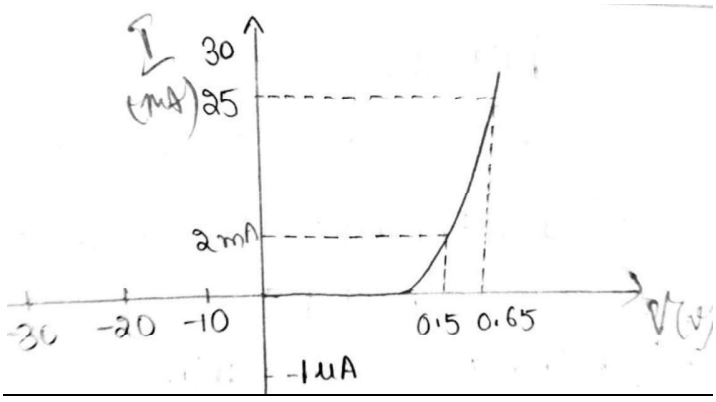

Fig.1: V-I characteristics

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ASSIGNMENT-2

1. In the transistor amplifier shown in figure.1, R_L = 8KΩ, R_1 = 24KΩ, V_{CC} = 24V. Draw the DC and AC load line, and determine the optimum operating point.

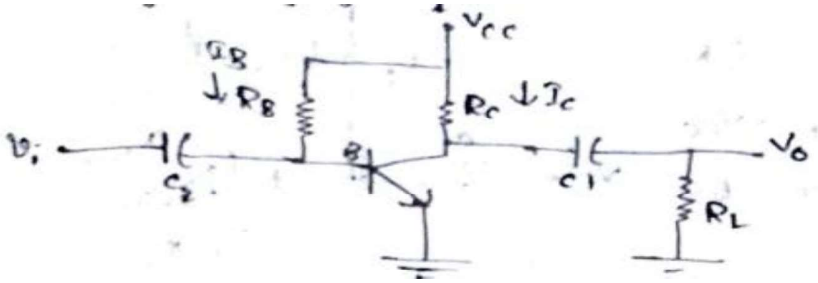


Fig.1: BJT amplifier

2. A silicon transistor with β =100, VCE = +6V, R_C = 3KΩ, R_B = 5KΩ.
   i) Draw the DC load line and determine Q-point
   ii) What is the stability factor?

3. In Germanium transistor used as an amplifier has I_{CBO} = 20μA and h_{FE} = 50. Find IC when I_B = 0.25 m A.

4. Design the circuit in Fig.1, given Q-point values are to be I_{CQ} = 1mA and V_{CEQ} = 6V. Assume V_{CE} = 10V, β = 100, V_{BE} = 0.7V.

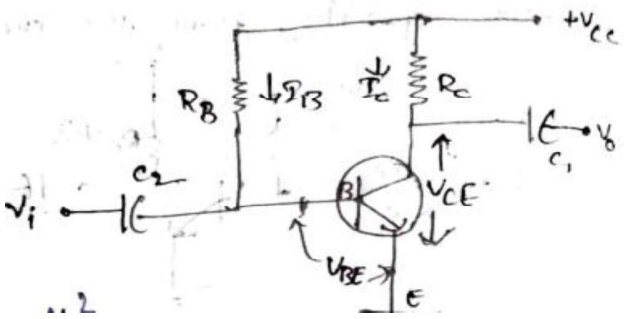


Fig.1: BJT amplifier

5. Consider voltage divider bias circuit, determine the Q-point. Let R_1= 56KΩ, R*2*= 12.2 KΩ, R_C = 2 KΩ, R_E= 400 Ω, V_{CC}=10V, V_{BE}=0.7V, and β = 150.

6. A transistor has I_B = 100μA and I_C= 2mA, find i) β ii) α iii) I_E iv) If I_B crosses by 25mA and changes by 0.6 mA, find the max. value of β.

7. For the given voltage divider configuration circuit, determine the i) DC bias voltage V_{CE} and ii) current I_C and β =140.

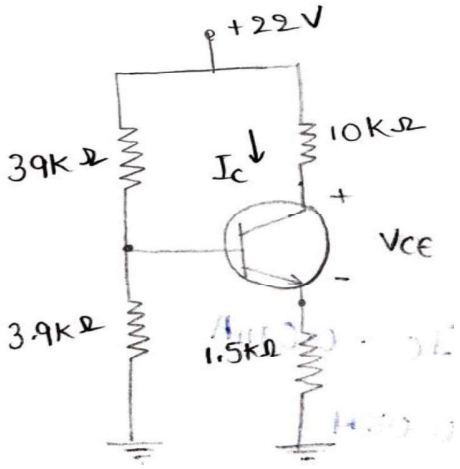


Fig.1. Voltage divider circuit

8. In an N-channel JFET, I_{DSS} = 20mA and V_P = -6V, calculate the drain current when V_{GS} = -3V.

9. Design a MOSFET circuit biased with both positive and negative voltages to meet set of specifications: IDQ= 0.5mA, and VDSQ = 4V, K_n' = 80μA/V^2 , (W/L) = 6.25, and V_{TN} = 1.2V.

S. Mohammed Arif, Roll No: 2109IA04B3, II-I ECE

Electronic Devices & Circuits (EDC)

13/11/22

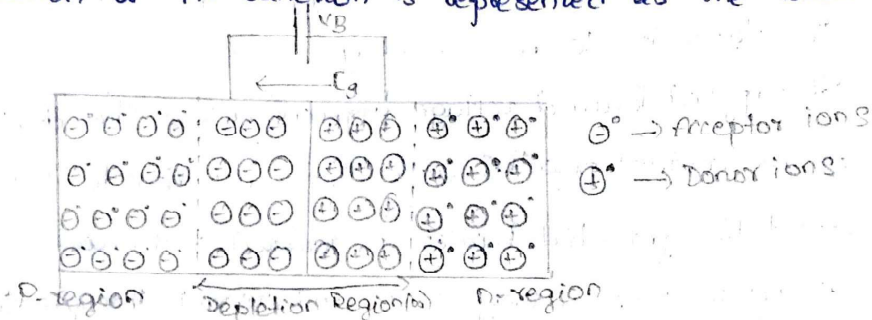
Assignment - 1

1. Write a short note on PN Junction diode, No Bias, Forward Bias and Reverse Bias?

A. Statement :- In a piece of semiconductor material, if one half is doped with p-type impurity and other half with n-type impurity, a junction is formed. This junction is called PN Junction.

Formation of PN Junction :-

The formation of PN Junction is represented as the following



→ The electrons are the majority carriers and holes are the minority carriers in n-type of semiconductor.

→ But the holes are the majority carriers and electrons are the minority carriers in p-type semiconductor.

→ When the electrons move across the junction from n-region to p-region, a net positive charge is built on the n-side of the junction

→ Similarly, due to the diffusion of holes from p-region, a net negative charge is built on the p-side of the junction.

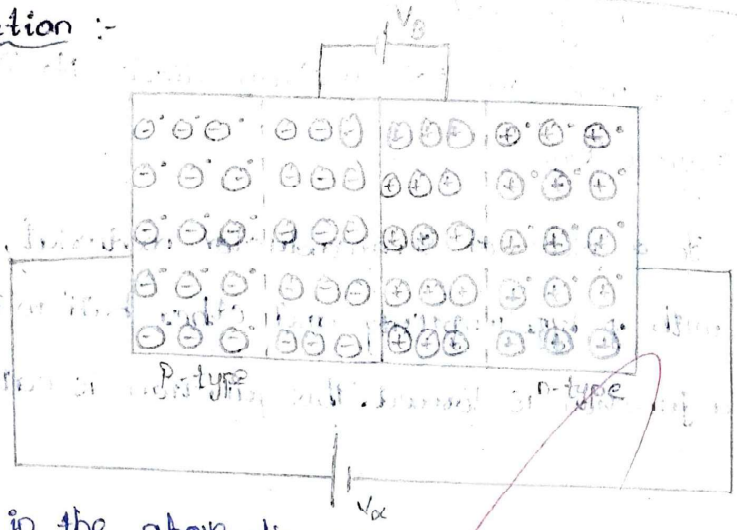
Biasing :- In PN Junction diode ~~two~~ three types of biasing techniques are present.

1) Forward Bias 2) Reverse Bias 3) No Bias

Forward Bias :-

When high potential is connected to p-type and lower potential is connected to 'n' type then majority charge carriers are across the junction which resulting in high current.

Explanation :-



where in the above diagram

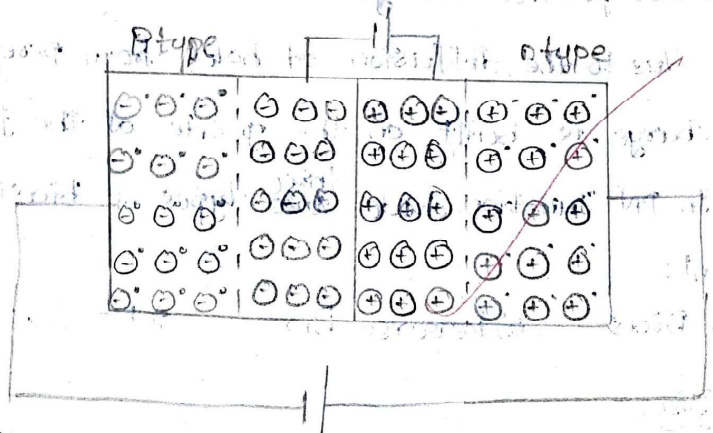
V_α = force direction due to applied potential

V_0 = force due to barrier voltage.

The applied forward voltage appears across the depletion region, As the contact potential acts from n-region to P-region the electrostatic potential barrier is lowered. In forward bias the resistance of PN Junction is very small and current through the diode increases.

Reverse Bias :-

When higher potential is connected to n-type and lower potential is connected to p-type the majority charge carrier are move away from the junction, and only minority charge carriers are move towards the junction which resulting in small current towards Junction.



The Majority carrier move away from the junction because of holes are +ve, so that holes are attracted towards electrons are -ve charged particles, so that attracted towards +ve terminal. In reverse Bias, applied force is added to the force developed by junction voltage

No Bias (or) zero Bias :-

The PN Junction in which no external voltage is applied is called zero Bias pn-Junction. zero Bias PN Junction is also called as un-biased pn-junction.

In n-type semiconductor materials, pentavalent impurities are added while, in p-type semiconductor materials trivalent impurities are added.

2. Diode expression with current components model.

A When a Forward bias is applied to a diode, holes are injected into the n-side and electrons into p side. The no. of these injected minority carriers falls of exponentially with distance from the junction. Since the diffusion current of minority carriers is proportional to the concentration gradient. This current must also vary exponentially with distance.

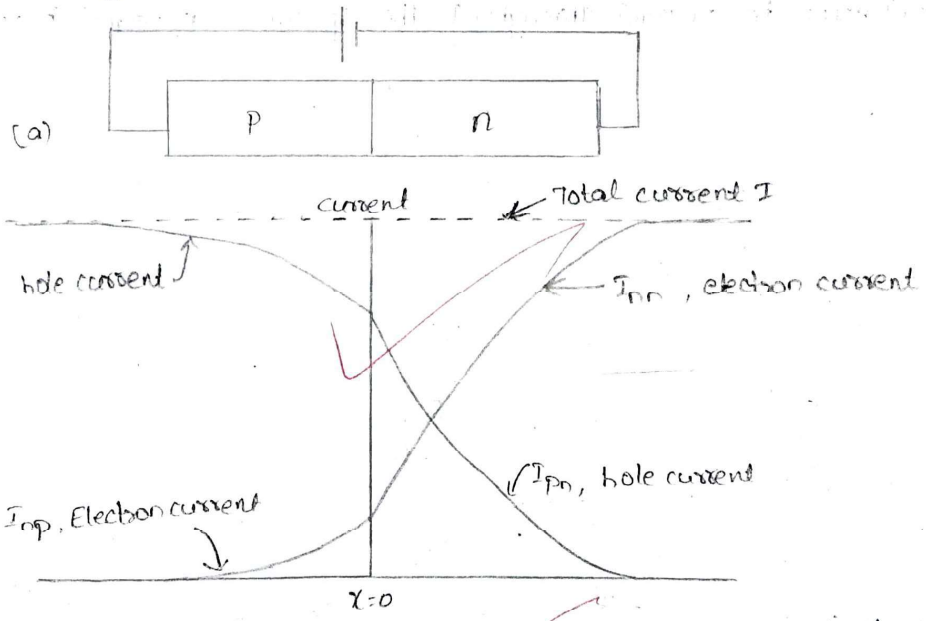


fig: b :- The hole and electron-current components (vs) distance in a pn-junction diode. The space charge region at the junction is assumed to be negligibly small.

Electrons crossing the junction at x=0, from right to left constitute a current in the same direction as hole crossing the junction

from left to right. Hence the total current I at $x=0$ is

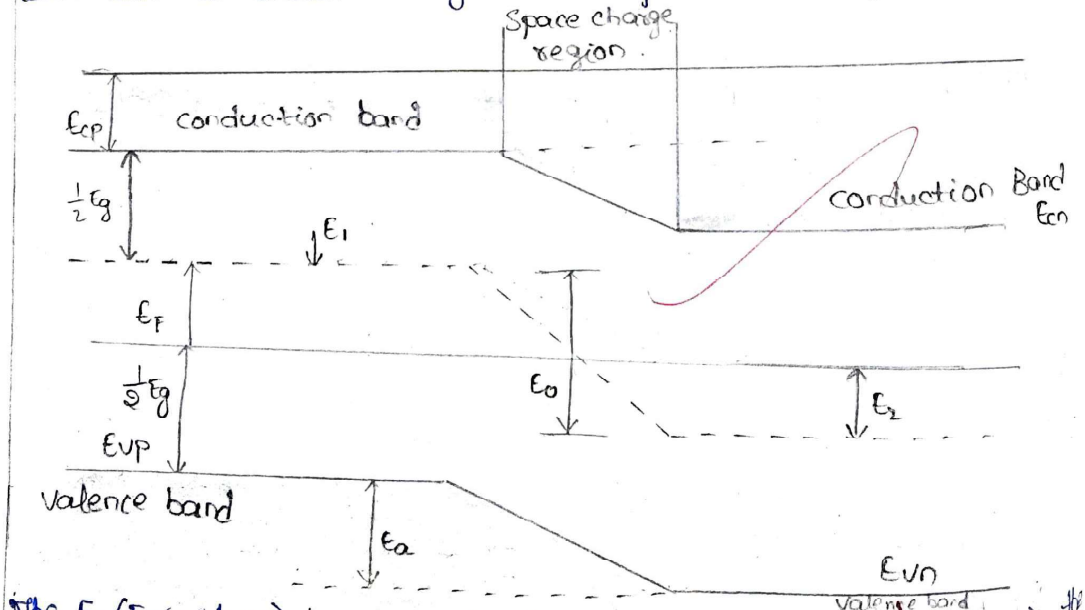
$$I = I_{pn}(0) + I_{np}(0) \longrightarrow (1)$$

Since the current is the same throughout a series circuit, I is independent of x and is indicated as a horizontal line. Consequently in the p-side, there must be a second component of current I_{pp} which when added to I_{np}, gives the total current I. Hence this hole current in the p-side I_{pp} is given by

$$I_{pp}(x) = I - I_{np}(x) \longrightarrow (2).$$

3) Write an Energy Band Diagram on PN-Junction diode and necessary Diagram.

A. A PN-Junction is formed by placing P- and n-type materials in intimate contact on an atomic scale. Under these conditions the Fermi level must be constant throughout the specimen at equilibrium.



The E_F (Fermi level) is closer to the conduction band edge E_{cn} in the n-type material and closer to the valence band edge E_{vp} in the p-side clearly, then the conduction band Edge E_{cp} in the p material cannot be at the same level as E_{cn}, nor can the valence band Edge E_{vn} in the n-side line up with E_{vp}. Hence the energy-band diagram for PN Junction appears as shown below.

$$E_0 = E_{cp} - E_{cn}$$
$$= E_{vp} - E_{vn}$$
$$= E_1 + E_2 \longrightarrow (1)$$

The contact difference of potential, we now obtain an expression for E_0 from the above figure,

$$E_F - E_{vp} = \frac{1}{2} E_g - E_1 \longrightarrow (2)$$

and

$$E_{cn} - E_F = \frac{1}{2} E_g - E_2 \longrightarrow (3)$$

Adding these two equations, we obtain

$$E_0 = E_1 + E_2 = E_g - (E_{cn} - E_F) - (E_F - E_{vp}) \longrightarrow (4)$$

we have,

$$E_g = KT \ln \left[\frac{N_c \cdot N_v}{n_i^2} \right] \longrightarrow (5)$$

where, N_c = Doping concentration in conduction Band.

N_v = Doping concentration in valency Band.

n_i = intrinsic material concentration for si/Ge.

$$E_{cn} - E_F = KT \ln \left(\frac{N_c}{N_D} \right) \longrightarrow (6)$$

$$E_F - E_{vp} = KT \ln \left(\frac{N_v}{N_A} \right) \longrightarrow (7)$$

using eq (5), eq (6), eq (7) in Eq (4).

$$E_0 = KT \ln \left[\frac{N_c \cdot N_v}{n_i^2} \right] - KT \ln \left[\frac{N_c}{N_D} \right] - KT \ln \left[\frac{N_v}{N_A} \right]$$

$$= KT \ln \left[\frac{N_c N_v}{n_i^2} \right] \cdot \frac{N_D}{N_c} \cdot \frac{N_A}{N_v}$$

$$E_0 = KT \ln \left(\frac{N_D \cdot N_A}{n_i^2} \right)$$

Contact Barrier potential, $V_0 = \frac{E_0}{e}$ in $V \longrightarrow (9)$

4) Write a short Notes on Junction capacitance?

A) A Reverse Bias causes majority carriers to move away from the junction thereby uncovering more immobile charges. Hence the thickness of the space-charge layer at the junction increases with reverse voltage. This increased in uncovered charge with applied voltage may be considered a capacitive effect. We may define an incremental capacitance C_T by

$$C_T = \left|\frac{dQ}{dV}\right|$$

where dQ = increase in charge

dV = change in voltage

It follows this defination that a change in voltage dV in a time dt will result in a current, $i = \frac{dQ}{dt}$ given by

$$i = C_T \frac{dV}{dt}$$

The junction capacitance is divided into two types

i) step graded junction

ii) Linear graded junction.

i) Step Graded Junction :- The step graded Junction is also called as Alloy junction.

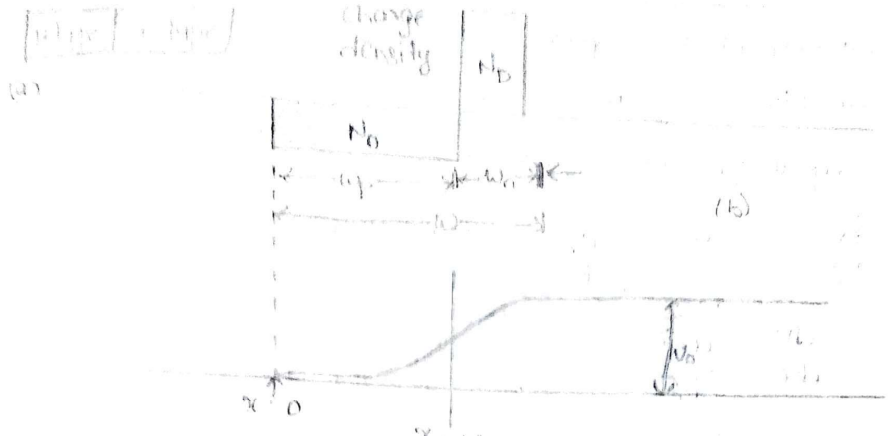
consider a Junction in which there is an abrupt change from acceptor ions on one side to donor ions on the other side. Such a junction is formed experimentally, for example by placing Indium, which is trivalent against n-type germanium and heating the combination to a high temperature for a short time. Such a Junction is called an alloy (or) fusion Junction.

Fig: The charge density and potential variation at a fusion PN Junction ($W \approx 10^{-4}$ cm).

Net charge value Equation is given by

$$\therefore \quad e N_A \cdot W_p = e N_D \cdot W_n \longrightarrow (1)$$

if $N_A << N_D$, Then $W_p >> W_n$



The relationship b/w charge density and potential from poission's law, rule

$$\frac{d^2V}{dx^2} = \frac{e N_A}{\epsilon}$$

$$d^2V = \frac{e N_A}{\epsilon} dx^2$$

Double integration on both sides, we obtain

$$V = \frac{e N_A}{\epsilon} \iint dx\, dx = \frac{e N_A}{\epsilon} x^2 \longrightarrow (2)$$

At $x=0$, $E = -\frac{dV}{dx} = 0 \longrightarrow (3)$

At $x = w = w_p$, $V = \frac{e N_A}{2\epsilon} w^2 \longrightarrow (4)a.$

If $V = +V_B$, $V_B = \frac{e N_A}{2\epsilon} \cdot w^2 = \frac{e N_A}{2\epsilon} w_p^2 \longrightarrow (4)b.$

$$\boxed{w \propto V_B^{1/2}}$$

→ If 'a' is the area of the junction and the charge in the given width is given as $Q = e N_A \cdot wA \longrightarrow (6)$

we have, $C_T = \frac{dQ}{dV} = \frac{d}{dV}(e N_A \cdot wA) \longrightarrow (7)$

From eq (4), (5), $dV = \frac{e N_A}{2\epsilon} \cdot 2w \cdot dw$

$$\frac{dw}{dV} = \frac{\epsilon}{e N_A w} \longrightarrow (8)$$

By using eq (7) and eq (8), we obtain → $C_T = \left|\frac{dQ}{dV}\right| = e N_A \cdot A \left|\frac{dw}{dA}\right|$

$$= e N_A \cdot A \frac{\epsilon}{e N_A \cdot w} = \frac{\epsilon A}{w}$$

$$\boxed{C_T = \frac{\epsilon A}{w}} \longrightarrow (9)$$

ε : permitivity of free space.

w = width b/w two plates.

According to poisson's equations

$$\frac{d^2V}{dx^2} = -\frac{eV}{\varepsilon} = \frac{eN}{E} = \frac{ax}{\varepsilon} \rightarrow (10)$$

$$\frac{dV}{dx} = \frac{ax^2}{2\varepsilon}$$

$$V = \frac{ax^3}{2 \times 3\varepsilon} = \frac{ax^3}{6\varepsilon} \rightarrow (11)$$

At $x = w$, & $V = V_B$ eq (11) becomes,

$$V = V_B = \frac{aw^3}{6\varepsilon} \Rightarrow w = \left(\frac{6\varepsilon V}{a}\right)^{1/3}$$

$$\boxed{w \propto V^{1/3}} \rightarrow (12)$$

2) Linear Graded Junction :- It is also called as a Grown Junction. A second form of Junction called a grown junction is obtained by drawing a Single crystal form a melt of germanium whose type is changed during the drawing process by adding first p-type and then n-type impurities.

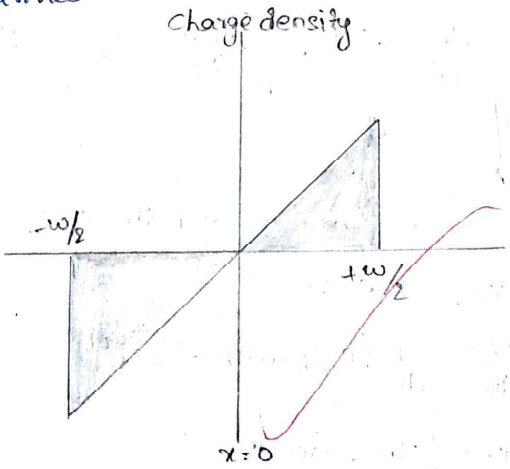


Fig : The charge-density variation at a grown pN Junction.

problems:-

P1. consider a Ge PN Junction at 300° K with doping concentration $N_A = 1.5 \times 10^{18}\ cm^{-3}$ and $N_D = 2 \times 10^{15}\ cm^{-3}$ in the p-type and n-type of the junction respectively. Determine the contact potential across the junction. Assume that intrinsic carrier concentration of Germanium, $n_i = 2.5 \times 10^{13}\ cm^{-3}$ at 300° K.

Sol: Given, $N_A = 1.5 \times 10^{18}\ cm^{-3}$

$N_D = 2 \times 10^{15}\ cm^{-3}$

We know that $\Rightarrow E_0 = KT \ln\left(\frac{N_D \cdot N_A}{n_i^2}\right)$

$$E_0 = 300 \times 1.38 \times 10^{-23} \ln\left[\frac{2 \times 10^{15} \cdot 1.5 \times 10^{18}}{(2.5 \times 10^{13})^2}\right]$$

$KT = 0.0259\ eV$

$E_0 = 0.398\ eV$

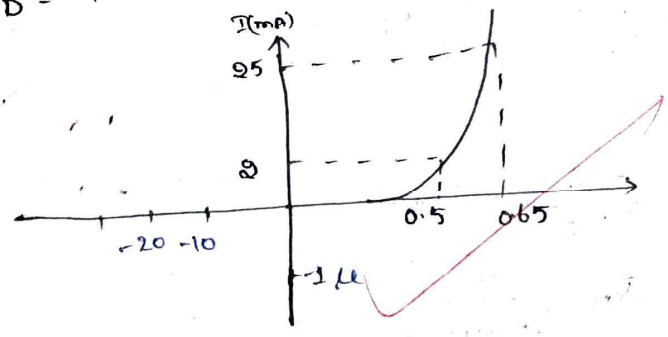
contact potential, $\Rightarrow V_0 = \frac{E_0}{E}$ in V

$V_0 = \frac{E_0}{e} \cdot 1V$

$V_0 = 0.398$

$\Rightarrow \boxed{V_0 = 0.398\ V}$

P2) Determine the DC resistance levels for the figure at a) $I_D = 2mA$ b) $I_D = 25\ mA$ c) $V_D = -10\ V$.



a) $R_D = \frac{V_D}{I_D} = \frac{0.5}{2mA} = \frac{0.5}{2 \times 10^{-3}} = 250\ \Omega$

b) $R_D = \frac{V_D}{I_D} = \frac{0.85}{25 \times 10^{-3}} = 34\ \Omega$

c) $R_D = \frac{-10}{-1\mu} = \frac{10}{1 \times 10^{-6}} = 1 \times 10^7\ \Omega \Longrightarrow$ Reverse bias condition

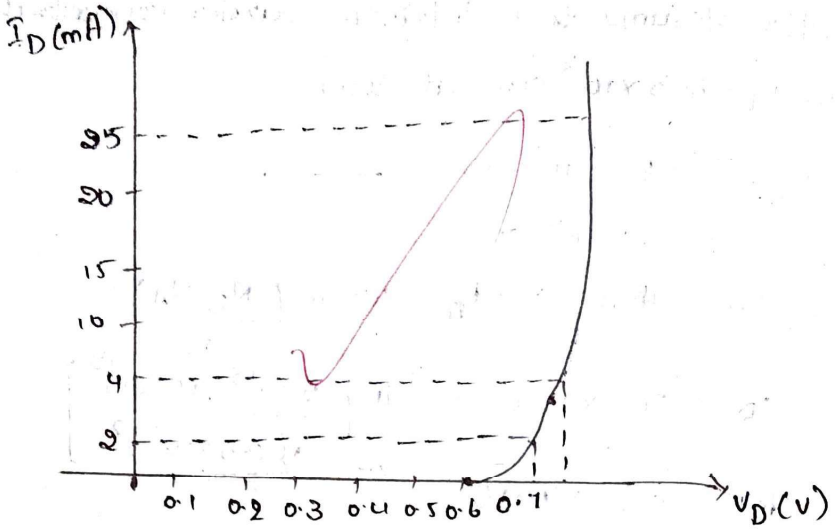
$= 10\ M\Omega$

3) For the characteristics of fig. A2

a) Determine the ac resistance at $I_D = 2mA$

b) Determine the ac resistance at $I_D = 25\,mA$

c) compare (a) and (b) quetions resistances to DC resistances.



VI - characteristics of ΔV_d a PN diode.

A) a) $\Delta I_d = 4mA - 0mA = 4mA$

$\Delta V_d = 0.76V - 0.65V = 0.11V$

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.11}{4mA} = \frac{0.11}{4\times10^{-3}} = 27.5\,\Omega$$

b) $I_d = 30\,mA - 20\,mA = 10\,mA$

$V_d = 0.8V - 0.78V = 0.02$

$$r_d = \frac{0.02}{10\times10^{-3}} = \frac{0.02}{10^{-2}} \Rightarrow R_d = 2\,\Omega$$

c) at $I_d = 2mA$

$$R_d = \frac{V_D}{I_D} = \frac{0.76}{2\times10^{-3}} = 380\,\Omega$$

at $I_d = 25mA \Rightarrow R_D = \frac{0.85}{25\times10^{-3}}$

$R_D = 34\,\Omega$

r_d (2mA) = 27.5 Ω

r_d (25 mA) = 2Ω

⇒ Dynamic resistance is minimum value as compare to the static resistance.

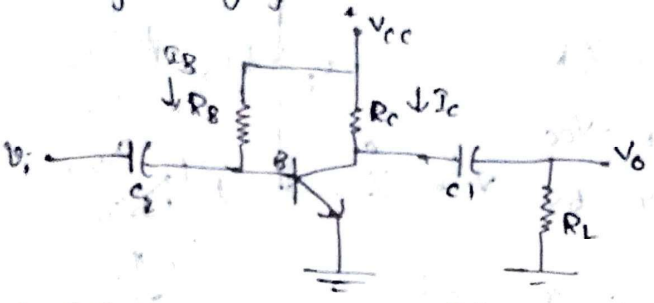
10/10

Akhtar 16/1/21

Assignment-3

1) problems :-

1. In the transistor Amplifier shown in figure, $R_L = 8\,k\Omega$, $R_1 = 24\,k\Omega$, $V_{cc} = 24V$. Draw the DC load line and Determine the optimum operating point. Also draw the Ac load line.



i) DC load line :-

$V_{cc} - I_c R_c - V_{CE} = 0$

$V_E = V_{cc} - I_c R_c$

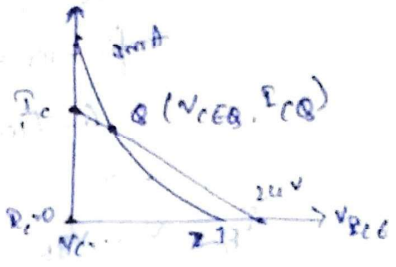
$0 = V_{cc} - I_c R_c$

$V_{cc} = I_c R_c$,

max. $V_{CE} = V_{cc} = 24V$

($I_c = 0$)

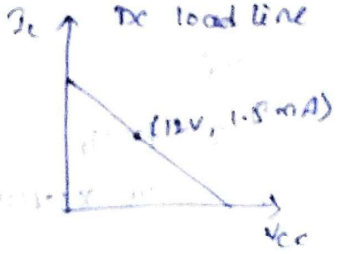
max I_c ($V_{CE} = 0V$) $= \frac{V_{cc}}{R_c} = \frac{24}{8\,k\Omega} = 3mA$



ii) Q-point, $V_{CQ}, I_{CQ} = \left(\frac{V_{cc}}{2}, \frac{I_c}{2}\right)$

$= \left(\frac{24}{2}, \frac{3mA}{2}\right)$

$= 12V, 1.5mA$



Ac load line :-

Max $V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$

max $I_c = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$ where $R_{ac} = R_c' \| R_L$

$= 8K \| 24K\Omega$

$= 6K\Omega$

max $V_{CE} = 12V + (1.5mA + 6K\Omega) = 21V$

max $I_c = 1.5mA + \left(\frac{12V}{6K\Omega}\right)$

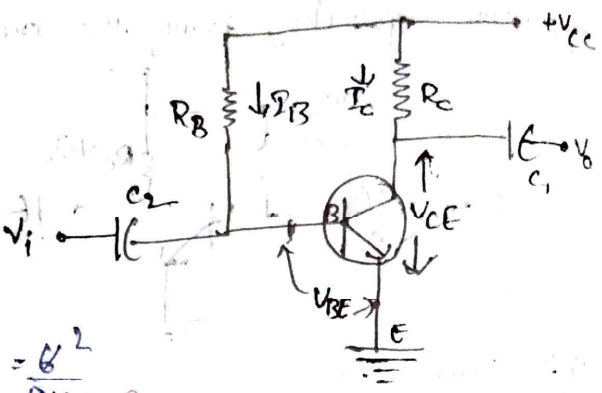
$= 3.5mA$

(2) A silicon transistor with $\beta = 100$, $V_{CE} = +6V$, $R_C = 3k\Omega$,

i) draw the dc load line and determine Q point.

ii) what is the stability factor.

Sol:



$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C$

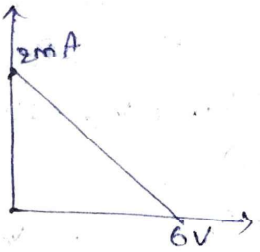
Max V_{CE}, $V_{CE} = V_{CC}$

at $I_C = 0$, $V_{CE} = 6V$

Max I_C

at $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C} = \frac{6}{3k\Omega}$

$= 2mA$



$V_{CEQ} = V_{CC} - \beta \cdot I_B \cdot R_C$

$= [6 - 100 I_B \cdot 3k\Omega]$

$= .6 - (100 \times 10\mu) 3k\Omega$

$= 3$

$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{6 - 0.7}{530k\Omega} = \frac{5.3}{530k\Omega}$

$= 10 \times 10^{-6} A$

(or) $= 10\mu A$

$I_{CQ} = \beta \cdot I_B$

$= 100 \times 10\mu A \Rightarrow 1mA$

ii) $S = 1 + \beta$

$= 1 + 100 \Rightarrow 101 \approx S$

(3) In a Germanium transistor used as an amplifier has I_{CO} 20μA and $h_{FE} = 50$. Find I_C when $I_B = 0.25mA$.

Sol:

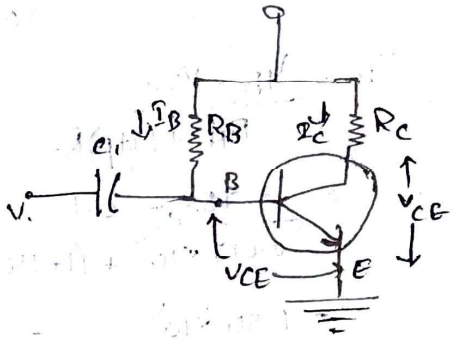
$I_C = \beta \cdot I_B + (1 + \beta) I_{CO}$

$= (50)(0.25 \times 10^{-3}) + (1 + 50) \times 10 \times 10^{-6} \Rightarrow (12.5 \times 10^{-3}) + (0$

$= 0.925 A$ (or) $0.925 + (5.1 \times 10^{-7})$

$= 13.01 mA$ $= 13.01 mA$

④ Design the circuit shown in fig P.1, given Q-point values are to be $I_{CQ} = 1mA$ & $V_{CEQ} = 6V$. Assume $V_{CE} = 10V$, $\beta = 100$, $V_{BE} = 0.7V$.



Sol:

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}}$$

$$= \frac{10-6}{1\times10^{-3}} = 4\ K\Omega$$

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{10-0.7}{I_B}$$

$$I_C = \beta \cdot I_B$$

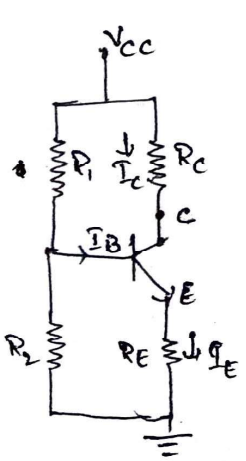
$$I_B = \frac{I_C}{\beta} = \frac{I_{CQ}}{100} = \frac{1\times10^{-3}}{100}$$

$$I_B = 0.01\ mA$$

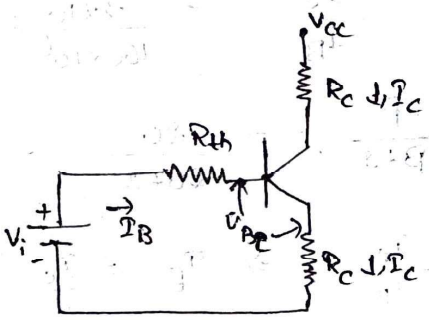
$$R_B = \frac{10-0.7}{0.01\times10^{-3}} \Rightarrow R_B = 930\ K\Omega$$

$$= 0.93\ m\Omega$$

⑤ Given a voltage divider bias circuit shown in fig P.1, determine the Q-point, let $R_1 = 56K\Omega$, $R_2 = 12.2K\Omega$, $R_C = 2K\Omega$, $R_E = 400\Omega$, $V_{CC} = 10V$, $V_{BE}(ON) = 0.7$ & $\beta = 150$.



$\Rightarrow$



Sol:

$$V_{th} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

$$= \left(\frac{12.2K\Omega}{(5+12.2)}\right) 10. \Rightarrow V_{th} = 1.788$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{56 \times 12.2}{56 + 12.2}$$

$$= 10.017\ K\Omega$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta)R_E}$$

$$= \frac{1.788 - 0.7}{0.017 \times 10^{-3} + (1+150)400}$$

$$= 1.54 \times 10^{-5} = 15.4 \times 10^{-6}$$

$$= 15.4\ \mu A$$

$$I_{CQ} = \beta I_B$$

$$= 150 \times 1.54\Omega \times 10^{-5}$$

$$= 2.31 \times 10^{-3} = 2.31\ mA$$

$$V_{CEQ} = V_{CC} - I_C R_C$$

$$= 10 - 2.3 \times 10^{-3} + 2 \times 10^{3}$$

$$V_{CEQ} = 5.4\ V.$$

6) A transistor has $I_B = 100\mu A$ & $I_C = 2mA$, find i) β b) α c) I_E d) If I_B crosses by 25 mA & I_C changes by 0.5 find the max value of β.

Sol:- i) $I_C = \beta I_B$

$$\beta = \frac{I_C}{I_B} = \frac{2 \times 10^{-3}}{100 \times 10^{-6}} = 20$$

ii) $$\alpha = \frac{\beta}{\beta + 1} = \frac{20}{20 + 1} = 1.952$$

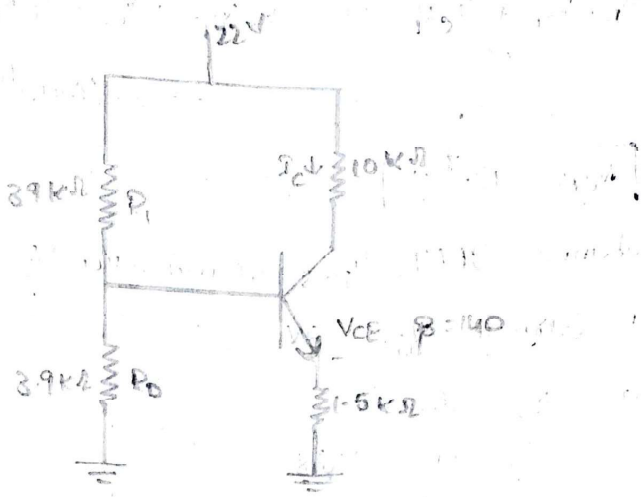
iii) $$\alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha}$$

$$I_E = \frac{2 \times 10^{-3}}{0.952}$$

$$= 2.1 \times 10^{-3}$$

$$= 2.1\ mA.$$

(4) For the voltage divide configuration of fig. Determine the i) DC bias voltage V_{CE} and ii) current I_C.



Sol Given data,

$R_1 = 39k\Omega$, $R_2 = 3.9k\Omega$, $R_C = 10k\Omega$, $R_E = 1.5k\Omega$, $\beta = 140$

$$V_{Th} = \frac{R_2}{R_1 + R_2} \quad ; \quad V_{CE} = \frac{3.9\times10^3}{(39+3.9)\times10^3} \times 22$$

$$= \frac{3.9\times10^3}{42.9\times10^3}$$

$$\boxed{V_{Th} = 2V.}$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

$$= \frac{3.9\times10^3 \times 3.9\times10^3}{(39+3.9)\times10^3} \Rightarrow \boxed{R_{Th} = 3.5\ k\Omega}$$

Apply KVL for input,

$$-V_{th} + I_B R_{th} + V_{BE} + I_C R_E = 0$$

$$-V_{th} + I_B R_{Th} + V_{BE} + I_B R_E = 0$$

$$I_B(R_{Th} + R_E) = V_{Th} - V_{BE}$$

$$\gamma = 1+\beta = 141$$

$$I_B = \frac{2 - 0.1}{3.5\times10^3 + (141)(15\times10^3)}$$

$$I_B = 6.04\mu A$$

$$\boxed{I_B = 6\mu A}$$

$I_C = \beta I_B = (140)(6\times10^{-6})$

$= 0.84\,mA$

$-V_{CC} + I_B R_B + V_{CE} + I_E R_E = 0 \Rightarrow V_{CC} = V_{CC} - I_B R_E - I_E R_E$

$= 20 - (6\times10^{-6}\times10\times10^{3}) - (0.8\times$
$(1.5\times$

$\boxed{V_{CE} = 12.34V}$

8) In an n-channel JFET, $I_{DSS} = 20\,mA$ and $V_p = -6V$, calculate the Drain current $V_{GS} = -3V$.

Sol: Given data, $I_{DSS} = 20mA$

$V_p = -6V$, $V_{GS} = -3V$

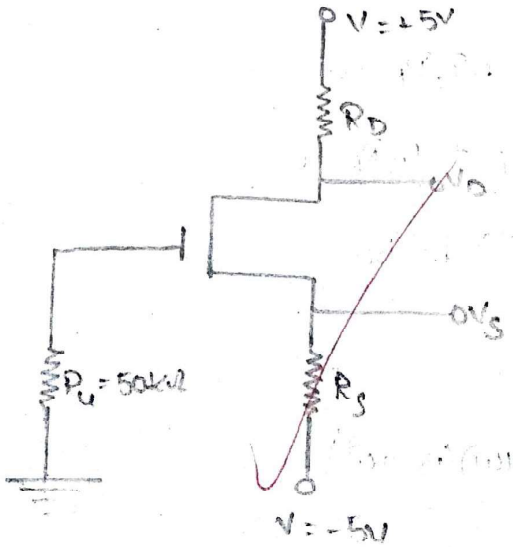
$I_D = ?$

∴ Drain current, $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$

$I_D = 20\times10^{-3}\left[1 - \left(\frac{+3}{-6}\right)\right]^2$

$\boxed{I_D = 5mA}$

9) Design a MOSFET circuit biased with both positive and negative voltages to meet a set of specifications. The circuit diagram to be configured is shown in fig. Design the circuit such that $I_{DQ} = 0.5mA$ and $V_{DSQ} = 4V$; standard resistor are to be used in final design. A transistor with nominal parameters of k_n: $20\,\mu A/V^2$, $(W/L) = 6.25$ and $V_{TN} = 1.2V$ is available.



Sol Given $I_{DQ} = 0.5mA$

$V_{DSQ} = 4V$

$K'_n = 80\mu A/V^2$

$\frac{W}{L} = 6.25$, $V_{TN} = 1.2V$

For above, fig $V_G = 0$

$V_{GS} = V_G - V_S$

$= 0 - V_S$

$V_S = V_G$

To find V_S we require V_{GS} & V_G is obtained from current equation.

i.e, $K'_n = \frac{W}{L}[V_{GS} - V_{TN}]^2$

$0.5 \times 10^{-3} = 80 \times 10^{-6} \times 6.25 [V_G - 1.2)^2$

$(V_{GS} - 1.2)^2 = \frac{0.5 \times 10^3}{80 \times 6.25}$

$(V_{gs} - 1.2)^2 = 1$

$\boxed{V_{gs} = 2.2V} \Rightarrow \because V_S = -V_{GS}$

$\boxed{V_S = -2.2V}$

From this we can calcute, R_S

$R_S = \frac{V_S - (-5)}{I_D} = \frac{-2.2 + 5}{0.5mA}$

$\boxed{R_S = 5.6 k\Omega}$

Given $V_{DSQ} = 4V$, $V_{DS} = V_D - V_S$

$4 = V_D - V_S$

$= V_D - (-2.2)$

$4 = V_D + 2.2$

$\boxed{V_D = 1.8V}$

9/10

From this we can calculate R_D

$R_D = \frac{5 - V_D}{I_D} = \frac{5 - 1.8}{0.5mA} = \frac{3.2}{0.5mA}$

$\boxed{R_D = 6.4 k\Omega}$

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II B.Tech I-Semester - Mid-I *Examinations*

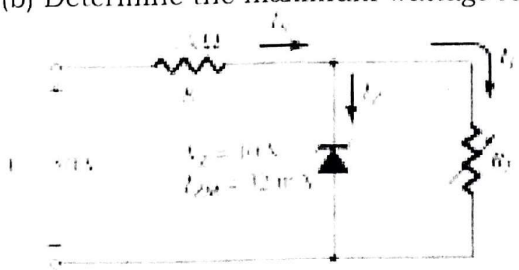
Electronic Devices and Circuits

ECE

Max. Marks: 20 **Date: 08 - 12 - 2022** **Time: 2 Hours**

Note: 1. Answer first question compulsorily. (5 x 1 = 5 Marks)

2. Answer Any *THREE* from 2 to 5 questions. (3 x 5 = 15 Marks)

Q.No			M	CO	BL
Q.1	a)	What is meant by Diffusion Current in a Semi-conductor?	1M	CO1	BL1
	b)	Write short notes about Zener break down mechanism.	1M	CO1	BL1
	c)	Define the Clipper circuit and draw the simple Positive clipper.	1M	CO3	BL1
	d)	Draw the circuit of L-C filter.	1M	CO3	BL1
	e)	In practice, NPN transistor is more preferred than PNP transistor. Why?	1M	CO2	BL1
Q.2	a)	Derive the current equation of P-N junction diode.	3M	CO1	BL2
	b)	The voltage across a Germanium diode at room temperature is 0.7 volts and 5mA current flows through it. If the voltage across diode increases to 0.75 volts, Calculate diode current. (Assume V_T = 26mV).	2M	CO1	BL2
Q.3	a)	Derive the expression of the Space charge or transition capacitance of PN diode under reverse bias	2M	CO1	BL1
	b)	For the network of Fig, a) Determine the range of R_L and I_L that will result in V_{RL} being maintained at 10 V. (b) Determine the maximum wattage rating of the diode. 	3M	CO3	BL3
Q.4	a)	Draw the neat diagram of Full-wave rectifier with capacitor filter and explain its principle of operation and derive its Ripple factor.	2M	CO3	BL2

	b)	Voltage of 5sinwt is applied to Half Wave Rectifier with load resistance of 5KΩ. Calculate the following i) Maximum DC Voltage ii) R.M.S iii) Ripple Factor iv) PIV v) Efficiency	**3M**	CO3	BL3
Q.5	**a)**	Define α, β and γ. Express β in terms of α and γ.	**2M**	CO2	BL2
	b)	With neat sketch explain the different current components of transistor and derive the current equation for transistor suitable for CB and CE configurations.	**3M**	CO2	BL2

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II B.TECH I SEMESTER MID-I EXAMINATIONS

ELECTRONIC DEVICES AND CIRCUITS

ECE

Max.Marks: 20 Date: 08-12-2022 Time: 2 Hours

SCHEME OF EVALUATION (Solutions)

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1 a) Diffusion Current in a Semiconductor;

Diffusion current is a current in a semiconductor caused by the diffusion of charge carriers due to the concentration gradient of charge carriers.

-That means diffusion current is due to movement of holes from p-type to n-type sides.

b) Zener breakdown mechanism;

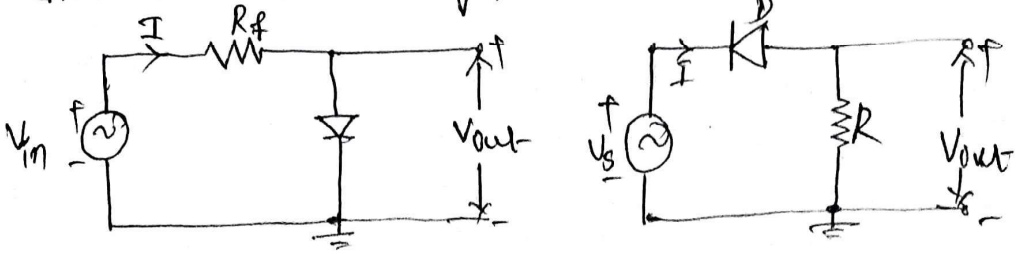
Zener break down occurs in heavily doped junctions in which the transition from the p-side to the n-side is very abrupt.

When the P and N regions are heavily doped conditions, the potential barrier separating carriers on the two sides of the junction is very narrow, and a quantum-mechanical process called tunneling can take place.

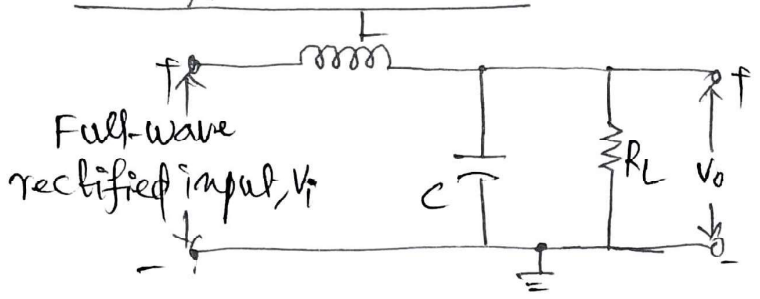
c) Clipper;

A clipper is a circuit designed to prevent a signal from exceeding a predetermined reference voltage level and does not distort the remaining part of the applied wave form.

Circuit;



(d) L-C filter circuit:



(e) In practice, NPN Transistors are preferred than PNP transistors because NPN transistors provide better conductivity, fast switching rates, and small in size comparitively.

2a) Current Equation of P-N junction diode:

When a forward bias is applied to a diode, holes are injected from P-side to the N-side. Due to this, the concentration of holes in the N-side P_n is increased from it thermal equilibrium value (P_{no}) and injected hole concentration $P_n(x)$ decreases exponentially with respect to distance x as shown in Fig.1

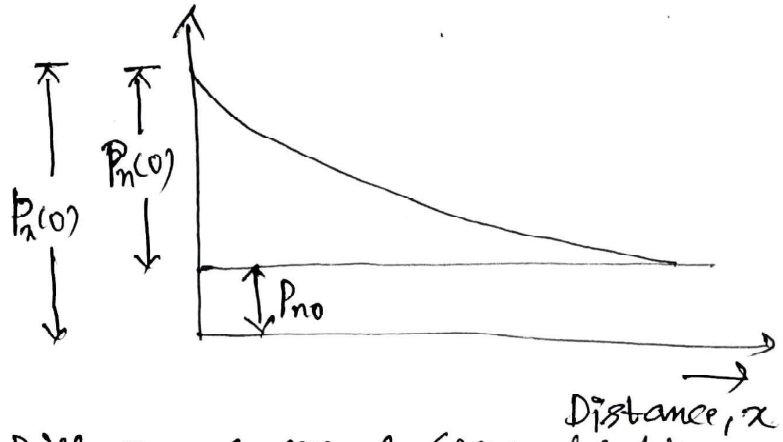


Fig.1: Diffusion current concentration

We have $P_n(x) = P_n - P_{no} = P_n(0)\, e^{-x/L_p}$ — (1)

Where L_p is the diffusion length for holes in the N-material

$$P_n(x) = P_{no} + P_n(0)\, e^{-x/L_p} \quad — (2)$$

2b) Given data: Germanium diode, Ge
At room temparature 0.7V & 5mA, $\eta = 1$

we have $I = I_0 (e^{V/\eta V_T} - 1)$

$5 \times 10^{-3} = I_0 (e^{0.7/1 \times 26 \times 10^{-3}} - 1)$

$= I_0 (4.9 \times 10^{11})$

$I_0 = \frac{5 \times 10^{-3}}{4.9 \times 10^{11}} = 1.0 \times 10^{-14}$

At t = constant $\Rightarrow I = I_0 (e^{V/\eta V_T} - 1)$ for $V = 0.75$

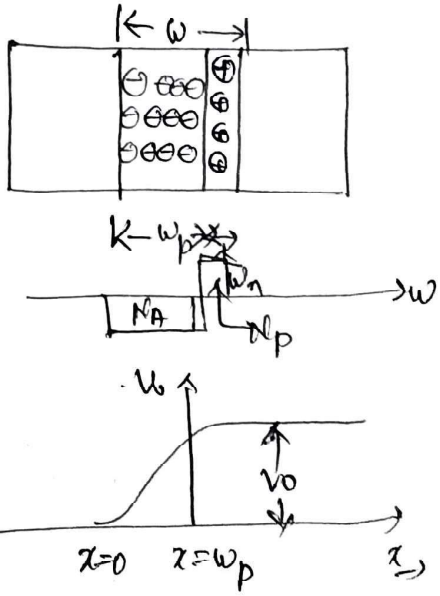
$I = 1.0 \times 10^{-4} (e^{\frac{0.75}{1 \times 26 \times 10^{-3}}} - 1)$

$I = 0.03 \mu A$.

3a) Space charge or transition capacitance derivation:

Transition in reverse bias:

$$C = \frac{dQ}{dV} = \frac{dQ}{dw} \times \frac{dw}{dV} \quad -(1)$$



Step graded:

$$C_T = \left|\frac{dQ}{dV}\right| = e \cdot N_A \cdot A \left|\frac{dw}{dV}\right| \quad -(2)$$

we have $\left|\frac{dw}{dV}\right| = \frac{\epsilon}{eN_A w}$, and hence

$$C_T = e \cdot N_A \cdot A \left(\frac{\epsilon}{eN_A w}\right) = \frac{\epsilon A}{w} \quad -(3)$$

Linear graded:

According poissions equations, $\frac{d^2V}{dx^2} = \frac{-\rho}{\epsilon} = \frac{ax}{\epsilon} \quad -(4)$

$$\frac{dV}{dx} = \frac{ax^2}{2\epsilon} \quad -(5)$$

$$V = \frac{ax^3}{2 \times 3\epsilon} = \frac{ax^3}{6\epsilon} \quad -(6)$$

where $x = w$, $V = \frac{aw^3}{6\epsilon} \Rightarrow w^3 = \frac{6\epsilon V}{a} \Rightarrow w = \left(\frac{6\epsilon V}{a}\right)^{1/3} \Rightarrow \boxed{w \propto V^{1/3}} \quad -(7)$

Injected hole concentration at $x=0$ is

$$P_n(0) = P_n(0) - P_{no} \quad -③$$

These several components of hole (or electron) concentration are shown in Fig. 1.

Let P_p and P_n hole concentration at the edge of the space charge in the P- and n-side, respectively.

Let $V_B = V_0 - V$, be the effective barrier potential across the depletion layer. Then

$$P_p = P_n e^{V_B/V_T} \quad -④$$

For forward currents, the hole current crossing the junction into N-side with $x=0$ is

$$I_{pn}(0) = \frac{A e D_p P_n(0)}{L_p} = \frac{A e D_p \cdot P_{no} (e^{V/V_T} - 1)}{L_p} \quad -⑤$$

The electron-current crossing the junction into the p side with $x=0$ is

$$I_{np}(0) = \frac{A e D_n \cdot N_p(0)}{L_n} = \frac{A e P_n n_{p0}}{L_n} \left(e^{V/V_T} - 1\right) \quad -⑥$$

Total diode current $I = I_{pn}(0) + I_{np}(0) = I_0 (e^{V/V_T} - 1)$ -⑦

where $I_0 = \frac{A e D_p P_{no}}{L_p} + \frac{A e D_n n_{p0}}{L_n}$ = reverse saturation current -⑧

The general equation of the diode current is approximately given by $I = I_0 (e^{V/\eta V_T} - 1)$ -⑨

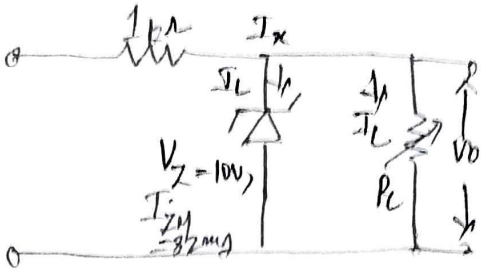
where I – diode current; V – External voltage applied to the diode

η – a constant; K – Boltzman constant

q – charge of the electron; T = temperature of diode junction

3b)

a) we have from fig. 1



$$R_{L\,min} = \frac{R V_Z}{V_i - V_Z} = \frac{(1k\Omega)(10V)}{50V - 10V} = \frac{10K\Omega}{40} = 250\Omega$$

$$V_R = V_i - V_Z = 50V - 10V = 40V.$$

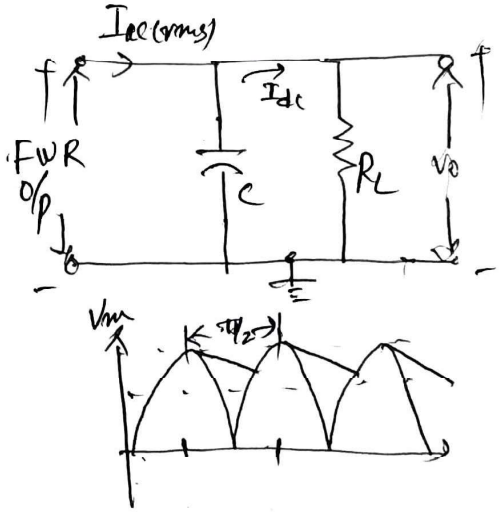
$$I_R = \frac{V_R}{R} = \frac{40V}{1k\Omega} = 40mA$$

$$I_{L\,min} = I_R - I_{ZM} = 40mA - 32mA = 8mA$$

$$R_{L\,max} = \frac{V_Z}{I_{L\,min}} = \frac{10V}{8mA} = 1.25k\Omega$$

b) $P_{max} = V_Z \cdot I_{ZM} = (10V) \times (32mA) = 320mW$

4a) capacitor filter:



Derivation:

$$I_{dc} = \frac{Q_{discharge}}{T/2}$$

$$Q_{discharge} = I_{dc} \cdot \frac{T}{2}$$

where $T = \frac{1}{f}$

$$Q_{discharge} = \frac{I_{dc}}{2f} \quad -(1)$$

$$Q_{charge} = C \cdot V_m \quad -(2)$$

charge conservation, $Q_{charge} = Q_{discharge}$

$$C \cdot V_m = \frac{I_{dc}}{2f} \Rightarrow V_m = \frac{I_{dc}}{2fC} \quad -(3)$$

For triangular wave, $V_{acrms} = \frac{V_m}{2\sqrt{3}} \Rightarrow V_{acrms} = \frac{I_{dc}}{4\sqrt{3}fC}$. $-(4)$

$$V_{acrms} = \frac{I_{dc} \cdot R_L}{4\sqrt{3}fC \cdot R_L} = \frac{V_{dc}}{4\sqrt{3}fC \cdot R_L} \Rightarrow \text{Ripple factor} = \frac{V_{acrms}}{V_{dc}} = \frac{1}{4\sqrt{3}fC \cdot R_L} \quad -(5)$$

4b)

(i) $V_m = 5V$

Max. DC Voltage $= \frac{V_m}{\pi} = \frac{5}{3.14} = 1.59$

(ii) RMS Voltage $= \frac{V_m}{2} = \frac{5}{2} = 2.5V$

(iii) Ripple factor $= \frac{V_{ac(rms)}}{V_{dc}} = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{2.5}{1.59}\right)^2 - 1} = 1.21$

(iv) $PIV = V_m = 5V$

(v) Efficiency $= \frac{P_{dc}^2}{P_{rms}^2} \times 100\% = \frac{V_{dc}^2/R_L}{V_{rms}^2/R_L} \times 100\% = \frac{(1.59)^2}{(2.5)^2} \times 100\%$

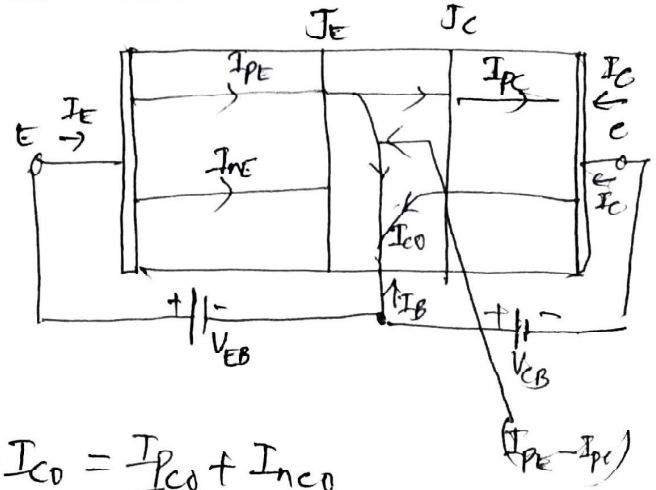
$= 40.5\%$

5a) α, β, and γ Definitions:

$\alpha = \frac{I_C}{I_E}$ — (1) ; $\beta = \frac{I_C}{I_B}$; $\gamma = \frac{I_E}{I_B}$ — (2)

β interms of α & γ is, $\boxed{\beta = \frac{\alpha}{1-\alpha}}$ — (4) & $\boxed{\beta = \gamma - 1}$ — (5)

b) Different current components in a transistor:



$\alpha = \frac{I_{PC}}{I_{PE}}$ — (1)

$I_{PC} = \alpha I_{PE}$ — (2)

$I_E = I_{PE} + I_{NE}$ — (3)

$I_E \simeq I_{PE}$

$I_{PC} = \alpha I_E$

$I_C = I_{PC} + I_{PCO} + I_{NCO}$, let $I_{CO} = I_{PCO} + I_{NCO}$

$I_C = I_{PC} + I_{CO} \Rightarrow \boxed{I_C = \alpha I_E + I_{CO}}$ — (4)

$I_C = \alpha(I_B + I_C) + I_{CO} \Rightarrow I_C = \alpha I_B + \alpha I_C + I_{CO}$

$\Rightarrow I_C(1-\alpha) = \alpha I_B + I_{CO} \Rightarrow I_C = \alpha I_E + I_{CO} \Rightarrow \boxed{I_C = \alpha I_E + I_{CO}}$ — (5)

$\boxed{I_C = \beta I_B + (1+\beta) I_{CO}}$ — (6)

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II B.Tech I-Semester - Mid-II *Examinations*

Electronic Devices and Circuits

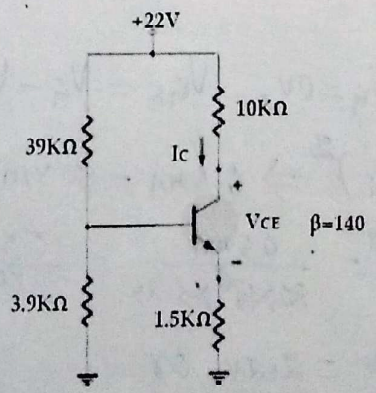
ECE

Max. Marks: 20 **Date: 14-02-2023** **Time: 2 Hours**

Note: 1. Answer first question compulsorily. (5 x 1 = 5 Marks)

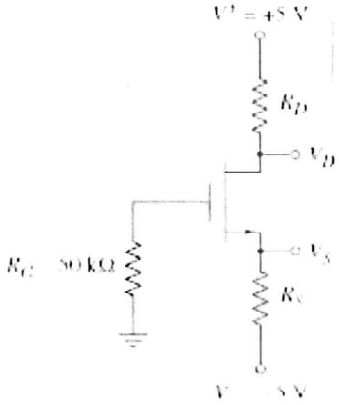
2. Answer Any *THREE* from 2 to 5 questions. (3 x 5 = 15 Marks)

Q.No			M	CO	BL
Q.1	a)	What is operating point? How to set Q-point.	1M	CO4	BL1
	b)	Define stability factors s and s||.	1M	CO4	BL1
	c)	Why FET is called unipolar device?	1M	CO2	BL2
	d)	Give any two differences between E-MOSFET and D-MOSFET.	1M	CO2	BL2
	e)	Draw the DC load line for MOSFET V-I characteristics	1M	CO4	BL2
Q.2	a)	Derive the stability factor **S** for Collector to Base bias circuit with emitter resistance	2M	CO4	BL2
	b)	For the voltage-divider configuration of Fig. Determine the i)dc bias voltage V_{CE} and ii) the current I_C	3M	CO4	BL3



Q.3	a)	Explain Diode compensation technique in detail and find the stability factor **S**.	3M	CO4	BL2
	b)	In an n-channel JFET, I_{DSS} = 20 mA and V_P = -6V. Calculate the drain current when V_{GS} = -3V	2M	CO2	BL4

Q.4	**a)**	Derive the following parameters of the JFET and relate them. i) g_m ii) r_d iii) μ	**3M**	CO2	BL2
	b)	Draw the Depletion mode NMOS physical structure and explain its working principle.	**2M**	CO2	BL2
Q.5	**a)**	Derive the current equation I_{DS} for MOSFET in three regions	**3M**	CO2	BL3
	b)	Design a MOSFET circuit biased with both positive and negative voltages to meet a set of specifications: The circuit configuration to be designed is shown in Figure. Design the circuit such that I_{DQ} = 0.5mA and V_{DSQ} = 4V. Choices: Standard resistors are to be used in the final design. A transistor with nominal parameters of k_n' = 80 μA/V², (W/L) = 6.25, and V_{TN} = 1.2V is available.	**2M**	CO4	BL4



5b) Given: $I_{DQ} = 0.5\,mA$, $V_{DSQ} = 4V$, $K_n' = 80\,\mu A/V^2$, $\frac{W}{L} = 6.25$

$V_{TN} = 1.2V$.

For above fig. $V_G = 0V$, $V_{GS} = V_G - V_S = 0 - V_S \Rightarrow \boxed{V_S = -V_{GS}}$

$i_D = K_n' \cdot \frac{W}{L}(V_{GS} - V_{TN})^2 \Rightarrow 0.5mA = 80\times10^{-6} \times 6.25\,(V_{GS} - 1.2V)^2$

$(V_{GS} - 1.2)^2 = \frac{0.5mA}{80\times10^{-6}\times6.25} = \frac{0.5\times10^{3}}{80\times6.25} \Rightarrow (V_{GS} - 1.2)^2 = 1$

$V_{GS} = 1 + 1.2 = 2.2V$ or

$V_S = -V_{GS} = -2.2V$

$R_S = \frac{V_S - (-5)}{I_D} = \frac{-2.2+5}{0.5mA} = \frac{2.8}{0.5mA} = 5.6K\Omega \Rightarrow \boxed{R_S = 5.6K\Omega}$

$V_{DSQ} = 4V$, $V_{DS} = V_D - V_S \Rightarrow 4 = V_D - (-2.2) = V_D + 2.2 \Rightarrow V_D = 4 - 2.2$

$\boxed{V_D = 1.8V}$

$R_D = \frac{V_{+} - V_D}{I_D} = \frac{5 - 1.8}{0.5mA} = 6.4K\Omega \Rightarrow \boxed{R_D = 6.4K\Omega}$

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

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NANDYAL – 518501

II B.TECH I-SEMESTER, MID-II EXAMINATIONS

ELECTRONIC DEVICES AND CIRCUITS (EDC)

ECE

Max. Marks: 20 Date: 14-02-2023 Time: 2 Hours

SCHEME OF EVALUATIONS

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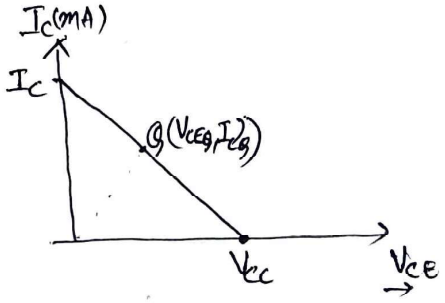
1 a) Operating point:

Operating point or quiescent point (Q-point) also known as a bias point, is a steady-state DC voltage or current at a specified terminal of an active device such as a diode or transistor with no input signal applied.

Setting Q-point:

The output characteristics show graph between I_C and V_{CE}. For setting or finding intersecting points of load line with x-axis and y-axis, take $I_C = 0$ and then $V_{CE} = 0$. So the value of point Q will be obtained as shown in Fig. (1)



$$V_{CC} = I_C R_C + V_{CE} \quad -(1)$$

If $I_C = 0$, $\boxed{V_{CE} = V_{CC}}$ $-(2)$

$V_{CE} = 0V$, $\boxed{I_C = \frac{V_{CC}}{R_C}}$ $-(3)$

b) Stability factor:

Stability factor, S, is defined as the ratio of change of collector current, I_C, with respect to the base leakage current, I_{CO}, keeping I_B and β constant, i.e $S = \frac{\partial I_C}{\partial I_{CO}} \simeq \frac{dI_C}{dI_{CO}}$ $-(1)$

then $S' = \frac{\partial I_C}{\partial V_{BE}} \simeq \frac{\Delta I_C}{\Delta V_{BE}}$ $-(2)$

$S'' = \frac{\partial I_C}{\partial \beta} \simeq \frac{\Delta I_C}{\Delta \beta}$ $-(3)$

c) FET is known as Unipolar device because the current flow through it is controlled by only a single type of charge carrier, either electrons or holes.

d) Two Differences between E-MOSFET and D-MOSFET:

E-MOSFET	D-MOSFET
i) There is no channel during its manufacturing.	i) The channel is fabricated during its manufacturing.
ii) In E-MOSFET, the channel is enhanced or induced using the gate voltage, but it does not conduct current when there is no gate voltage, V_{GS}.	ii) In D-MOSFET, the channel depletes with the gate voltage, but it conducts current when there is no gate voltage, V_{GS}.

e) DC load line for MOSFET V-I characteristics:

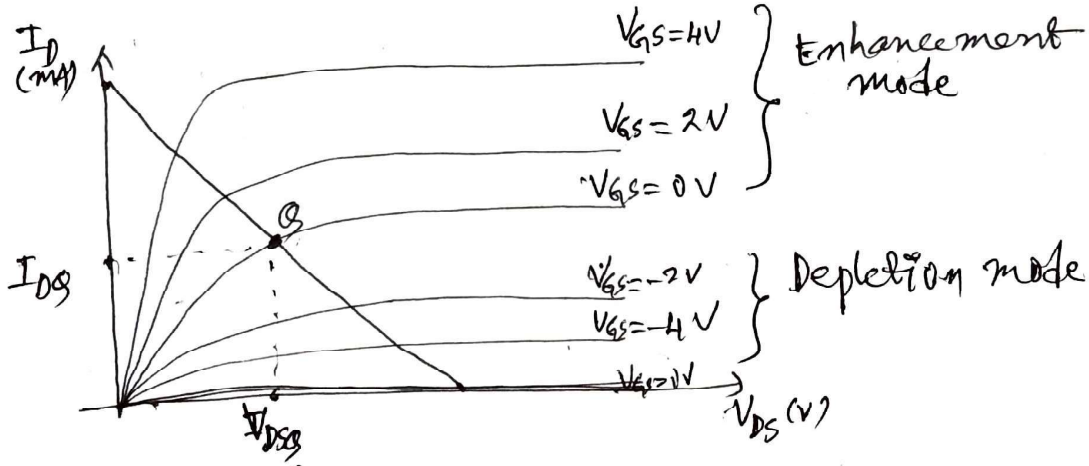


Fig 1: Load line for MOSFET

2a) Stability factor S for Collector to Base bias circuit with R_E:

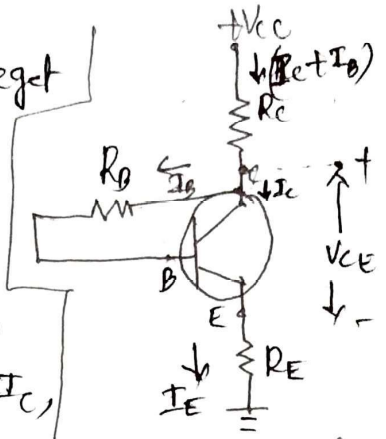


Fig.1: collect-to-base circuit

Applying KVL at i/p side loop, we get

$$V_{CC} - I_C R_C - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0 \quad -(1)$$

$$V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_B R_E - I_C R_E = 0 \quad -(2)$$

Differentiate above equation w.r.t I_C, we get

$$0 - R_C - \frac{dI_B}{dI_C} R_B - \frac{dI_B}{dI_C} R_E - R_E = 0$$

$$-(R_C + R_E) - \frac{dI_B}{dI_C}(R_B + R_E + R_C) = 0$$

$$\Rightarrow \frac{dI_B}{dI_C} = -\left(\frac{R_C + R_E}{R_B + R_E + R_C}\right) \quad -(3)$$

We have $$S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}} = \frac{1+\beta}{1+\beta\left[\frac{(R_C+R_E)}{(R_B+R_E+R_C)}\right]} \quad -(4)$$

b) Given $I_B = 6\mu A$, $I_C = 0.84mA$

$\beta = 140.1$

$$V_{Th} = \frac{R_2}{R_1+R_2} \cdot V_{CC} = \frac{3.9K}{39K+3.9K} \times 22 = 2V$$

$$R_{Th} = \frac{3.9K \times 39K}{39K+3.9K} = 3.54K\Omega$$

Apply KVL in i/p loop for Fig.1(b)

$$\Rightarrow V_{Th} - R_{Th} \cdot I_B - V_{BE} - I_E \cdot R_E = 0$$

$$2V - 3.54K \times 6\mu A - 0.6 - I_E \times 1.5K\Omega = 0$$

$$I_E = \frac{1.379}{1.5K\Omega} = 0.9mA$$

$I_E = I_B + I_C = (1+\beta) I_B$ or

$I_C = I_E - I_B = 0.9mA - 0.06mA = 0.859mA$

$V_{CE} = V_{CC} - I_C R_C = 22 - (0.859m \times 10K\Omega) = 13.41V$

$\boxed{I_C = 0.86mA}$ $\boxed{V_{CE} = 13.41V}$

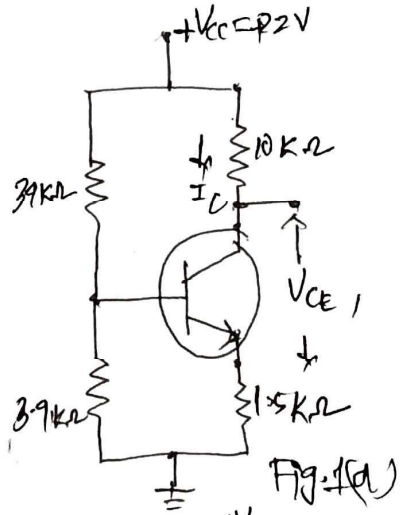


Fig.1(a)

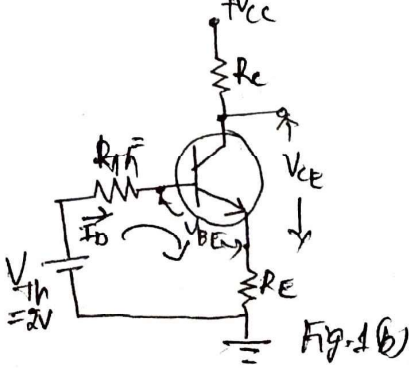


Fig.1(b)

3a) Diode Compensation technique:

→ The diode is of the same material as the transistor and it is reverse biased by the base-emitter junction, allowing the diode reverse saturation current into I to flow through the diode, D.

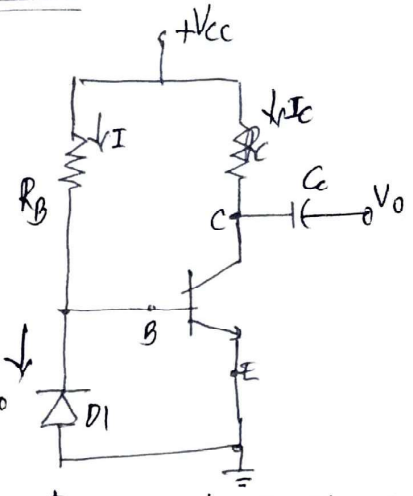


Fig 1: Diode compensation circuit

The base current $I_B = I - I_o$ and we have $I_C = \beta I_B + (1+\beta) I_{CO}$

$= \beta(I - I_o) + (1+\beta) I_{CO}$

$I_{CO} \simeq \beta I - \beta I_o + \beta I_{CO}$ $\quad [\because I_o = I_{CO}]$

$\boxed{I_{CO} \simeq \beta I}$ or $\boxed{I_B = I - I_o}$

This method does not need a change in I_C to effect the change in I_B, as both I_o and I_{CO} can track almost equally according to the change in temperature.

b) Given data: $I_{DSS} = 20mA$, $V_p = -6V$ & $V_{GS} = -3V$.

we have $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

$= 20mA\left(1 - \frac{(-3)}{(-6)}\right)^2$

$= 20mA\,(1/2)^2$

$= 20^5 mA \times \frac{1}{4_1} = 5mA$

$\boxed{I_D = 5mA}$

49) Parameters of JFET derivation:

(i) Transconductance, g_m:

According to Shockley's equation, $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$ — ①

Differentiating eqn ① w.r.t V_{GS}, we get

$$\frac{\partial I_{DS}}{\partial V_{GS}} = 2 I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right) \cdot \left(-\frac{1}{V_p}\right)$$

Transconductance, $g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = -\frac{2 I_{DSS}}{V_p}\left(1 - \frac{V_{GS}}{V_p}\right)$ — ②

When $V_{GS} = 0$, $g_m = \frac{-2 I_{DSS}}{V_p}$ — ③

Let $-\frac{2 I_{DSS}}{V_p} = g_{m0}$, So, $g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right)$ — ④

When $V_{GS} = V_p$, $g_m = g_{m0}\left(1 - \frac{V_p}{V_p}\right) = g_{m0}(1-1) = 0 \Rightarrow \boxed{g_m = 0}$ — ⑤

ii) Drain resistance, r_d:

It is the reciprocal of the slope of the drain characteristics and is defined by

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}\text{-constant}}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D}$$

(iii) Amplification factor, μ:

Amplification factor, μ, is defined as $\mu = -\left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)$

$$\mu = \frac{\partial V_{DS}}{\partial V_{GS}} = \frac{\partial V_{DS}}{\partial I_{DS}} \cdot \frac{\partial I_{DS}}{\partial V_{GS}} = r_d \cdot g_m$$

where r_d - drain resistance
g_m - transconductance

4b) N-MOSFET physical Structure:

Enhancement MOSFET is operated in enhancement mode only i.e current increases w.r.t Voltage.

Types:
i) N-channel enhancement MOSFET
ii) P-channel enhancement MOSFET

physical structure:

The transistor is fabricated on p-type substrate, which is single crystal silicon wafer that provides physical support for the device as shown in Fig 1.

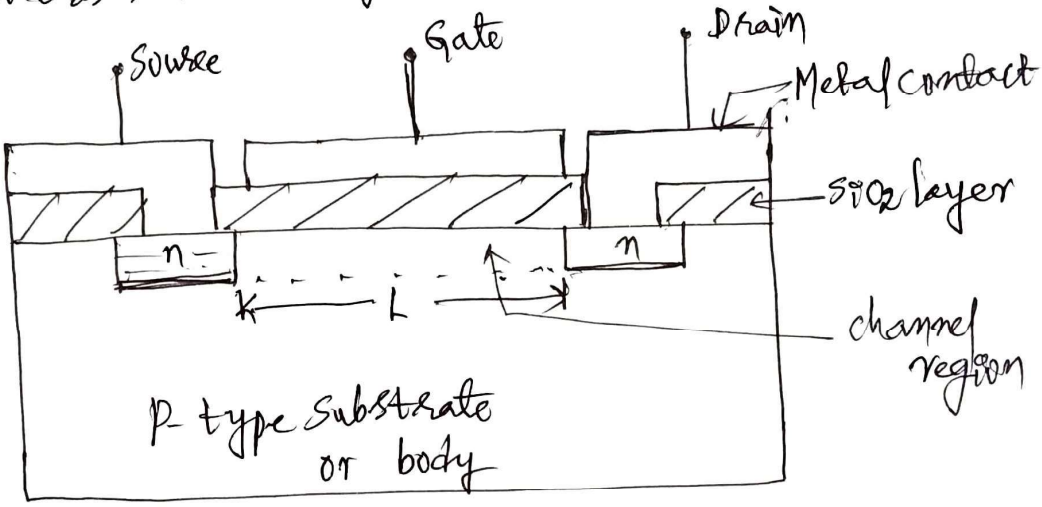


Fig 1: physical structure of NMOSFET

→ Two heavily doped n-type regions are created in the substrate to serve as the source (S) and drain (D).

→ A thin layer of silicon dioxide (SiO_2), which is an excellent electrical insulator, is grown on the surface of the silicon.

→ Metal is deposited on top of the oxide layer to form the "gate" contact of MOSFET. Metal contacts are also made for source and drain

→ Substrate is known as body. The name Metal oxide semiconductor FET is derived from its physical structure

→ The gate material is electrically insulated (or separated) from the device body by the oxide layer.

5a) Current equation I_{DS} for MOSFET derivation;

Since the charge induced is dependent on the gate to source voltage V_{gs} then I_{ds} depends on both V_{gs} and V_{ds}.

Current from Drain to source

$$I_{ds} = \frac{\text{Charge induced in channel (Qc)}}{\text{Electron transit time, (t)}} \quad -(1)$$

The factor $\frac{W}{L}$ is contributed by the geometry and it is common practice to write, $\beta = K\frac{W}{L}$ -(2)

So that $I_{ds} = K \cdot \frac{W}{L}\left[(V_{gs}-V_t) - \frac{V_{ds}}{2}\right]V_{ds}$ -(3)

$$I_{ds} = \beta\left[(V_{gs}-V_t) - \frac{V_{ds}}{2}\right]V_{ds} \quad -(4) \text{ for ohmic region.}$$

In Saturation region, $V_{ds} > V_{gs}-V_t$, in this condition effective channel length $L_{eff} = L-\Delta L$,

$$I_{ds} = \frac{1}{2}\beta(V_{gs}-V_t)^2(1+\lambda V_{ds}) \quad \text{where } \lambda = \frac{\Delta L/L}{V_{ds}} \quad -(5)$$

In pinch-off region, $V_{ds} = V_{gs}-V_t$, substitute this in equation, $I_{ds} = \beta\left[(V_{gs}-V_t) - \frac{V_{ds}}{2}\right]V_{ds}$

$$= \beta\left[(V_{gs}-V_t) - \frac{(V_{gs}-V_t)}{2}\right](V_{gs}-V_t)$$

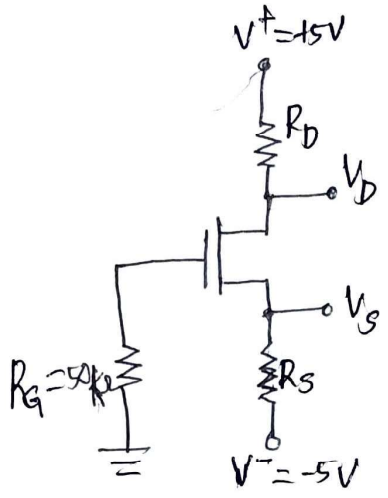
$$= \frac{\beta}{2}(V_{gs}-V_t)^2$$

$$\text{or } I_{ds} = \frac{K\cdot W}{2L}(V_{gs}-V_t)^2$$

$$\text{or } I_{ds} = \frac{1}{2}C_{ox}\cdot\mu_n\cdot\frac{W}{L}(V_{gs}-V_t)^2 \quad \text{where } \beta = C_{ox}\cdot\mu_n\cdot\frac{W}{L}.$$

5b) Given: $I_{DQ}=0.5\,mA$, $V_{DSQ}=4V$, $K_n'=80\mu A/V^2$, $\frac{W}{L}=6.25$, $\{V_{TN}=1.2V$

For given figure shown below



$V_G=0V$,

$V_{GS}=V_G-V_S=0-V_S \Rightarrow \boxed{V_S=-V_{GS}}$

we have,

$$i_D=K_n'\cdot\frac{W}{L}(V_{GS}-V_{TN})^2 \Rightarrow$$

$$0.5mA=80\times10^{-6}\times6.25\,(V_{GS}-1.2V)^2$$

$$(V_{GS}-1.2V)^2=\frac{0.5mA}{80\times10^{-6}\times6.25}=\frac{0.5\times10^3}{80\times6.25}\Rightarrow(V_{GS}-1.2)^2=1$$

$$V_{GS}=1+1.2=2.2V\ (or)$$

$$V_S=-V_{GS}=-2.2V$$

$$R_S=\frac{V_S-V^-}{I_D}=\frac{-2.2-(-5)}{0.5mA}=\frac{2.8}{0.5mA}=5.6K\Omega$$

$V_{DSQ}=4V$, $V_{DS}=V_D-V_S \Rightarrow 4=V_D-(-2.2)=V_D+2.2 \Rightarrow V_D=4-2.2=1.8V$

$\boxed{V_D=1.8V}$

$$R_D=\frac{V_1^+-V_D}{I_D}=\frac{5-1.8}{0.5mA}=6.4K\Omega \Rightarrow \boxed{R_D=6.4K\Omega}$$

R20

Code: A0403203R0223

RGM COLLEGE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS)

25th February 2023

II B.Tech. I Sem. (R20) End Examinations (Regular)

ELECTRONIC DEVICES AND CIRCUITS

ECE

22-23

Time: 3 Hrs **Total Marks: 70**

Note 1:Answer Question No.1 (Compulsory) and 4 from the remaining

2:All Questions Carry Equal Marks

1a Classify the different rectifiers. CO1

b Discuss about Zener break down mechanism. CO2

c Define input impedance. CO2

d When a reverse gate voltage is 12v is applied to JFET, the gate current is 1nA.determine the resistance between gate and source. CO3

e Mention the three regions that present in the drain source characteristics of JFET. CO1

f If a transistor, with α=0.96 and emitter current is 10mA, find the value of I_C CO4

g Define transformer utilization factor. CO1

2 a) With the help of a neat circuit diagram, input and output waveforms, describe the operation of a Half-wave rectifier. CO2 (7)

b) Derive an expression for ripple factor in a π-section filter when used with a full wave rectifier. CO3 (7)

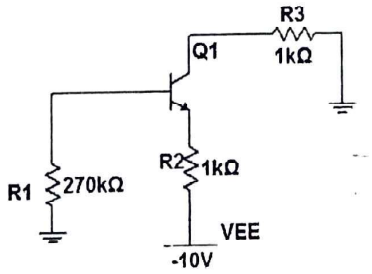
3 a) Explain Diode compensation technique in detail and find the stability factor S. CO3 (10)

b) Explain the role of R_E in biasing techniques. CO2 (4)

4 a) Draw the output V-I characteristics of CE configuration and mention the operating reasons in the diagram. CO3 (6)

b) For the circuit shown below, calculate I_B, V_C and V_{CE} where β = 100. (8)

CO6



5 a) A silicon diode has a saturation current of 7.5μA at room temperature 300⁰ K. Calculate the saturation current at 400⁰ K. CO4 (7)

b) Distinguish between Avalanche and Zener mechanisms. CO1 (7)

6 a) Compare JFET and BJT.Give the applications of FET CO3 (7)

b) Explain the construction and principle operation of Enhancement MOSFET. (7)

CO3

7 a) Explain the small signal JFET $i_D = f(V_{GS}, V_{DS})$ and define g_m, r_d and μ. (7)
b) An NMOS transistor with VTN = 1V has drain current ID = 0.8mA when VGS = 3V and VDS = 4.5V. Calculate the drain current when VGS = 2V and VDS = 4.5V. (7)

- xxx -

II B.Tech. I Sem. (R20) End Examinations 1/12
Regular

Code : A0403203RD.

Electronic Devices and Circuits

ECE

Total Marks: 70

SCheme of Evaluation

1a. Classify the different rectifiers.

Ans:- Rectifiers are used to convert bidirectional signal to unidirectional signal (or) AC to pulsating DC. — 1M

Rectifiers are classified as

1. Half wave Rectifier
2. Full wave Rectifier
   - with Center tapped
   - with Bridge ckt

— 1M

1b. Discuss about Zener breakdown mechanism.

Ans:- This breakdown is occur in the heavily dopped ($1:10^5$) PN junction diode. In heavily doped PN diodes, Concentration of charge carriers are very high and Junctio width is thin. Due to this direct rupture is taken plac between the charge carriers. potential is developed due to rupture b/n atoms, that potential is sufficient to break the covalent bonds, which resulting in more charge carrie are become free. — 1M

Major difference between avalanche breakdown and zener diode breakdown is, in avalanche breakdown, breakdown is due to secondary emission due to temperal generation. So avalanche breakdown damages the PN Junct In zener breakdown, breakdown is due to direct rupture So that temperature generation is very very less. —— 1M

1c. Define input impedance

Ans:- Input impedance is defined as ratio of input voltag to input current. It is calculated from the AC equivale. Circuit as the equivalent resistance looking into the input with all current source replaced by an open and all voltage source replaced by a short. —— 2M

1d. When a reverse gate voltage is 12V is applied to JFET, the gate current is 1nA. determine the resistance between gate and source.

Ans:- ~~Drain resistance / rd~~

Trance conductance

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \quad \text{—— 1M}$$

$$= \frac{1nA}{12V} = \frac{1nA}{12}$$

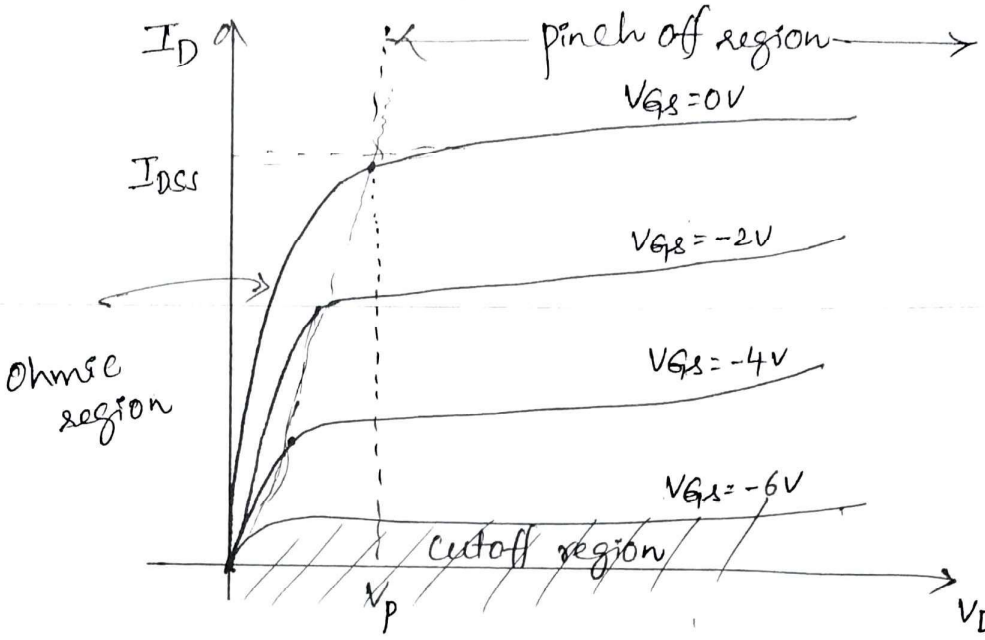
$\therefore$ resistance between gate and source $= \frac{1}{g_m}$

$$= \frac{12}{1n} = 12 \times 10^9$$

—— 1M

1e. Mention the three regions that present in the drain source characteristics of JFET.

Ans:-



2M

1f. If a transistor, with $\alpha = 0.96$ and emitter current is 10mA, find the value of I_C.

Ans:-

Given

$$I_E = 10mA$$

Current gain $\alpha = 0.96$

where $\alpha = \frac{I_C}{I_E}$ ——— 1M

$\therefore I_C = \alpha I_E = 0.96 \times 10mA$

$\therefore$ Collector current = I_C = 9.6mA ——— 1M

19. Define transformer utilization factor.

Ans:-

$$\text{Transformer utilization factor (TUF)} = \frac{P_{dc}}{V_{rms} \cdot I_{rms} \text{ of Se}}$$

—— 1M

For Example, for Halfwave Rectifier

$$P_{dc} = \frac{V_{dc}^2}{R_L} = \frac{\left(\frac{V_m}{\pi}\right)^2}{R_L}$$

V_{rms} of Secondary terminal is $= \frac{V_m}{\sqrt{2}}$

I_{rms} of Secondary terminal is $= \frac{I_m}{2}$

where $I_m = \frac{V_m}{R_L}$

I_{rms} of Secondary terminal is $= \frac{V_m}{2R_L}$

$$V_{rms} \times I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{V_m}{2R_L} = \frac{V_m^2}{2\sqrt{2}R_L}$$

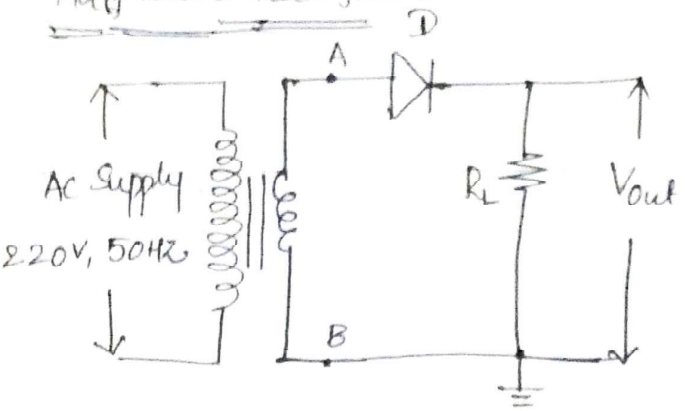
$$\therefore \text{TUF} = \frac{\left(\frac{V_m}{\pi}\right)^2 / R_L}{\frac{V_m^2}{2\sqrt{2}R_L}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

—— 1M

which indicates 28.7 % of Transformer energy or power is utilized for Half wave Rectification.

2 a) With the help of a neat Circuit diagram, input and o/p output waveforms, describe the operation of a Half wave rectifier.

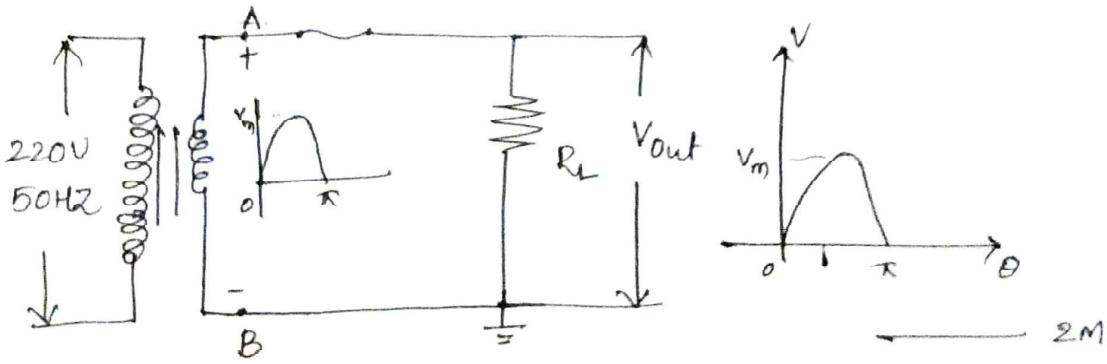
Ans:- **Half wave Rectifier :-**



2M

Operation :-

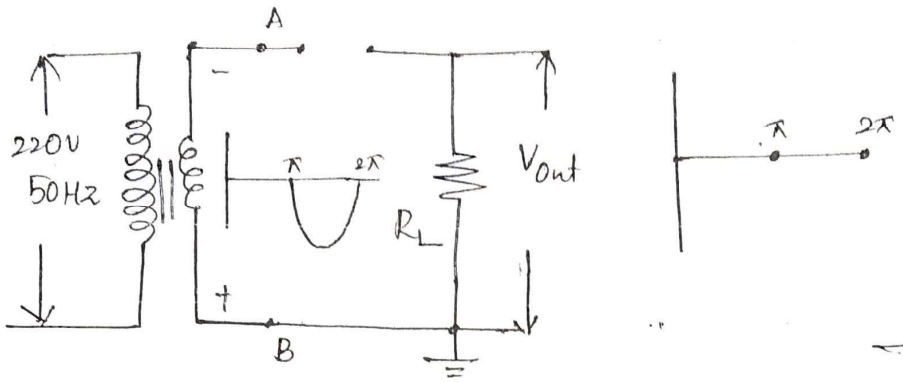
For positive cycle of input ac voltage, end "A" becomes +ve w.r.t "B", So that diode is operated in Forward bia i.e ideally it is treated as "ON" Switch. So it passes the entire positive cycle to load as shown in below Fig



2M

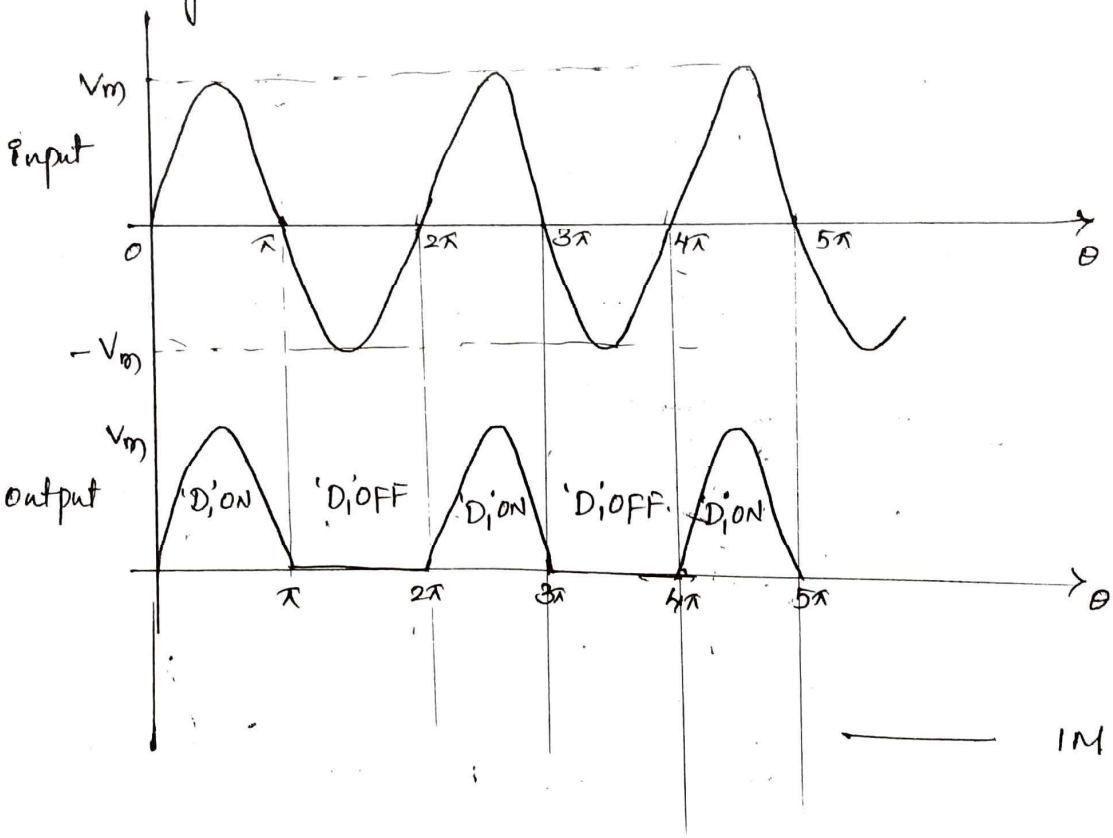
For Negative cycle, end A becomes -ve w.r.t B, So that diode is operated in reverse bias i.e ideally it is treated as "OFF" Switch. So that total voltage drop across the diode i.e no current flows through the R_L for

-ve Half cycle as shown in below Fig.



2M

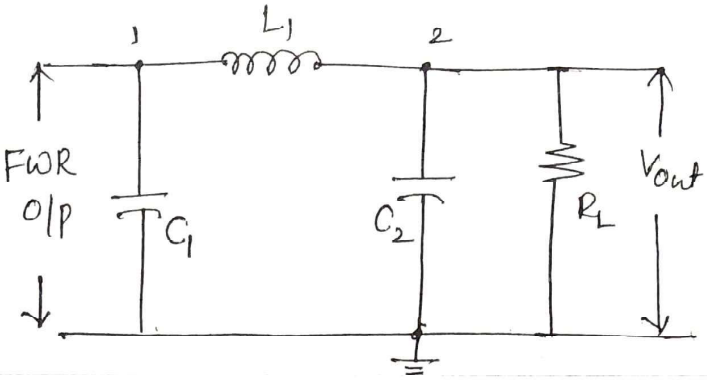
operation of the Half wave Rectifier is illustrated using following waveforms.



1M

2b) Derive an expression for ripple factor in π section filter when used with a Full wave rectifier.

Ans:- **π- Section Filter :-**



2M

FWR output contains both ac and dc component applied to i/p terminals of the filter. Here the filtering action of three components C_1, L_1, C_2 is discussed in below.

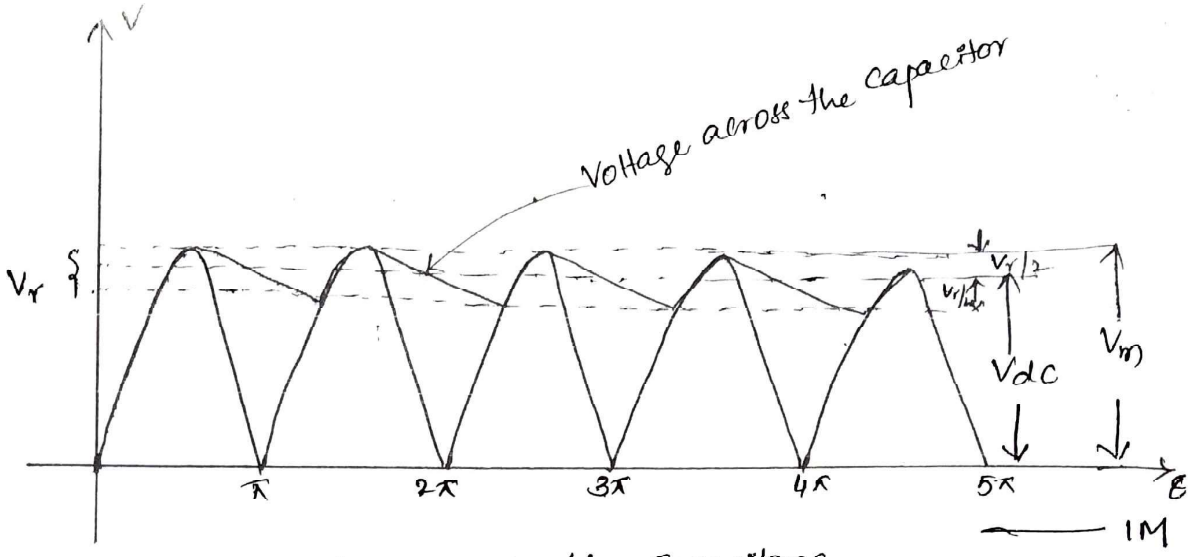
a) Capacitor "C_1" offers low reactance to ac component of FWR output, while it offers infinite reactance to the dc component of FWR output. Therefore Capacitor C_1 allows maximum ac component while the dc component move towards Inductor L.

b) The Inductor "L" offers high reactance to the dc compone Therefore, it allows the dc component, while the un by passe ac component is blocked.

c) The Capacitor C_2 by passes the ac component which the Inductor has failed to block. Therefore, only dc Component ~~approach~~ appears across the load and that is what we desire

1M

In π Section filter, Voltage appears across the capacitor C_1 terminal is approximately triangular wave is shown in Fig.



1M

Fig: Voltage across the capacitor C_2

Fourier Series of Triangular wave is given by

$$= \frac{V_r}{2} - \frac{V_r}{\pi} \sin 2\omega t$$

where $V_r = \frac{I_{dc}}{2fC_1}$

Magnitude of ac component is $\frac{V_r}{\pi} = \frac{I_{dc}}{2\pi fC_1}$

$$V_{ac\,rms}\ Value = \frac{\text{Magnitude of "ac" component}}{\sqrt{2}}$$

$$= \frac{V_r}{\sqrt{2}\pi}$$

$$= \frac{I_{dc}}{\sqrt{2}2\pi fC_1}$$ — 1M

$$V_{1ac\,rms} = \frac{I_{dc} \times 2}{\sqrt{2} \times 2\pi fC_1 \times 2}$$ multiply and divide by 2

$$V_{1ac\,rms} = \frac{I_{dc} \times 2}{\sqrt{2} \times 2\pi fC_1 \times 2}$$

$$V_{1ac\,rms} = \frac{2\,I_{dc}}{\sqrt{2}\ 2\omega C_1} = \sqrt{2}\, I_{dc} \times C_1 \longrightarrow (1)$$

From first loop of the filter

$$V_{1acrms} = I_{1acrms} \times Z$$

Where $Z = \sqrt{X_{L_1}^2 + X_{C_2}^2}$

for ac component X_{C_2} is negligible

$\therefore Z = X_{L_1}$

$$V_{1acrms} = I_{1acrms} \cdot X_{L_1}$$

$$\therefore I_{1acrms} = \frac{V_{1acrms}}{X_{L_1}} \longrightarrow (2)$$

And Voltage across the C_2 i.e at node 2 is

$$V_{2acrms} = I_{1acrms} \times X_{C_2} \longrightarrow (3)$$

Sub eqn(2) in eqn(3)

$$V_{2acrms} = \frac{V_{1acrms} \cdot X_{C_2}}{X_{L_1}} \longrightarrow (4)$$

Sub eqn(1) in eqn(4)

$$\therefore V_{2acrms} = \frac{\sqrt{2}\, I_{dc}\, X_{C_1} X_{C_2}}{X_{L_1}}$$

Where $I_{dc} = \frac{V_{dc}}{R_L}$

$$\therefore V_{2acrms} = \frac{\sqrt{2} \cdot V_{dc}\, X_{C_1} X_{C_2}}{R_L\, X_{L_1}}$$

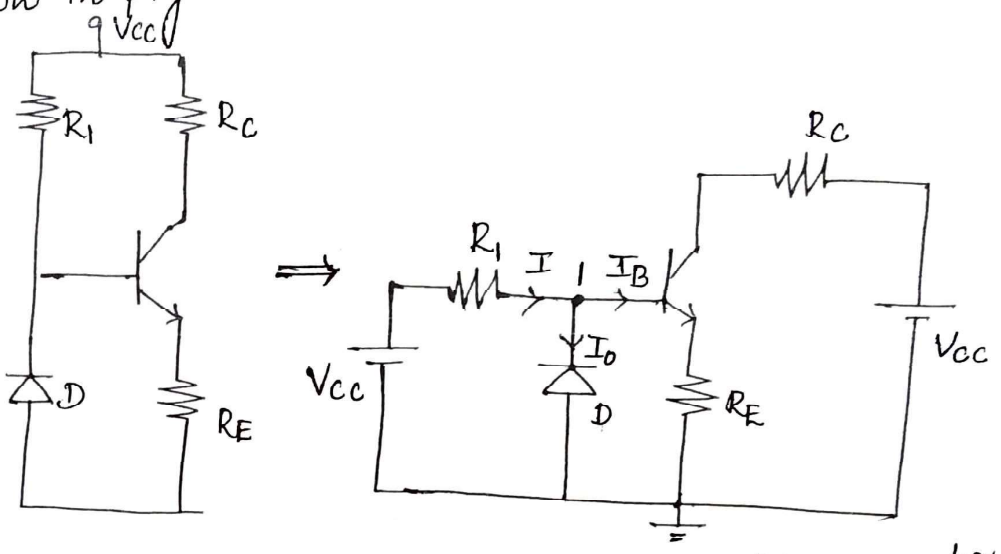
$$\therefore \text{Ripple factor} = \frac{V_{2acrms}}{V_{dc}} = \frac{\sqrt{2}}{R_L} \frac{X_{C_1} X_{C_2}}{X_{L_1}}$$

2M

3a) Explain Diode Compensation technique in detail and find the Stability factor S.

Ans:- **Diode Compensation technique:-**

In Self biasing circuit, R_2 is replaced with diode as shown in Fig.



4M

In above Circuit, diode operating in reverse bias so it allows I_o.

according KCL at node 'i'.

$$I = I_o + I_B$$

Base Current $I_B = I - I_o \longrightarrow (1)$ ——— 1M

From Current equation of BJT

$$I_C = \beta I_B + (1+\beta) I_{Co} \longrightarrow (2)$$

Compare β, '1' is neglected

$$\therefore I_C \simeq \beta I_B + \beta I_{Co} \longrightarrow (3)$$ ——— 1M.

Sub equ(1) in equ(3)

$$\therefore \quad I_C = \beta(I - I_0) + \beta I_{CO}$$

$$= \beta I - \beta I_0 + \beta I_{CO}$$

$$= \beta I + \beta(I_{CO} - I_0) \longrightarrow (4) \qquad \text{—— 1M}$$

Where I_{CO} is the reverse Saturation current of transistor

I_0 is the reverse Saturation current of diode.

If diode and Transistor are made with same material I_{CO} and I_0 are equal, so when temp ↑ both I_{CO} & I_0 are get double for every 10°C rise.

In eqn (4), effect of temperature on I_0 and I_{CO} get cancelled.

$$\therefore \quad I_C = \beta I \qquad \text{—— 1M}$$

So Stability factor $\frac{\partial I_C}{\partial I_{CO}} = 0$ ∴ Stability of the device is Very large. —— 2M

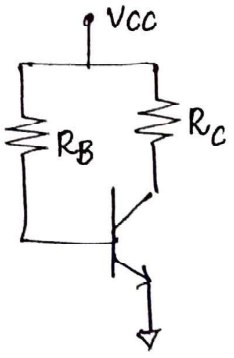
3b) Explain the role of R_E in biasing techniques.

Ans:

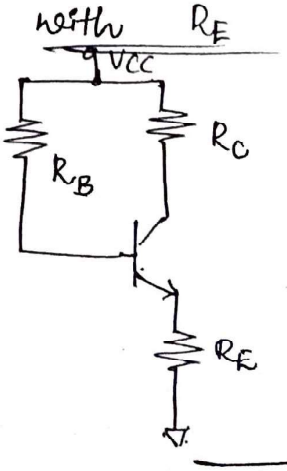
without R_E

Example

Fixed Bias



with R_E



—— 1M

Input KVL

$-V_{CC} + I_B R_B + V_{BE} = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow (1)$$

* without R_E

I_B is ~~large~~ High

Hence I_C also High

So Gain $\frac{I_C}{I_B}$ also High

from equ(1)

$$\frac{\partial I_B}{\partial I_C} = 0$$

$\therefore$ Stability factor $S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$

$= 1+\beta$

*: Stability is poor

Input KVL

$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$

where $I_E = I_B + I_C$

$-V_{CC} + I_B R_B + V_{BE} + (I_B + I_C) R_E = 0$

$-V_{CC} + I_B R_B + V_{BE} + I_B R_E + I_C R_E = 0$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E} \rightarrow (1)$$

* with R_E

I_B is LOW

Hence I_C also LOW

So Gain $\frac{I_C}{I_B}$ is low ~~→ 1~~

from equ(1)

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$$

$\therefore$ Stability factor

$$S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$$

$$= \frac{1+\beta}{1+\beta \cdot \frac{R_E}{R_B + R_E}}$$

if $R_E >> R_B$

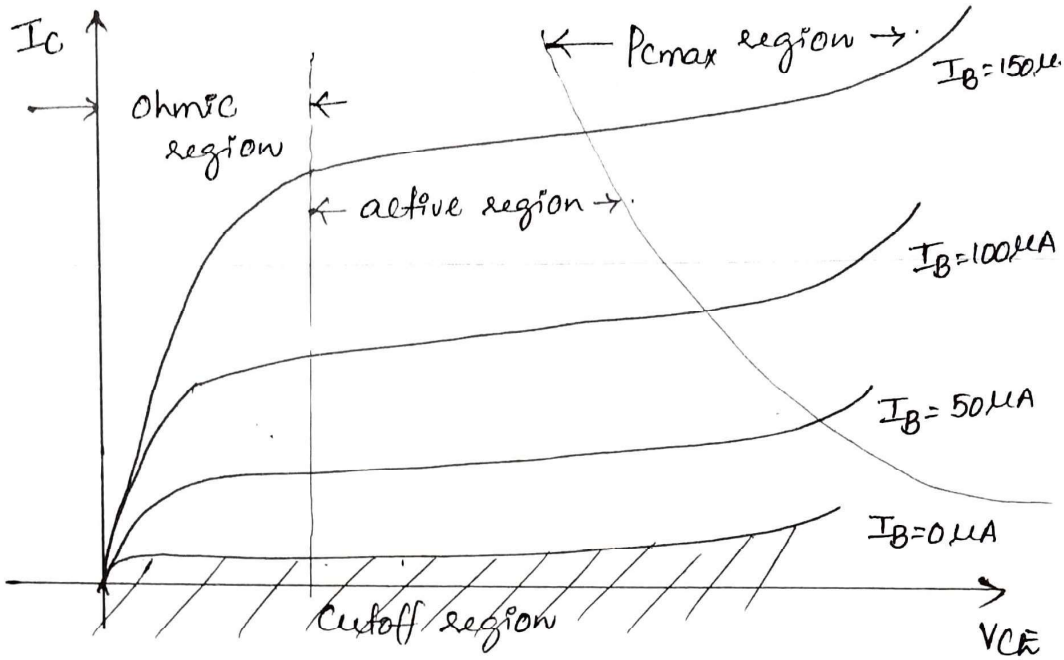
$R_B + R_E \simeq R_E$

$$\therefore S \simeq \frac{1+\beta}{1+\beta \frac{R_E}{R_E}} = 1$$

*: Stability is High

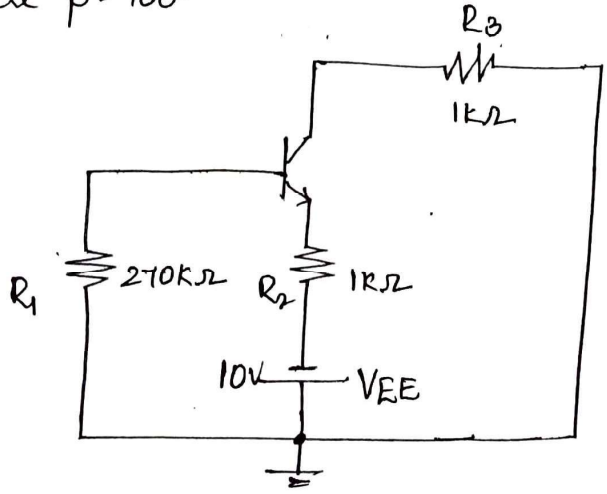
4a) Draw the Output V-I Characteristics of CE Configuration and mention the Operating regions on the diagram. 7/12

Ans:-



6M

4b) For the circuit shown below, Calculate I_B, V_C and V_{CE} where $\beta = 100$.



~~$I_B = 1/10 - V_{BE}$~~

Input KVL

$$-V_{EE} + I_B R_1 + V_{BE} + I_E R_2 = 0$$

where $I_E = \gamma I_B$

where $\gamma = (1+\beta) I_B$

$$-V_{EE} + I_B R_1 + V_{BE} + (1+\beta) I_B \cdot R_2 = 0$$

$$I_B (R_1 + (1+\beta) R_2) = V_{EE} - V_{BE}$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_1 + (1+\beta) R_2}$$

$$= \frac{10 - 0.7}{(270 + (101)1)\,K}$$

$$I_B = \frac{9.3}{371\,K} = 0.025\,mA$$

$$= 25\,\mu A \quad \text{—— 4M}$$

O/p KVL

$$-V_{EE} + I_C R_3 + V_{CE} + I_E R_2 = 0 \qquad I_E \simeq I_C$$

$$-10 + 2.5\times10^{-3} \times 1\times10^{3} + V_{CE} + 2.5\times10^{-3} \times 1\times10^{3} = 0$$

$$V_{CE} = 10 - 5$$

$$V_{CE} = \underline{5V}$$

O/p KVL

$$-V_{EE} + I_C R_3 + V_C = 0$$

$$V_C = V_{EE} - I_C R_3$$

$$= 10 - 2.5$$

$$V_C = 7.5V$$ ——— 4M

5a) A Silicon diode has a Saturation current of 7.5μA at room temperature 300°K. Calculate the Saturation current at 400°K.

Ans:- 300°K = 27°C formula is 300°K - 273°K

400°K = 127°C. ——— 1M

Let I_{CO1} = 7.5μA at 300°K or at 27°C.

I_{CO2} = ?

$$I_{CO2} = I_{CO1} \times 2^{(T_2 - T_1)/10}$$ ——— 2M

$$I_{CO2} = I_{CO1} \times 2^{(127-27)/10}$$

$$= 7.5 \times 10^{-6} \times 2^{100/10}$$

$$= 7.5 \times 10^{-6} \times 1024$$

$$= 7680 \times 10^{-6}$$

$$I_{CO2} = 7.68mA$$ ——— 4M

5b) Distinguish between Avalanche and Zener mechanisms.

Ans:-

Avalanche Breakdown Mechanism:-

This avalanche breakdown is occured in lightly (1:10^8) doped diode. For lightly dopped pn diode, transistion region (or) junction is thick. In such diodes, for reverse bias (>50V), the breakdown is through process of avalanche multiplication. ——— 1M

When reverse potential increases, generation of free carriers are high, on that condition temperature is generate due to collisions, that temperature able to break the covalant bonds, hence some more charge carriers are becomes free, this process is cummulative in nature. This cummulative process is known as "Avalanche multiplication".

Avalanche breakdown occured at higher voltages normally at 50V. ——— 2M

Zener Breakdown Mechanism:-

This break down is occur in the heavily dopped (1:10^5) pn junction diodes. In heavily dopped pn junct diodes, concentration of charge carriers are very high and junction width is thin. Due to this, direct rapture is taken place between the charge carriers. rapture between the charge carriers will produce the electric field, that

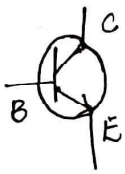
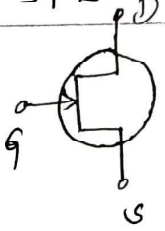
electric field break the covalent bonds, which results in further rise in concentration of charge carriers. — 2M

9/12

Major diff between avalanche breakdown and zener breakdown is, in avalanche breakdown, breakdown is due to secondary emission due to temperature generation. So avala breakdown damages the pN junction. In zener breakdown, breakdown is due to direct rupture. So that temp generation is very very less. — 2M

6a) Compare JFET and BJT. Give the applications of FET.

Ans:

Parameter	BJT	JFET
• Symbol		
• Definition	BJT is known as Bipolar Junction device because it use both electrons and holes for condection	JFET is known as unipolar device because current is due to one type of Charge carriers i.e either electrons or Holes.
• Biasing used	Fixed Bias, Collector Base Bias, voltage divider Bias	Self Bias, Voltage divider Bias
• Operating region	Active, Saturation, Cutoff region	Ohmic and Pinchoff region

• Thermal run away	Thermal runaway occurs at High temperature	No Thermal runaway
• Type of Device	Current Controlled device	Voltage Controlled device.
• Terminals	Emitter, Base, Collector	Gate, Source, Drain
• Input current	Input current is in order of either mA or μA	Gate current is order of nA.
• Applications	Low current application	Low Voltage applicat

—— 5M

Applications of JFET :-

JFETs are used in

1) High power switching applications
2) Voltage Variable Resistor (VVR)
3) Tone controls etc., for Mixer operation on FM and TV receivers
4) In Logic circuits.
5) As a amplifiers.
6) As a oscillator
7) Chopper and current limitter

—— 2M

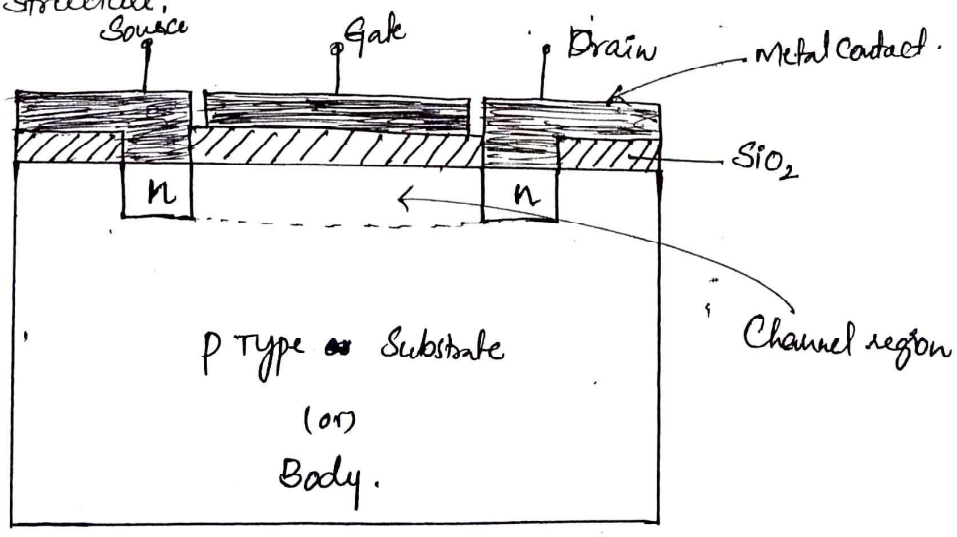
10/12

6b) Explain the Construction and Principle Operation of Enhancement MOSFET.

Ans:- **Physical Structure of Enhancement MOSFET :-**
(N- Channel Enhancement MOSFET)

The transistor is fabricated on p-type substrate, which is single crystal silicon wafer that provides physical support for the device. Two heavily doped n-type regions are created in the substrate to serve as the source and Drain. A thin layer of silicon dioxide (SiO_2) which is an excellent electrical insulator, is grown on the surface of the silicon, covering the area between source and Drain regions. Metal is deposited on top of the oxide layer to form the "Gate" contact of MOSFET. Metal contacts are also made for source and Drain. Substrate is known as Body. The name metal oxide semiconductor FET is derived from its physical structure.

— 2 M



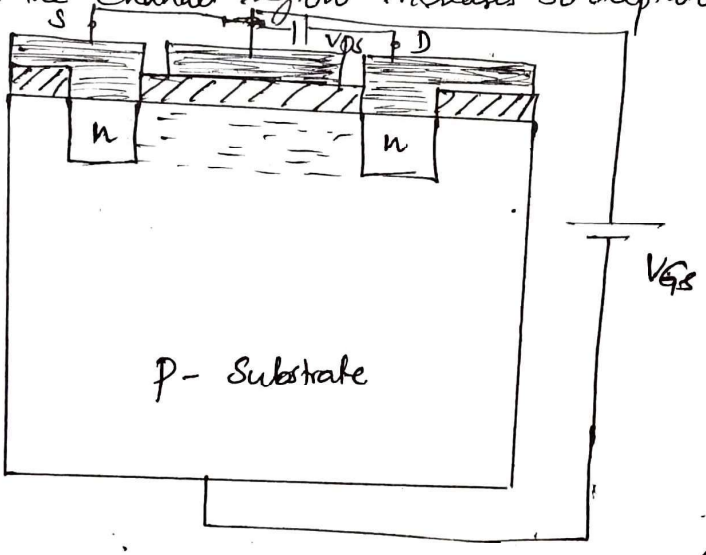
— 1M

Operation of Enhancement n-Channel MOSFET :-

When Gate is more +ve than p-type Substrate :

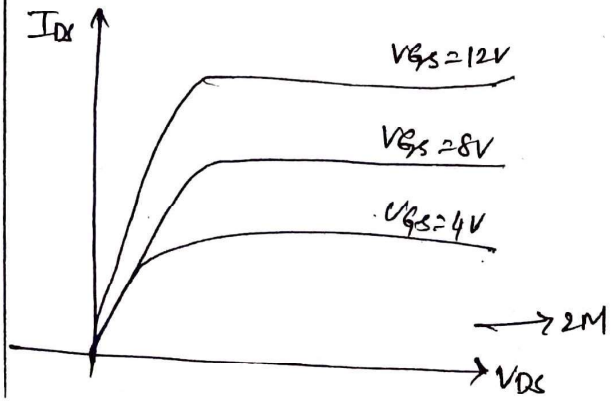
In p-type Substrate majority carriers are holes and minority carriers are electrons. So holes are repelled by the +ve potential, hence holes are move downwards. Electrons are attracted towards Gate terminals, So negative charge carriers are fill the region between Source and Drain regions i.e Channel region.

The negative carriers provides a Conduction Channel between the Source and the Drain. When magnitude of V_{GS} increases carrier in the Channel region increases So depth of Channel is increases.

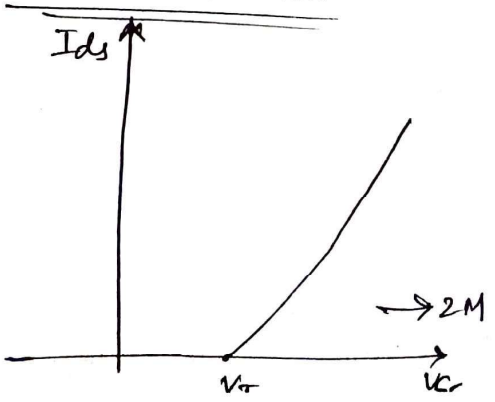


Now if a +ve potential is applied to Drain w.r.t Source. Then electrons in the Channel region are attracted towards +ve potential. current direction is opposite to electron flow so that current direction is drain to Source.

Drain Characteristics



Transfer Characteristics



7a) Explain the Small Signal JFET $i_D = f(V_{GS}, V_{DS})$ and define g_m, r_d and μ. 11/12

Ans:-

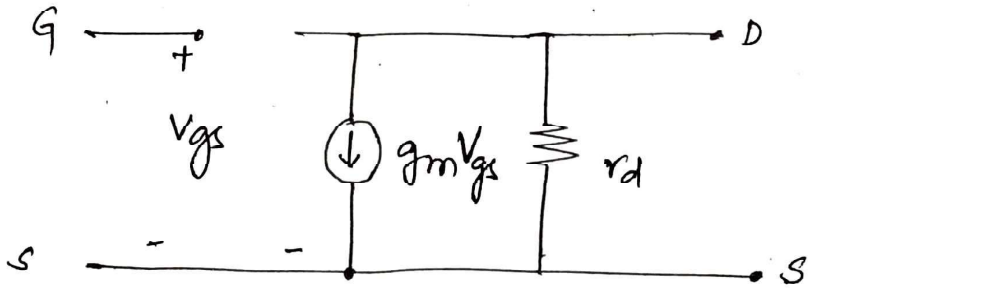
FET Small Signal model :-

$$i_D = f(V_{GS}, V_{DS})$$

$$\Delta i_D = \frac{\partial i_D}{\partial V_{GS}} \Delta V_{GS} + \frac{\partial i_D}{\partial V_{DS}} \cdot \Delta V_{DS}$$

where $\frac{\partial i_D}{\partial V_{GS}} = g_m$; $\frac{\partial i_D}{\partial V_{DS}} = \frac{1}{r_d}$.

$$\Delta i_D = g_m \Delta V_{GS} + \frac{1}{r_d} \cdot \Delta V_{DS} \quad \text{——} \quad 1M$$



—— 2M

Define g_m, r_d and μ :-

Drain resistance $r_d = \frac{V_{DS}}{I_{DS}} = \frac{L}{N_D q \mu 2b \cdot w}$

where $b = a\left[1 - \left\{\frac{V_{GS}}{V_p}\right\}^{1/2}\right]$

$\therefore$ $r_d = \frac{L}{2 N_D q \mu a \left[1 - \left\{\frac{V_{GS}}{V_p}\right\}^{1/2}\right] w}$

When $V_{GS} = 0$

$r_{d(ON)} = \dfrac{L}{2N_D q \mu a W}$ is called as Drain ON resistance and denoted as $r_{d(ON)}$

$\therefore$ Drain resistance $r_d = \dfrac{r_{d(ON)}}{\left[1 - \left\{\dfrac{V_{GS}}{V_p}\right\}^{1/2}\right]}$

When $V_{GS} = V_p$

Drain resistance $r_d = \infty$ ——— 2M

Trance conductance g_m :-

Shockley equation is given by $I_{DS} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_p}\right)^2$ ⟶(1)

equation (1) is differentiate w.r.t V_{GS}

$$\frac{\partial I_{DS}}{\partial V_{GS}} = 2I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)\left(\frac{-1}{V_p}\right)$$

Trance conductance $g_m = \dfrac{\partial I_{DS}}{\partial V_{GS}} = \dfrac{-2I_{DSS}}{V_p}\left(1 - \dfrac{V_{GS}}{V_p}\right)$ ⟶(2)

When $V_{GS} = 0$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2I_{DSS}}{V_p}$$

Let $\dfrac{-2I_{DSS}}{V_p}$ as g_{mo} so $g_{mo} = \dfrac{-2I_{DSS}}{V_p}$

$\therefore$ Trance conductance $g_m = g_{mo}\left(1 - \dfrac{V_{GS}}{V_p}\right)$

When $V_{GS} = V_p$

Trance conductance $g_m = g_{mo}\left(1 - \dfrac{V_p}{V_p}\right)$

$g_m = g_{mo}(1-1)$ ⟶ 2M

$g_m = 0$

Amplification factor μ :-

Amplification factor μ = $\frac{\text{Change in } V_{DS}}{\text{Change in } V_{GS}}$

i.e $\mu = \frac{\partial V_{DS}}{\partial V_{GS}}$

$= \frac{\partial V_{DS}}{\partial I_{DS}} \times \frac{\partial I_{DS}}{\partial V_{GS}}$

$\therefore$ Amplification factor $= \mu = r_d \times g_m$ —— 1M

7b) An NMOS transistor with $V_{TN} = 1V$ has drain current $I_D = 0.8mA$ when $V_{GS} = 3V$ and $V_{DS} = 4.5V$. Calculate the Drain current when $V_{GS} = 2V$ and $V_{DS} = 4.5V$.

Ans:-

Given data

$i_D = 0.8mA$

$V_{GS} = 3V$

$V_{DS} = 4.5V$

$V_{TN} = 1V$ —— 1M

For given data, NMOS operating in "Saturation region"

because $V_{DS} > V_{GS} - V_{TN}$ i.e $4.5V > 3V - 1V$

$4.5V > 2V$ —— 1M

$\therefore$ Current equation in NMOS for Saturation region is

$i_D = \frac{\beta}{2}(V_{GS} - V_{TN})^2$ Where $\beta = \frac{k\epsilon_0}{L}$

Let $\frac{\beta}{2}$ as K

$i_D = K(V_{GS} - V_{TN})^2$

CO- PO Attainment Process(Model Calculations)

Academic Year 2022-23
Regulations R20
Year II Sem I
Batch 21
Branch ECE
Subject(Code) EDC
Name of the Faculty M.A. VIJAY KAMALNATH/Dr.M.CHENNAKESAVULU/Dr. SATHISH

Note:Work out for all the subjects of 2021-22 (I-year to IV year)

External Question Paper Marks --> Cos

Q.No.	CO 1	CO 2	CO 3	CO 4			Total
1 a)	2						2
b)		2					2
c)	2						2
d)			2				2
e)		2					2
f)			2				2
g)	2						2
2 a)				7			7
b)				7			7
c)							0
3 a)	10						10
b)		4					4
c)							0
4 a)		6					6
b)			8				8
c)							0
5 a)				7			7
b)	7						7
c)							0
6 a)		7					7
b)				7			7
c)							0
7 a)			7				7
b)			7				7
c)							0
Total	23	21	26	28			98

Mid I Marks --> Cos

Q.No.	CO 1	CO 2	CO 3	CO 4			Total
1 a)	1						1
b)			1				1
c)		1					1
d)	1						1
e)			1				1
2 a)	3						3
b)				2			2
3 a)			3				3
b)							0
4 a)							0
b)		2					2
5 a)			3				3
b)			2				2
Total	5	3	10	2			20

Total	10	7	14	9			40

Mid II Marks --> Cos

Q.No.	CO 1	CO 2	CO 3	CO 4			Total
1 a)	1						1
b)		1					1
c)			1				1
d)				1			1
e)							0
2 a)	2						2
b)				3			3
3 a)		3					3
b)							0
4 a)			3	1			4
b)				2			2
5 a)							0
b)	2						2
Total	5	4	4	7			20

Assignment 1 Marks --> Cos

	CO 1	CO2	CO3	CO4			Total
	3	2	3	2			10
Total	3	2	3	2			10

Total	5	5	6	4			20
Total	5	5	6	4			20

Assignment 2 Marks --> Cos

	CO1	CO2	CO3	CO4			Total
	2	3	3	2			10
Total	2	3	3	2			10

S.No	Reg.No.	Internal marks	Assignment marks	Final Internal marks	Total Final Marks
1	21091A0401	6	10	16	31
2	21091A0402	15	10	25	78
3	21091A0403	6	10	16	32
4	21091A0404	13	10	23	66
5	21091A0405	7	10	17	61
6	21091A0406	18	10	28	76
7	21091A0407	19	10	29	92
8	21091A0408	16	10	26	69
9	21091A0409	17	10	27	88
10	21091A0410	14	10	24	57
11	21091A0411	19	10	29	93
12	21091A0412	7	10	17	59
13	21091A0413	4	10	14	15
14	21091A0414	4	10	14	16
15	21091A0415	9	10	19	60
16	21091A0416	16	10	26	75
17	21091A0417	15	10	25	80
18	21091A0418	17	10	27	84
19	21091A0419	8	10	18	48
20	21091A0420	13	10	23	79
21	21091A0421	15	10	25	79
22	21091A0422	14	10	24	77
23	21091A0423	16	10	26	87
24	21091A0424	17	10	27	93
25	21091A0426	8	10	18	52
26	21091A0427	10	10	20	70
27	21091A0428	11	10	21	65
28	21091A0429	18	10	28	84
29	21091A0430	11	10	21	62
30	21091A0431	8	10	18	64
31	21091A0432	9	10	19	55
32	21091A0433	5	10	15	32
33	21091A0434	8	10	18	67
34	21091A0435	17	10	27	90
35	21091A0436	6	10	16	50
36	21091A0437	6	10	16	33
37	21091A0438	7	10	17	24
38	21091A0439	13	10	23	61
39	21091A0440	18	10	28	89
40	21091A0441	10	10	20	60
41	21091A0442	19	10	29	77
42	21091A0443	8	10	18	46
43	21091A0444	5	10	15	28
44	21091A0445	11	10	21	49
45	21091A0446	8	10	18	44
46	21091A0447	18	10	28	93
47	21091A0448	18	10	28	83
48	21091A0449	19	10	29	86
49	21091A0450	6	10	16	34
50	21091A0451	12	10	22	67
51	21091A0452	15	10	25	71
52	21091A0453	12	10	22	60
53	21091A0454	15	10	25	73
54	21091A0455	14	10	24	76
55	21091A0456	11	10	21	64
56	21091A0457	7	10	17	46
57	21091A0458	11	10	21	62
58	21091A0459	11	10	21	66
59	21091A0460	19	10	29	88
60	21091A0461	18	10	28	88
61	21091A0462	15	10	25	73
62	21091A0463	19	10	29	97
63	21091A0464	5	10	15	28
64	2209SA0402	18	10	28	77
65	2209SA0403	13	10	23	84
66	2209SA0404	16	10	26	80
67	2209SA0406	19	10	29	86
68	2209SA0410	18	10	28	82
69	2209SA0416	14	10	24	69
70	2209SA0420	18	10	28	80
71	2209SA0424	8	10	18	54
72	2209SA0427	13	10	23	64
73	2209SA0433	13	10	23	65
74	21091A0465	13	10	23	66
75	21091A0466	4	10	14	48
76	21091A0467	7	10	17	53
77	21091A0468	2	10	12	20
78	21091A0469	6	10	16	59
79	21091A0470	13	10	23	71
80	21091A0471	3	10	13	28
81	21091A0472	5	10	15	31
82	21091A0473	14	10	24	76
83	21091A0474	2	10	12	22

External Marks
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% of IM	% of AM	% of EM
30	100	21.42857
75	100	75.71429
30	100	22.85714
65	100	61.42857
35	100	62.85714
90	100	68.57143
95	100	90
80	100	61.42857
85	100	87.14286
70	100	47.14286
95	100	91.42857
35	100	60
20	100	1.428571
20	100	2.857143
45	100	58.57143
80	100	70
75	100	78.57143
85	100	81.42857
40	100	42.85714
65	100	80
75	100	77.14286
70	100	75.71429
80	100	87.14286
85	100	94.28571
40	100	48.57143
50	100	71.42857
55	100	62.85714
90	100	80
55	100	58.57143
40	100	65.71429
45	100	51.42857
25	100	24.28571
40	100	70
85	100	90
30	100	48.57143
30	100	24.28571
35	100	10
65	100	54.28571
90	100	87.14286
50	100	57.14286
95	100	68.57143
40	100	40
25	100	18.57143
55	100	40
40	100	37.14286
90	100	92.85714
90	100	78.57143
95	100	81.42857
30	100	25.71429
60	100	64.28571
75	100	65.71429
60	100	54.28571
75	100	68.57143
70	100	74.28571
55	100	61.42857
35	100	41.42857
55	100	58.57143
55	100	64.28571
95	100	84.28571
90	100	85.71429
75	100	68.57143
95	100	97.14286
25	100	18.57143
90	100	70
65	100	87.14286
80	100	77.14286
95	100	81.42857
90	100	77.14286
70	100	64.28571
90	100	74.28571
40	100	51.42857
65	100	58.57143
65	100	60
65	100	61.42857
20	100	48.57143
35	100	51.42857
10	100	11.42857
30	100	61.42857
65	100	68.57143
15	100	21.42857
25	100	22.85714
70	100	74.28571
10	100	14.28571

N CO 1	N CO 2	N CO 3	N CO 4		
31.42857	32.21088	31.77857	28.81402		
78.10235	78.48639	78.08929	77.42588		
32.40938	33.23129	32.70714	29.89218		
66.20469	66.61565	66.35357	64.94609		
60.91684	62.63605	59.93214	60.92992		
76.33262	75.88435	77.12143	74.58221		
92.08955	92.02381	92.275	91.60377		
69.33902	69.11565	70.02857	67.49326		
88.03838	88.31633	87.96786	87.74933		
57.44136	57.2449	58.29286	55.01348		
93.07036	93.04422	93.20357	92.68194		
58.95522	60.59524	58.075	58.77358		
15.60768	16.2585	16.32857	12.02156		
16.58849	17.27891	17.25714	13.09973		
60.06397	61.2415	59.59643	59.39353		
75.22388	75.2381	75.6	73.96226		
80.06397	80.52721	79.94643	79.58221		
84.11514	84.23469	84.25357	83.43666		
48.23028	49.18367	48.15714	46.68464		
78.95522	79.88095	78.425	78.96226		
79.08316	79.5068	79.01786	78.50404		
77.05757	77.65306	76.86429	76.57682		
86.9936	87.48299	86.74286	86.90027		
92.94243	93.41837	92.61071	93.14016		
52.15352	53.26531	51.87143	50.9973		
69.93603	71.2585	69.17857	69.94609		
65.09595	65.96939	64.83214	64.32615		
84.1791	84.04762	84.55	83.20755		
62.15352	62.90816	62.04643	61.09164		
63.92324	65.5102	63.01429	63.93531		
55.15991	56.13946	54.95357	54.0027		
32.34542	33.41837	32.41071	30.12129		
66.86567	68.57143	65.8	67.16981		
90	90.35714	89.825	89.90566		
50.06397	51.59864	49.42143	49.29919		
33.39019	34.2517	33.63571	30.97035		
24.62687	24.88095	25.575	21.03774		
61.30064	61.51361	61.71071	59.55526		
89.08316	89.14966	89.19286	88.59838		
60.12793	61.05442	59.89286	59.16442		
77.3774	76.71769	78.34643	75.43127		
46.26866	47.14286	46.3	44.5283		
28.42217	29.33673	28.69643	25.80863		
49.40299	49.64286	49.975	47.07547		
44.30704	45.10204	44.44286	42.37197		
93.0064	93.23129	92.90714	92.91105		
83.19829	83.02721	83.62143	82.12938		
86.20469	85.90136	86.70357	85.13477		
34.371	35.27211	34.56429	32.04852		
67.12154	67.82313	66.98571	66.25337		
71.23667	71.34354	71.58929	69.87871		
60.25586	60.68027	60.48571	58.7062		
73.19829	73.38435	73.44643	72.03504		
76.07676	76.63265	75.93571	75.49865		
64.11514	64.94898	63.90357	63.24798		
46.20469	47.32993	46.00357	44.75741		
62.15352	62.90816	62.04643	61.09164		
66.07676	66.9898	65.76071	65.40431		
88.16631	87.94218	88.56071	87.29111		
88.10235	88.12925	88.26429	87.52022		
73.19829	73.38435	73.44643	72.03504		
96.9936	97.12585	96.91786	96.99461		
28.42217	29.33673	28.69643	25.80863		
77.31343	76.90476	78.05	75.66038		
83.85928	84.98299	83.06786	84.3531		
80.12793	80.34014	80.24286	79.3531		
86.20469	85.90136	86.70357	85.13477		
82.21748	82.0068	82.69286	81.05121		
69.21109	69.4898	69.43571	67.95148		
80.25586	79.96599	80.83571	78.89488		
54.11514	55.30612	53.72857	53.15364		
64.24307	64.57483	64.49643	62.78976		
65.22388	65.59524	65.425	63.86792		
66.20469	66.61565	66.35357	64.94609		
47.97441	49.93197	46.97143	47.60108		
53.07036	54.47279	52.50357	52.30458		
20.3838	21.73469	20.37857	17.87062		
58.89126	60.78231	57.77857	59.0027		
71.10874	71.71769	70.99643	70.33693		
28.29424	29.71088	28.10357	26.26685		
31.36461	32.39796	31.48214	29.04313		
76.07676	76.63265	75.93571	75.49865		
22.34542	23.77551	22.23571	20.02695		

R20 Regulation Weightage of Marks

Final exam	Internal tests	Ass/Quiz
70	20	10
0.7	0.2	0.1

Weightage marks for each CO

	CO 1	CO 2	CO 3	CO 4			Total
EM	23	21	26	28			98
IM	10	7	14	9			40
AM	5	5	6	4			20

% Weightage of each CO

	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6	Total
EM (%)	23.46939	21.42857	26.53061	28.57143			100
IM (%)	25	17.5	35	22.5			100
AM (%)	25	25	30	20			100
Avg	23.92857	21	28.57143	26.5			100

84	21091A0475	10	10	20	75	55		50	100	78.57143		74.84009	76.36054	73.82143	75.33693				
85	21091A0476	11	10	21	54	33		55	100	47.14286		54.30704	54.7449	54.61786	52.46631				
86	21091A0477	5	10	15	33	18		25	100	25.71429		33.32623	34.43878	33.33929	31.19946				
87	21091A0478	5	10	15	33	18		25	100	25.71429		33.32623	34.43878	33.33929	31.19946				
88	21091A0479	8	10	18	43	25		40	100	35.71429		43.32623	44.08163	43.51429	41.2938				
89	21091A0480	3	10	13	29	16		15	100	22.85714		29.27505	30.73129	29.03214	27.34501				
90	21091A0481	14	10	24	73	49		70	100	70		73.13433	73.57143	73.15	72.26415				
91	21091A0482	17	10	27	83	56		85	100	80		83.13433	83.21429	83.325	82.35849				
92	21091A0483	10	10	20	64	44		50	100	62.85714		64.05117	65.13605	63.60714	63.47709				
93	21091A0484	5	10	15	20	5		25	100	7.142857		20.57569	21.17347	21.26786	17.18329				
94	21091A0485	8	10	18	48	30		40	100	42.85714		48.23028	49.18367	48.15714	46.68464				
95	21091A0486	14	10	24	73	49		70	100	70		73.13433	73.57143	73.15	72.26415				
96	21091A0487	11	10	21	59	38		55	100	54.28571		59.21109	59.84694	59.26071	57.85714				
97	21091A0488	12	10	22	64	42		60	100	60		64.1791	64.7619	64.2	63.01887				
98	21091A0489	4	10	14	32	18		20	100	25.71429		32.28145	33.60544	32.11429	30.3504				
99	21091A0490	7	10	17	68	51		35	100	72.85714		67.78252	69.77891	66.43214	68.47709				
100	21091A0491	11	10	21	60	39		55	100	55.71429		60.1919	60.86735	60.18929	58.93531				
101	21091A0493	18	10	28	84	56		90	100	80		84.1791	84.04762	84.55	83.20755				
102	21091A0494	11	10	21	61	40		55	100	57.14286		61.17271	61.88776	61.11786	60.01348				
103	21091A0495	8	10	18	57	39		40	100	55.71429		57.05757	58.36735	56.51429	56.38814				
104	21091A0496	16	10	26	80	54		80	100	77.14286		80.12793	80.34014	80.24286	79.3531				
105	21091A0497	13	10	23	80	57		65	100	81.42857		79.93603	80.90136	79.35357	80.04043				
106	21091A0498	7	10	17	42	25		35	100	35.71429		42.28145	43.2483	42.28929	40.44474				
107	21091A0499	15	10	25	68	43		75	100	61.42857		68.29424	68.28231	68.80357	66.6442				
108	21091A04A0	9	10	19	53	34		45	100	48.57143		53.19829	54.09864	53.09643	51.84636				
109	21091A04A1	8	10	18	52	34		40	100	48.57143		52.15352	53.26531	51.87143	50.9973				
110	21091A04A2	9	10	19	53	34		45	100	48.57143		53.19829	54.09864	53.09643	51.84636				
111	21091A04A3	15	10	25	73	48		75	100	68.57143		73.19829	73.38435	73.44643	72.03504				
112	21091A04A4	16	10	26	75	49		80	100	70		75.22388	75.2381	75.6	73.96226				
113	21091A04A5	9	10	19	45	26		45	100	37.14286		45.35181	45.93537	45.66786	43.22102				
114	21091A04A6	13	10	23	56	33		65	100	47.14286		56.39659	56.41156	57.06786	54.16442				
115	21091A04A7	10	10	20	53	33		50	100	47.14286		53.26226	53.91156	53.39286	51.61725				
116	21091A04A8	14	10	24	76	52		70	100	74.28571		76.07676	76.63265	75.93571	75.49865				
117	21091A04A9	12	10	22	59	37		60	100	52.85714		59.27505	59.65986	59.55714	57.62803				
118	21091A04B0	5	10	15	32	17		25	100	24.28571		32.34542	33.41837	32.41071	30.12129				
119	21091A04B1	9	10	19	37	18		45	100	25.71429		37.50533	37.77211	38.23929	34.59569				
120	21091A04B2	6	10	16	31	15		30	100	21.42857		31.42857	32.21088	31.77857	28.81402				
121	21091A04B3	16	10	26	77	51		80	100	72.85714		77.1855	77.27891	77.45714	76.1186				
122	21091A04B4	9	10	19	44	25		45	100	35.71429		44.371	44.91497	44.73929	42.14286				
123	21091A04B5	10	10	20	53	33		50	100	47.14286		53.26226	53.91156	53.39286	51.61725				
124	21091A04B6	5	10	15	27	12		25	100	17.14286		27.44136	28.31633	27.76786	24.73046				
125	21091A04B7	5	10	15	43	28		25	100	40		43.13433	44.64286	42.625	41.98113				
126	21091A04B8	8	10	18	18			40	100	0		18.80597	18.57143	20.3	14.33962				
127	21091A04B9	10	10	20	38	18		50	100	25.71429		38.55011	38.60544	39.46429	35.44474				
128	21091A04C0	15	10	25	78	53		75	100	75.71429		78.10235	78.48639	78.08929	77.42588				
129	21091A04C1	10	10	20	46	26		50	100	37.14286		46.39659	46.76871	46.89286	44.07008				
130	21091A04C2	2	10	12	24	12		10	100	17.14286		24.30704	25.81633	24.09286	22.18329				
131	21091A04C3	13	10	23	71	48		65	100	68.57143		71.10874	71.71769	70.99643	70.33693				
132	21091A04C4	16	10	26	71	45		80	100	64.28571		71.30064	71.15646	71.88571	69.6496				
133	21091A04C5	14	10	24	78	54		70	100	77.14286		78.03838	78.67347	77.79286	77.65499				
134	21091A04C6	18	10	28	89	61		90	100	87.14286		89.08316	89.14966	89.19286	88.59838				
135	21091A04C7	6	10	16	51	35		30	100	50		51.04478	52.61905	50.35	50.37736				
136	2209SA0407	18	10	28	92	64		90	100	91.42857		92.02559	92.21088	91.97857	91.83288				
137	2209SA0408	10	10	20	48	28		50	100	40		48.35821	48.80952	48.75	46.22642				
138	2209SA0409	9	10	19	54	35		45	100	50		54.1791	55.11905	54.025	52.92453				
139	2209SA0411	16	10	26	89	63		80	100	90		88.95522	89.52381	88.6	89.0566				
140	2209SA0413	13	10	23	75	52		65	100	74.28571		75.03198	75.79932	74.71071	74.6496				
141	2209SA0415	15	10	25	75	50		75	100	71.42857		75.15991	75.42517	75.30357	74.19137				
142	2209SA0417	17	10	27	63	36		85	100	51.42857		63.51812	62.80612	64.75357	60.79515				
143	2209SA0422	18	10	28	91	63		90	100	90		91.04478	91.19048	91.05	90.75472				
144	2209SA0428	11	10	21	50	29		55	100	41.42857		50.3838	50.66327	50.90357	48.15364				
145	2209SA0429	16	10	26	76	50		80	100	71.42857		76.20469	76.2585	76.52857	75.04043				
146	2209SA0435	14	10	24	70	46		70	100	65.71429		70.1919	70.5102	70.36429	69.02965				
147	2209SA0436	9	10	19	61	42		45	100	60		61.04478	62.2619	60.525	60.4717				
148	21091A04C8	5	10	15	49	34		25	100	48.57143		49.01919	50.76531	48.19643	48.45013				
149	21091A04C9	10	10	20	62	42		50	100	60		62.08955	63.09524	61.75	61.32075				
150	21091A04D0	4	10	14	26	12		20	100	17.14286		26.39659	27.48299	26.54286	23.8814				
151	21091A04D1	11	10	21	72	51		55	100	72.85714		71.96162	73.11224	71.33214	71.87332				
152	21091A04D2	2	10	12	24	12		10	100	17.14286		24.30704	25.81633	24.09286	22.18329				
153	21091A04D3	6	10	16	47	31		30	100	44.28571		47.12154	48.53741	46.63571	46.06469				
154	21091A04D4	12	10	22	72	50		60	100	71.42857		72.02559	72.92517	71.62857	71.6442				
155	21091A04D5	5	10	15	40	25		25	100	35.71429		40.1919	41.58163	39.83929	38.74663				
156	21091A04D6	11	10	21	70	49		55	100	70		70	71.07143	69.475	69.71698				
157	21091A04D7	9	10	19	64	45		45	100	64.28571		63.98721	65.32313	63.31071	63.7062				
158	21091A04D8	12	10	22	59	37		60	100	52.85714		59.27505	59.65986	59.55714	57.62803				
159	21091A04D9	3	10	13	41	28		15	100	40		41.04478	42.97619	40.175	40.28302				
160	21091A04E0	16	10	26	85	59		80	100	84.28571		85.03198	85.44218	84.88571	84.74394				
161	21091A04E1	2	10	12	27	15		10	100	21.42857		27.24947	28.87755	26.87857	25.41779				
162	21091A04E2	7	10	17	54	37		35	100	52.85714		54.05117	55.4932	53.43214	53.38275				
163	21091A04E3	3	10	13	40	27		15	100	38.57143		40.06397	41.95578	39.24643	39.20485				
164	21091A04E4	16	10	26	79	53		80	100	75.71429		79.14712	79.31973	79.31429	78.27493				
165	21091A04E5	1	10	11	14	3		5	100	4.285714		14.43497	15.79932	14.51071	11.63073				
166	21091A04E6	2	10	12	40	28		10	100	40		40	42.14286	38.95	39.43396				
167	21091A04E7	15	10	25	83	58		75	100	82.85714		83.0064	83.58844	82.73214	82.81671				
168	21091A04E8	11	10	21	72	51		55	100	72.85714		71.96162	73.11224	71.33214	71.87332				
169	21091A04E9	16	10	26	81	55		80	100	78.57143		81.10874	81.36054	81.17143	80.43127				
170	21091A04F0	11	10	21	74	53		55	100	75.71429		73.92324	75.15306	73.18929	74.02965				
171	21091A04F1	11	10	21	61	40		55	100	57.14286		61.17271	61.88776	61.11786	60.01348				
172	21091A04F2	14	10	24	77	53		70	100	75.71429		77.05757	77.65306	76.86429	76.57682				
173	21091A04F3	6	10	16	48	32		30	100	45.71429		48.10235	49.55782	47.56429	47.14286				
174	21091A04F4	-2	10	8	9	1		-10	100	1.428571		9.339019	11.2585	8.978571	6.927224				
175	21091A04F5	1	10	11	25	14		5	100	20		25.22388	27.02381	24.725	23.49057				
176	21091A04F6	1	10	11	31	20		5	100	28.57143		31.10874	33.14626	30.29643	29.95957				
177	21091A04F7	17	10	27	84	57		85	100	81.42857		84.11514	84.23469	84.25357	83.43666				
178	21091A04F8	9	10	19	49	30		45	100	42.85714		49.27505	50.01701	49.38214	47.53369				
179	21091A04F9	14	10	24	72	48		70	100	68.57143		72.15352	72.55102	72.22143	71.18598				
180	21091A04G0	0	10	10	13	3		0	100	4.285714		13.39019	14.96599	13.28571	10.78167				
181	21091A04G1	8	10	18	46	28		40	100	40		46.26866	47.14286	46.3	44.5283				
182	21091A04G2	9	10	19	63	44		45	100	62.85714		63.0064	64.30272	62.38214	62.62803				
183	21091A04G3	0	10	10	12	2		0	100	2.857143		12.40938	13.94558	12.35714	9.703504				
184	21091A04G4	0	10	10	40	30		0	100	42.85714		39.87207	42.51701	38.35714	39.89218				
185	21091A04G5	8	10	18	58	40		40	100	57.14286		58.03838	59.38776	57.44286	57.46631				
186	21091A04G6	6	10	16	49	33		30	100	47.14286		49.08316	50.57823	48.49286	48.22102				
187	21091A04G7	5	10	15	46	31		25	100	44.28571		46.07676	47.70408	45.41071	45.21563				
188	21091A04G8	6	10	16	48	32		30	100	45.71429		48.10235	49.55782	47.56429	47.14286				
189	21091A04G9	6	10	16	60	44		30	100	62.85714		59.87207	61.80272	58.70714	60.08086				
190	21091A04H0	12	10	22	60	38		60	100	54.28571		60.25586	60.68027	60.48571	58.7062				
191	21091A04H1	9	10	19	60	41		45	100	58.57143		60.06397	61.2415	59.59643	59.39353				
192	21091A04H2	2	10	12	40	28		10	100	40		40	42.14286	38.95	39.43396				
193	21091A04H3	6	10	16	32	16		30	100	22.85714		32.40938	33.23129	32.70714	29.89218				
194	21091A04H4	12	10	22	22			60	100	0		22.98507	21.90476	25.2	17.73585				
195	21091A04H5	5	10	15	47	32		25	100	45.71429		47.05757	48.72449	46.33929	46.2938				
196	21091A04H6	6	10	16	31	15		30	100	21.42857		31.42857	32.21088	31.77857	28.81402				
197	21091A04H7	4	10	14	32	18		20	100	25.71429		32.28145	33.60544	32.11429	30.3504				
198	21091A04H8	2	10	12	25	13		10	100	18.57143		25.28785	26.83673	25.02143	23.26146				
199	21091A04H9	18	10	28	85	57		90	100	81.42857		85.15991	85.06803	85.47857	84.28571				
200	21091A04I0	19	10	29	84	55		95	100	78.57143		84.24307	83.86054	84.84643	82.97844				
201	21091A04I1	16	10	26	64	38		80	100	54.28571		64.43497	64.01361	65.38571	62.10243				
202	21091A04I2	11	10	21	58	37		55	100	52.85714		58.23028	58.82653	58.33214	56.77898				
203	21091A04I3	14	10	24	85	61		70	100	87.14286		84.90405	85.81633	84.29286	85.20216				
204	21091A04I4	11	10	21	70	49		55	100	70		70	71.07143	69.475	69.71698				
205	21091A04I5	5	10	15	40	25		25	100	35.71429		40.1919	41.58163	39.83929	38.74663				
206	21091A04I6	3	10	13	40	27		15	100	38.57143		40.06397	41.95578	39.24643	39.20485				
207	21091A04I7	12	10	22	81	59		60	100	84.28571		80.85288	82.10884	79.98571	81.34771				
208	21091A04I8	7	10	17	62	45		35	100	64.28571		61.89765	63.65646	60.86071	62.00809				
209	21091A04I9	15	10	25	79	54		75	100	77.14286		79.08316	79.5068	79.01786	78.50404				
210	2209SA0401	9	10	19	45	26		45	100	37.14286		45.35181	45.93537	45.66786	43.22102				
211	2209SA0405	5	10	15	49	34		25	100	48.57143		49.01919	50.76531	48.19643	48.45013				
212	2209SA0412	8	10	18	45	27		40	100	38.57143		45.28785	46.12245	45.37143	43.45013				
213	2209SA0414	18	10	28	82	54		90	100	77.14286		82.21748	82.0068	82.69286	81.05121				
214	2209SA0418	11	10	21	70	49		55	100	70		70	71.07143	69.475	69.71698				
215	2209SA0419	14	10	24	76	52		70	100	74.28571		76.07676	76.63265	75.93571	75.49865				
216	2209SA0421	18	10	28	88	60		90	100	85.71429		88.10235	88.12925	88.26429	87.52022				
217	2209SA0425	17	10	27	81	54		85	100	77.14286		81.17271	81.17347	81.46786	80.20216				
218	2209SA0426	11	10	21	76	55		55	100	78.57143		75.88486	77.19388	75.04643	76.18598				
219	2209SA0430	11	10	21	54	33		55	100	47.14286		54.30704	54.7449	54.61786	52.46631				
220	2209SA0432	17	10	27	75	48		85	100	68.57143		75.28785	75.05102	75.89643	73.73315				
221	2209SA0437	2	10	12	34	22		10	100	31.42857		34.11514	36.02041	33.37857	32.96496				

222	19091A04N9	12	10	22	77	55		60	100	78.57143	76.92964	78.02721	76.27143	77.03504		
223	20091A0481	8	10	18	18			40	100	0	18.80597	18.57143	20.3	14.33962		
224	20091A0482	6	10	16	44	28		30	100	40	44.1791	45.47619	43.85	42.83019		
225	20091A0498	2	10	12	27	15		10	100	21.42857	27.24947	28.87755	26.87857	25.41779		
226	20091A04A1	1	10	11	25	14		5	100	20	25.22388	27.02381	24.725	23.49057		
227	20091A04F0	1	10	11	19	8		5	100	11.42857	19.33902	20.90136	19.15357	17.02156		
228	20091A04F3	9	10	19	19			45	100	0	19.85075	19.40476	21.525	15.18868		
229	20091A04K9	9	10	19	19			45	100	0	19.85075	19.40476	21.525	15.18868		
230	20091A04M0	9	10	19	19			45	100	0	19.85075	19.40476	21.525	15.18868		
231	20091A04M4	15	10	25	71	46		75	100	65.71429	71.23667	71.34354	71.58929	69.87871		
232	21091A04K0	14	10	24	70	46		70	100	65.71429	70.1919	70.5102	70.36429	69.02965		
233	21091A04K1	11	10	21	46	25		55	100	35.71429	46.46055	46.58163	47.18929	43.84097		
234	21091A04K2	11	10	21	80	59		55	100	84.28571	79.8081	81.27551	78.76071	80.49865		
235	21091A04K3	10	10	20	68	48		50	100	68.57143	67.97441	69.21769	67.32143	67.78976		
236	21091A04K4	7	10	17	46	29		35	100	41.42857	46.20469	47.32993	46.00357	44.75741		
237	21091A04K5	-2	10	8	10	2		-10	100	2.857143	10.31983	12.27891	9.907143	8.005391		
238	21091A04K6	1	10	11	14	3		5	100	4.285714	14.43497	15.79932	14.51071	11.63073		
239	21091A04K7	3	10	13	40	27		15	100	38.57143	40.06397	41.95578	39.24643	39.20485		
240	21091A04K8	10	10	20	57	37		50	100	52.85714	57.1855	57.9932	57.10714	55.92992		
241	21091A04K9	4	10	14	43	29		20	100	41.42857	43.07036	44.82993	42.32857	42.21024		
242	21091A04M0	7	10	17	71	54		35	100	77.14286	70.72495	72.84014	69.21786	71.71159		
243	21091A04M1	15	10	25	58	33		75	100	47.14286	58.48614	58.07823	59.51786	55.86253		
244	21091A04M2	9	10	19	60	41		45	100	58.57143	60.06397	61.2415	59.59643	59.39353		
245	21091A04M3	12	10	22	66	44		60	100	62.85714	66.14072	66.80272	66.05714	65.1752		
246	21091A04M4	1	10	11	11	0		5	100	0	11.49254	12.7381	11.725	8.396226		
247	21091A04M5	-2	10	8	28	20		-10	100	28.57143	27.97441	30.64626	26.62143	27.4124		
248	21091A04M6	19	10	29	95	66		95	100	94.28571	95.03198	95.08503	95.06071	94.83827		
249	21091A04M7	15	10	25	83	58		75	100	82.85714	83.0064	83.58844	82.73214	82.81671		
250	21091A04M8	12	10	22	75	53		60	100	75.71429	74.96802	75.98639	74.41429	74.87871		
251	21091A04M9	4	10	14	55	41		20	100	58.57143	54.84009	57.07483	53.47143	55.14825		
252	21091A04N0	10	10	20	68	48		50	100	68.57143	67.97441	69.21769	67.32143	67.78976		
253	21091A04N1	2	10	12	40	28		10	100	40	40	42.14286	38.95	39.43396		
254	21091A04N2	4	10	14	46	32		20	100	45.71429	46.01279	47.89116	45.11429	45.44474		
255	21091A04N3	5	10	15	40	25		25	100	35.71429	40.1919	41.58163	39.83929	38.74663		
256	21091A04N4	10	10	20	78	58		50	100	82.85714	77.78252	79.42177	76.60714	78.57143		
257	21091A04N5	10	10	20	58	38		50	100	54.28571	58.16631	59.01361	58.03571	57.00809		
258	21091A04N7	6	10	16	43	27		30	100	38.57143	43.19829	44.45578	42.92143	41.75202		
259	21091A04N8	17	10	27	75	48		85	100	68.57143	75.28785	75.05102	75.89643	73.73315		
260	21091A04N9	13	10	23	75	52		65	100	74.28571	75.03198	75.79932	74.71071	74.6496		
261	21091A04P0	1	10	11	33	22		5	100	31.42857	33.07036	35.18707	32.15357	32.1159		
262	21091A04P1	16	10	26	80	54		80	100	77.14286	80.12793	80.34014	80.24286	79.3531		
263	21091A04P2	8	10	18	65	47		40	100	67.14286	64.90405	66.53061	63.94286	65.01348		
264	21091A04P3	19	10	29	95	66		95	100	94.28571	95.03198	95.08503	95.06071	94.83827		
265	21091A04P4	12	10	22	53	31		60	100	44.28571	53.39019	53.53741	53.98571	51.15903		
266	21091A04P5	3	10	13	29	16		15	100	22.85714	29.27505	30.73129	29.03214	27.34501		
267	21091A04P6	11	10	21	65	44		55	100	62.85714	65.09595	65.96939	64.83214	64.32615		
268	21091A04P7	0	10	10	23	13		0	100	18.57143	23.19829	25.17007	22.57143	21.56334		
269	21091A04P8	18	10	28	91	63		90	100	90	91.04478	91.19048	91.05	90.75472		
270	21091A04P9	13	10	23	74	51		65	100	72.85714	74.05117	74.77891	73.78214	73.57143		
271	21091A04Q0	8	10	18	48	30		40	100	42.85714	48.23028	49.18367	48.15714	46.68464		
272	21091A04Q1	11	10	21	65	44		55	100	62.85714	65.09595	65.96939	64.83214	64.32615		
273	21091A04Q2	4	10	14	40	26		20	100	37.14286	40.12793	41.76871	39.54286	38.97574		
274	21091A04Q3	0	10	10	21	11		0	100	15.71429	21.23667	23.12925	20.71429	19.40701		
275	21091A04Q4	4	10	14	43	29		20	100	41.42857	43.07036	44.82993	42.32857	42.21024		
276	21091A04Q5	3	10	13	27	14		15	100	20	27.31343	28.69048	27.175	25.18868		
277	21091A04Q6	0	10	10	25	15		0	100	21.42857	25.15991	27.21088	24.42857	23.71968		
278	21091A04Q7	11	10	21	51	30		55	100	42.85714	51.36461	51.68367	51.83214	49.23181		
279	21091A04Q8	6	10	16	41	25		30	100	35.71429	41.23667	42.41497	41.06429	39.59569		
280	21091A04Q9	4	10	14	42	28		20	100	40	42.08955	43.80952	41.4	41.13208		
281	21091A04R0	0	10	10	17	7		0	100	10	17.31343	19.04762	17	15.09434		
282	21091A04R1	5	10	15	26	11		25	100	15.71429	26.46055	27.29592	26.83929	23.65229		
283	21091A04R2	7	10	17	50	33		35	100	47.14286	50.12793	51.41156	49.71786	49.07008		
284	21091A04R3	0	10	10	17	7		0	100	10	17.31343	19.04762	17	15.09434		
285	21091A04R4	2	10	12	28	16		10	100	22.85714	28.23028	29.89796	27.80714	26.49596		
286	21091A04R5	10	10	20	71	51		50	100	72.85714	70.91684	72.27891	70.10714	71.02426		
287	21091A04R6	5	10	15	24	9		25	100	12.85714	24.49893	25.2551	24.98214	21.49596		
288	21091A04R7	1	10	11	14	3		5	100	4.285714	14.43497	15.79932	14.51071	11.63073		
289	21091A04R8	5	10	15	32	17		25	100	24.28571	32.34542	33.41837	32.41071	30.12129		
290	21091A04R9	11	10	21	73	52		55	100	74.28571	72.94243	74.13265	72.26071	72.95148		
291	21091A04S0	5	10	15	40	25		25	100	35.71429	40.1919	41.58163	39.83929	38.74663		
292	21091A04S1	-1	10	9	10	1		-5	100	1.428571	10.3838	12.09184	10.20357	7.77628		
293	2209SA0423	17	10	27	89	62		85	100	88.57143	89.01919	89.33673	88.89643	88.82749		
294	2209SA0431	8	10	18	43	25		40	100	35.71429	43.32623	44.08163	43.51429	41.2938		
295	2209SA0434	10	10	20	67	47		50	100	67.14286	66.9936	68.19728	66.39286	66.71159		

	CO 1		CO 2		CO 3		CO 4					
	No. of students Attained	Weightage Points	No. of students Attained	Weightage Points	No. of students Attained	Weightage Points	No. of students Attained	Weightage Points				
>= 45%	204	3	192	3	190	3	181	3				
40% to 45%	24	2	17	2	9	2	18	2				
<40%	67	1	53	1	63	1	63	1				
Total No. of students	295		262		262		262					
Atainment value		2.46		2.53		2.48		2.45				
% of Attainment		69.15		73.28		72.52		69.08				
Attained or not		YES		YES		YES		YES				

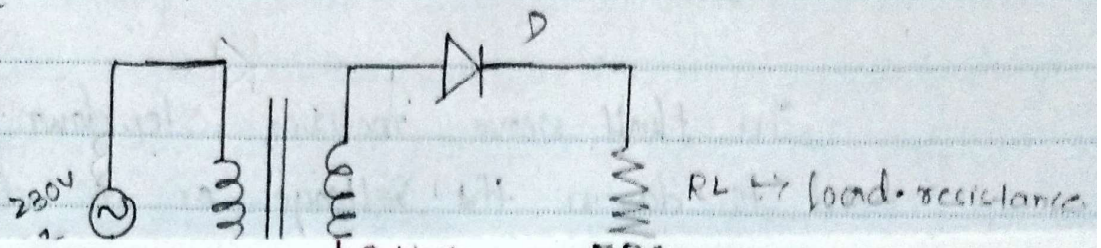
II Year Threshold
45

CO	CO Attainment Value	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO 1	2.46	3	2											2	2	
CO 2	2.53	1	3											2	3	
CO 3	2.48	2		3										1	2	1
CO 4	2.45		2	3										2	1	
EDC		2.48	2.49	2.47	-	-	-	-	-	-	-	-	-	2.48	2.49	2.48

(ESTD-1995)

2 b) Half wave rectifier

Circuit :-



Subject : EDC

Q.P. Code : A0403203R0223

For Office Use 12403183

VALUATION-II

Q.No.	1	2	3	4	5	6	7
A							
B							
C							
D							
E							
F							
G							
TOTAL							

GRAND TOTAL

(in words)

Signature of the Examiner

Signature of the Scrutinizer

Subject : EDC

Q.P. Code : A0403203R0223

For Office Use 12403183

VALUATION-I

Q.No.	1	2	3	4	5	6	7
A	2	7	10	6	2	4	5
B	2	7	2	5	2	2	5
C	0						
D	2						
E	2						
F	2						
G	2						
TOTAL	12	14	12	11	4	6	10

GRAND TOTAL 59

(in words) Five Nine

Signature of the Examiner

Signature of the Scrutinizer

For Office Use 12403183

INSTRUCTIONS TO THE STUDENTS

1. The student is prohibited from :

   - Writing his / her Hall Ticket Number in any part of his / her Answer Booklet
   - Writing his / her name or any other matter including God's name say Om, Rama etc. or any symbol which may lead to his / her identification, in any part of the Answer Booklet
   - Addressing the Examiner in any manner what-so-ever in his / her Answer Booklet.

2. Every student has to :

   - Enter the Question Paper Code Number received by them in the Block specified on the first Page of the answer booklet.
   - Write the Correct number and sub-number of the question, answered
   - Write answers legibly on both sides of the page.

3. No loose sheets or paper will be allowed into the examination hall and no paper must be detached from the Answer Booklet.

4. Students should not write more than 25 lines per page. It is not necessary to begin each answer on a fresh page.

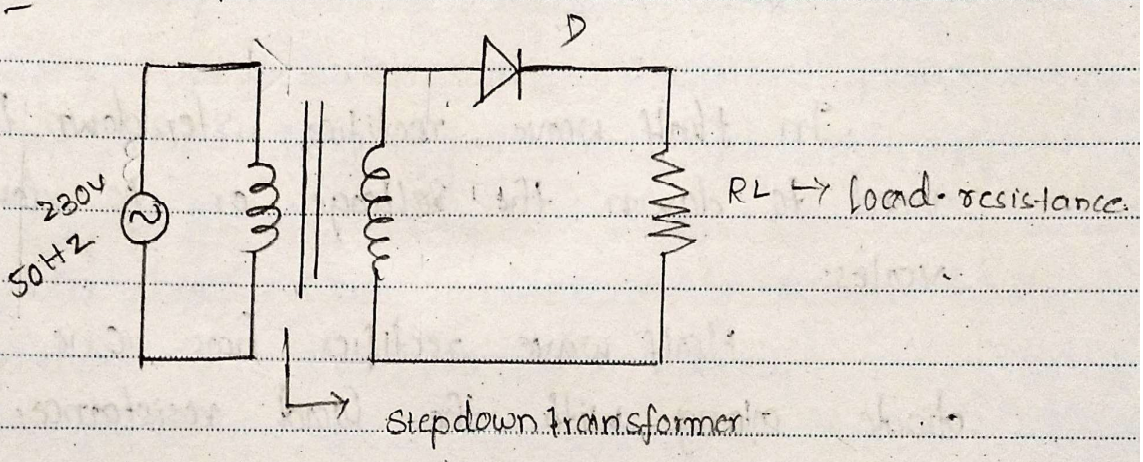
5. Students will not be allowed into the Examination Hall after the commencement of the Examination and not permitted to leave the Examination Hall till the completion of the duration.

6. Carrying / Keeping Cell Phones in the examination hall will amounts for malpractice.

(ESTD-1995)

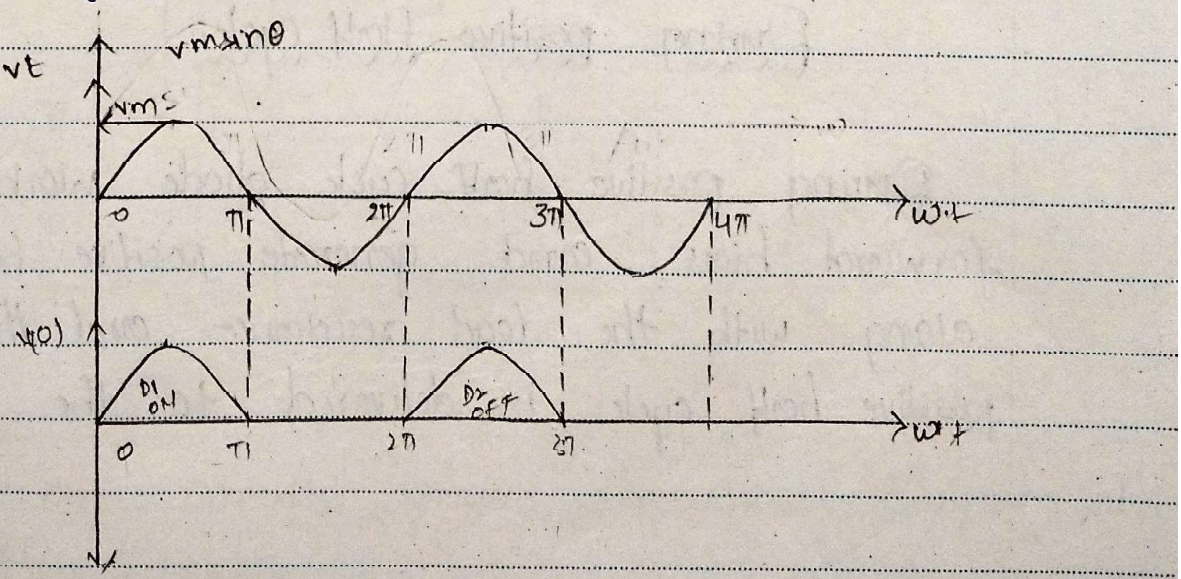
2(a) Half-wave rectifier

Circuit:-



The above figure signifies the circuit and its

Output wave forms:-



For the use of Evaluator Only

Q.No	Marks

Q.No	Marks

Q.No	Marks

The above figure signifies both circuit and the input and output waveforms of Half wave rectifier.

In Half wave rectifier step down transformer is used to down the voltage or to down the current scales.

Half wave rectifier has one p-N Junction diode along with the load resistance.

Operation of Half wave rectifier:-

During positive Half cycle:

During positive half cycle diode works under forward bias and generate positive half cycle along with the load resistance and the produced positive half cycle is delivered to the output

For the use of Evaluator Only

Q.No	Marks

Q.No	Marks
2a	7

Q.No	Mar

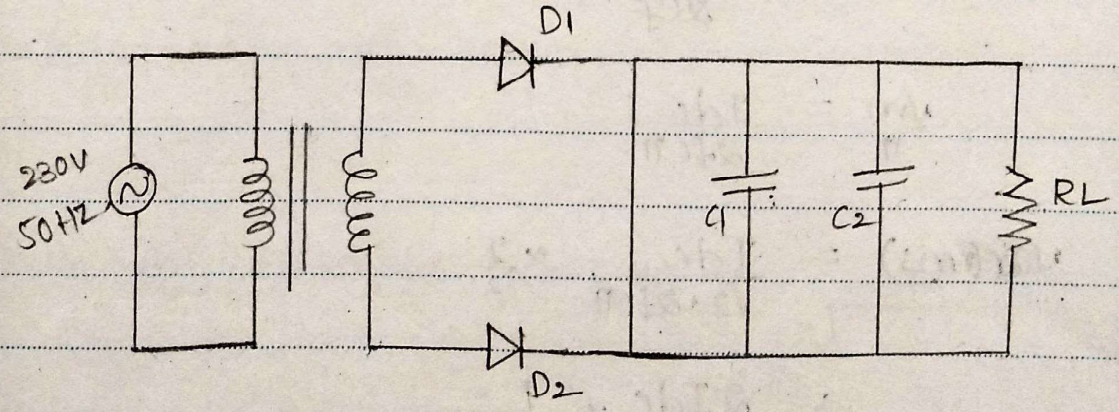
(ESTD-1995)

During negative half cycle:

During negative half cycle the p-N Junction diode works under Reversed bias condition then the diode act as open switch and no-current flow through it and their won't be negative half cycle at output

Hence in half wave rectifier only positive half cycle is produced or given to the output.

2b) Π-Section filter:



The above circuit signifies the circuit diagram of Π-Section filter

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Q.No	Marks

Q.No	Marks

Q.No	Marks

(ESTD-1995)

The π-Section filter greatly reduces the AC component when compared with the full wave rectifier with capacitor filter greatly reduces the AC component and provide a pure DC.

Ripple factor for π-Section.

Qcharge = Qdischarge

$Q_{VM} = I_{DC} \frac{T}{2}$

$V_m = \frac{I_{DC} T}{2Cf}$

$\frac{V_m}{\pi} = \frac{I_{DC}}{2fC\pi}$

$V_{ac(rms)} = \frac{I_{DC}}{\sqrt{2} \cdot 2fC\pi} \times \frac{2}{2}$

$= \frac{2 I_{DC}}{\sqrt{2}} \cdot \frac{1}{4\pi fC}$

$V_{a(rms)} = \sqrt{2} I_{DC} \cdot X_C$

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Q.No	Marks

Q.No	Marks

Q.No	M

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$$I_{ac(rms)} = V_{ac(rms)} \cdot \frac{1}{X_L}$$

$$= \frac{\sqrt{2}\, I_{dc} X_{C1}}{X_L}$$

$$V_{ac(rms)} = I_{ac(rms)}\, X_{C2}$$

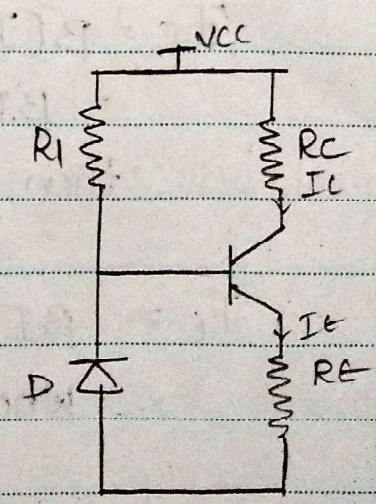
$$= \frac{\sqrt{2}\, I_{dc}\, X_{C1}\, X_{C2}}{X_L}$$

where $I_{dc} = \frac{V_{dc}}{R_L}$

$$V_{ac(rms)} = \frac{\sqrt{2}\, V_{dc}}{R_L} \cdot \frac{X_{C1} \cdot X_{C2}}{X_L}$$

$$\frac{V_{ac(rms)}}{V_{dc}} = \frac{\sqrt{2}}{R_L} \cdot \frac{X_{C1} X_{C2}}{X_L}$$

3a) Diode compensation technique.



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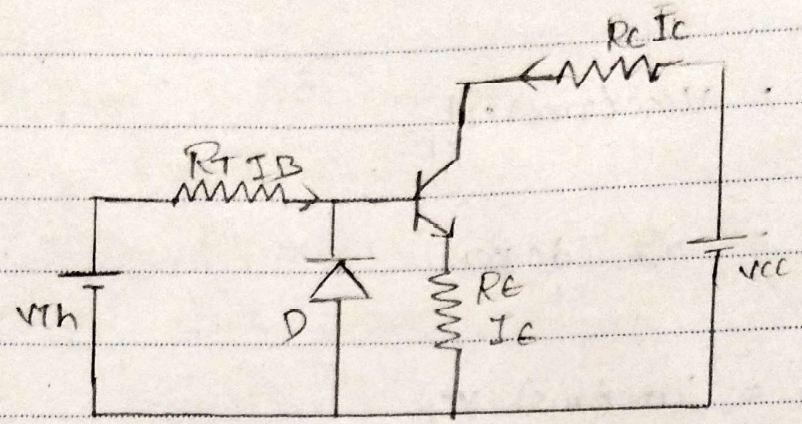
Q.No	Marks
2b	7

Q.No	Marks

Q.No	Marks



(b)

$$I = I_O + I_B$$

$$I_B = (I - I_O)$$

for I_C current equation

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

Substitute the I_B value in Current equation

then,

$$I_C = \beta(I - I_O) + (1+\beta) I_{CO}$$

$$= \beta I - \beta I_O + \beta I_{CO}$$

then take commom β

$$I_C = \beta I - \beta(I_O + I_{CO})$$

- When $(I_O + I_{CO})$ are same then.

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Q.No	Marks

Q.No	Marks

Q.No	Marks

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$$I_C = \beta I$$

$$\frac{\partial I_C}{\partial I_{CO}} = 0 \text{ //}$$

3b) The R_E in the biasing techniques are R_E is the resistance for emitter. because of the presence of R_E in the biasing techniques. they are getting loss of gain because of presence of R_E R_E provides the negative feedback to the biasing circuits.

3a) JFET

⇒ Junction field effect Transistor

⇒ JFET is a unipolar devices which it has only one mode depletion mode.

⇒ The input resistance in the JFET is very large

⇒ JFET has no thermal runway, &

⇒ It has 3 terminals Gate, Source, Drain

⇒ It has JFET is a voltage controlled devices.

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Q.No	Marks
3a	10

Q.No	Marks
3b	2

Q.No	Marks

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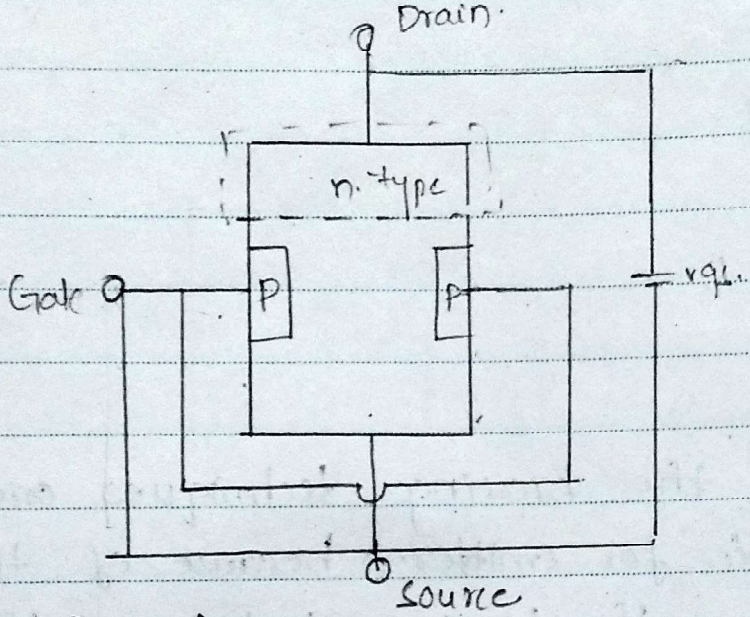

$i_D = f(V_{GS}, V_{DS})$

$V_{gs} = 0$

$V_{ds} = 0$

Transistor is in ON state

No current flows through the transistor

gm (Transconductance) = The transconductance is the ratio between output drain current(I_d) vs input voltage (V_{gs}) by keeping output voltage as constant

$$g_m = \frac{\Delta I_d}{\Delta V_{GS}} \Big| V_{DS} = \text{constant}$$

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Q.No	Marks

Q.No	Marks

Q.No	Marks

(ESTD-1995)

Drain Resistance (r_d):-

It is the ratio between output voltage (V_{ds}) and output current voltage v_{ds} by keeping the input voltage as constant

$$r_d = \frac{V_{ds}}{I_d}$$

$$r_d = \frac{v_{ds}}{I_d} \Big| v_{gs} \text{ constant}$$

Amplification factor (μ):-

It is the product of Transconductance (g_m) and Drain resistance (r_d) by keeping I_d constant.

$$\boxed{\mu = g_m \times r_d}$$

$$= \frac{I_d}{V_{GS}} \times \frac{v_{ds}}{I_d}$$

$$= \frac{v_{ds}}{V_{GS}} \Big| I_d \text{ constant}$$

For the use of Evaluator Only

Q.No	Marks
7a	8

Q.No	Marks

Q.No	Marks

(ESTD-1995)

7b) The given data

$V_{TN} = 1V$

$I_D = 0.8mA$

$V_{GS} = 3V$

$V_{DS} = 4.5$

$V_{DS} > V_{GS} - V_T$

$\Rightarrow I_D = k(V_{GS} - V_t)^2$

$\Rightarrow \frac{I_D}{(V_{GS} - V_t)^2} = k$

$k = \frac{0.8 \times 10^{-3}}{(3-1)^2}$

$k = \frac{0.8 \times 10^{-3}}{(2)^2}$

$k = 0.2mA$

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Q.No	Marks

Q.No	Marks

Q.No	Ma

(ESTD-1995)

$V_{GS} = 2V$

$V_{DS} = 4.5V$

$$I_D = K \frac{W}{L} \left[(V_{GS} - V_t) - \frac{V_{DS}}{2} \right] V_{DS}$$

$$= 0.2 \times 10^{-3} \left[(2-1) - \frac{4.5}{2} \right] 4.5$$

$$= [0.2 \times 10^{-3}] \left[1 - \frac{4.5}{2} \right] 4.5$$

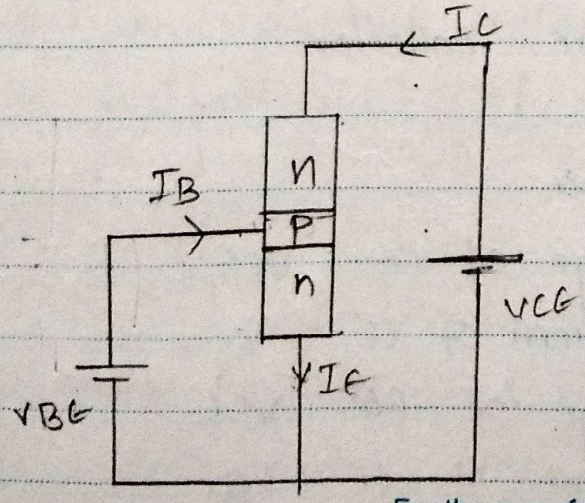
$$= 0.2 \times 10^{-3} [-1.25] 4.5)$$

$$\Rightarrow -1.25 \times 10^{-3}$$

$$\Rightarrow -1.25 \text{ mA} //.$$

4)a)

Common Emitter Configuration.



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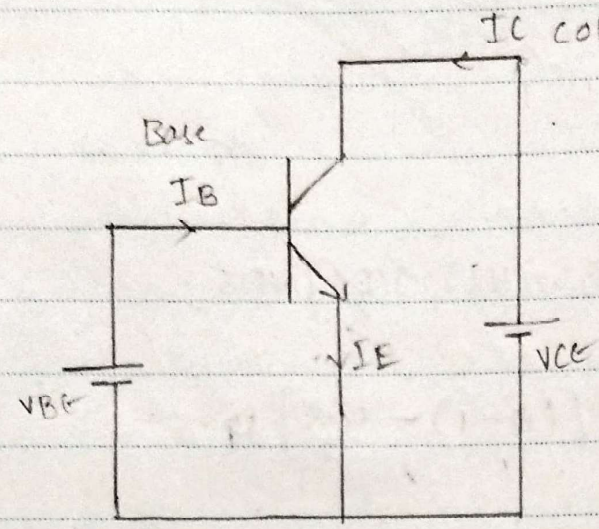
Q.No	Marks
7b	5

Q.No	Marks

Q.No	Marks



The output V I Characteristics of common Emitter Configuration

In common Emitter configuration Base is input and collector is output and the Emitter is common for both the Base and the collector.

Output characteristics

Out put voltage of CE = VCE

Output current of CE = IC

Input voltage of CE = VBE

Input current of CE = IB

Q.No	Marks

For the use of Evaluator Only

Q.No	Marks
4a.	

Q.No	Marks

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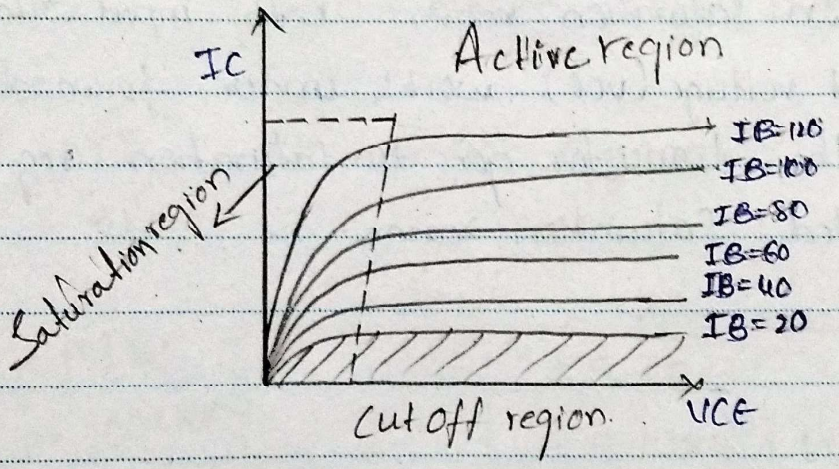
Output characteristics

Output characteristics are drawn by the ratio of output current (Ic) and output voltage (VCE) by keeping input current as a constant (IB).



Cut off region:-

In cutoff region both the input voltage (VBE) and output voltage (VCE) works under the reverse bias it is called cut off region.

Active region:-

In active region input voltage (VBE) works under input forward bias and output voltage (VCE) works under reverse bias then the transistors goes

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Q.No	Marks
49	6

Q.No	Marks

Q.No	Marks

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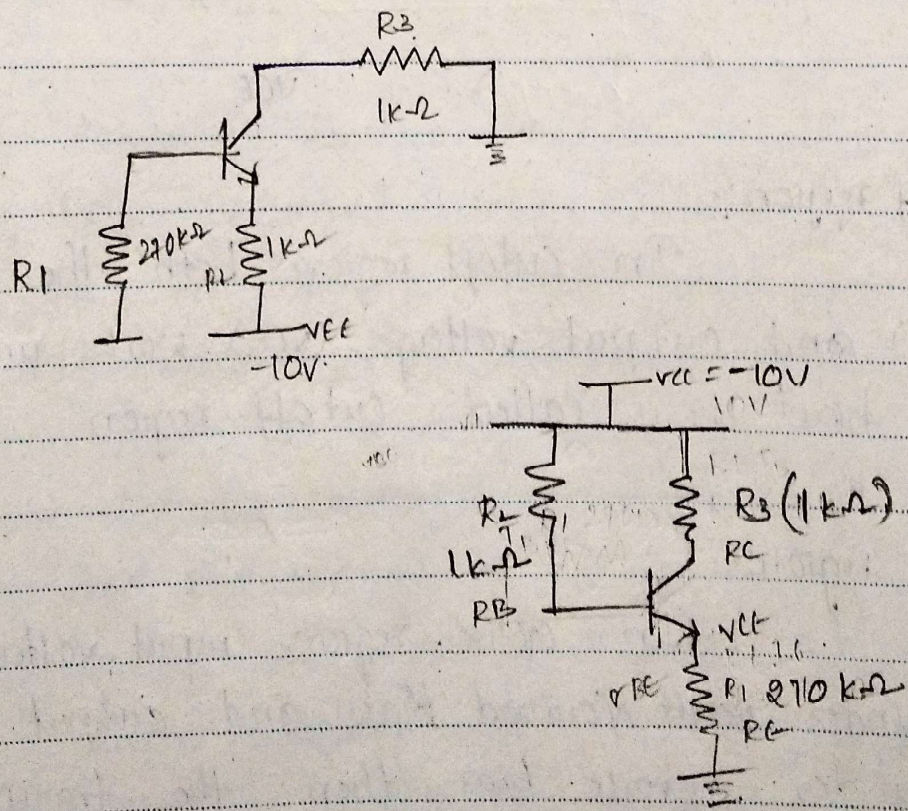
to active region it is called active region.

$$\beta = \frac{I_C}{I_B}$$

Saturation region:-

In saturation region both input voltage (V_{BE}) and output voltage (V_{CE}) works under forward bias condition the transistor goes to saturation region then it is called saturation reason.

4b)



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Q.No	Marks

Q.No	Marks

Q.No	Mark

(ESTD-1995)

$-V_{CC} + I_C R_C + V_{CE} + I_E R_E$

$-V_{CC} + I_C R_C + V_{CE} + (I_B + I_C) R_E$

$-V_{CC} + I_C R_C + V_{CE} + I_B R_E + I_C R_E$

$-V_{CC} + I_C (R_C + R_E) + V_{CE} + I_B R_E$

$V_{CE} = V_{CC} - I_B R_E - I_C (R_C + R_E)$

$= -10 - 2\times10^{-3} - 2\times10^{5}(1\times10^{3} + 270\times10^{3})$

$I_E = I_B + I_C$ $\Rightarrow$ $-5\,\text{k}\Omega - 54200\times10^{9}$

$= 8\,\text{k}\Omega$

$I_C = \beta I_B$

$= 100 \times 2\times10^{-3}$

$\Rightarrow \boxed{2\times10^{5}}$

$I_E = I_B + I_C$

$= 1\times10^{3} + 1\times10^{3}$

$= 8\times10^{3}$.

$-V_{CC} + I_B R_B + V_{BE} + I_B R_E + I_C R_L$ $I_C = \beta I_B$

$I_B(R_B + R_E) = V_{CC} - V_{BE} - I_C R_C$ $= 100 \times 2\times10^{3}$

$\boxed{I_B = \dfrac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E}}$ $\Rightarrow 200\times10^{3}$

$= 2\times10^{5}$

$V_{CE} = V_C - V_E$

$V_{CE} = -54200\times10^{9}$

$I_B = -V_{CC} + R_B I_B + V_{BE} + R_E I_C$

$-V_{CC} + I_B R_B + V_{BE} + (I_B + I_C) R_E$

$I_B = (V_{CC} - V_{BE}$

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Q.No	Marks
95	5

Q.No	Marks

Q.No	Marks

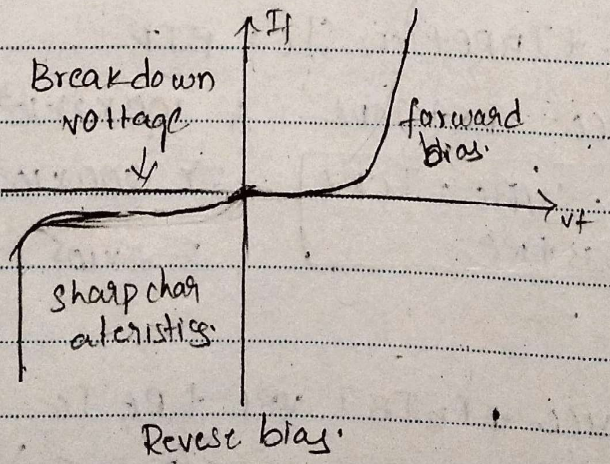
(ESTD-1995)

1a) Different rectifiers

① Half wave rectifier
② full wave rectifier
③ Bride wave rectifier.

1b) Zener break down.

When the reverse voltage is less than 0.6 ev then the due to heavy dopping region the depletion region get narrow position and the junction get breakdown and sudden flow of current take through diode these mechanism is called Zener break down mechanism.



Q.No	Marks
1a	2

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Q.No	Marks
1b	2

Q.No	Mar

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d) The given data,

reverse gate voltage = 12V

gate current = 1nA = 1×10^{-9}

$$R = \frac{V}{I}$$

$$R = \frac{12}{1 \times 10^{-9}}$$

$$= 12 \times 10^{9} \Omega$$

e) The three regions that present in drain source characteristics of JFET

* ohmic region
* Saturation region
* Cut off region.

f) Given data

$\alpha = 0.96$

$I_E = 10\ mA$

$I_C = ?$

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Q.No	Marks
12	2

Q.No	Marks
12	2

Q.No	Marks

(ESTD 1995)

$$\alpha = \frac{I_C}{I_E}$$

$$0.96 = \frac{I_C}{10 \times 10^3}$$

$$0.96 \times 10 \times 10^3 = I_C$$

$$I_C = 9.6\text{mA}.$$

g) Transform utilization factor.

Transform utilization factor is the ratio between power of dc component and the ac component rated to the transform it is called as Transform utilization factor.

$$T_f = \frac{P_{dc}}{P_{ac\ (rated)}} \times 100.$$

c) input impedence is the reverse voltage given to the circuit. In JFET has high low input impedence when compared to MOSFET.

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Q.No	Marks
1C	6

Q.No	Marks
1F	2

Q.No	Mar
19	2

(ESTD-1995)

5a) Given data.

$I_O = 7.5\ \mu A$ for $300^\circ K$ temperature.

$I_O = ?$ for 400^K temperature.

$$I = I_O\left[e^{V/\eta V_T} - 1\right]$$

$$= \frac{\eta V_T}{I_O}$$

$$= \frac{2 \times 25.6 \times 10^{-3}}{7.5 \times 10^{-6}}$$

$$I \Rightarrow 6.8\ kA$$

5b) Avalance breakdown mechanism

When the reverse voltage is greater than 0.6ev. then freely excited charge carriers are gain the thermal energy and create a new charge carriers these new charge carriers are collaid with the

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Q.No	Marks
5a	2

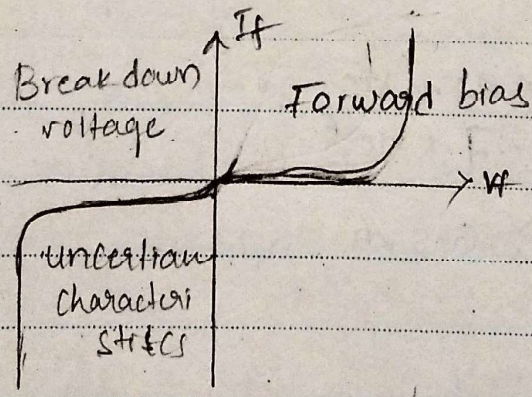
Q.No	Marks

Q.No	Marks

(ESTD-1995)

im mobile ions and again generates the energy the charge carries take energy and again colloids with im mobile ions and generate the newly charged carries it is called multiple charge carrirs process and at some point

Due to high heat (or) energy the depletion Junction may breakdown and then current flows suddenly into the diode these mechanism is called avalance breakdown.



Ratio of Avalanche breakdown = 11:10

Zener break down

when reverse voltage is less than 0.6 ev then the due to heaverly dopped region

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Q.No	Marks

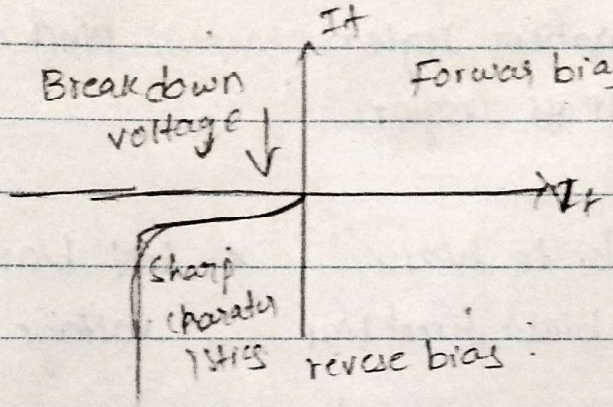
Q.No	Marks
5b	9

Q.No	Marks

(ESTD-1995)

the depletion layer get narrow and the junction breaks then a sudden flow of current occur in the diode.

The ratio of zenos breakdown = $10^{\%0}$



6a)

Comparision

	BJT	JFET
Sp Defination	Bipolar Junction Transistor	Junction field effect Transistor
Input resistance	* Input resistance is less	* Input resistance large

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Q.No	Marks
6a	4

Q.No	Marks

Q.No	Marks

(ESTD-1995)

Input current	* The input current mA	* The input current μA
Region	* active region saturation region. cutt off region.	* ohmic region * pinch off region.
Bias	Collector to bias, self bias, fixed bias	* self bias (or) voltage divider bias.
Device.	Current control device	voltage controled device.
Terminal.	Base, emitter, collector	Gate, Drain, source.
Thermal runaway.	Thermal run away is high	No thermal runaway

* FET (Field effect transistor) is used as switch
* used in the electrical device
* used to control the speed of the devices.

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Q.No	Marks

Q.No	Marks

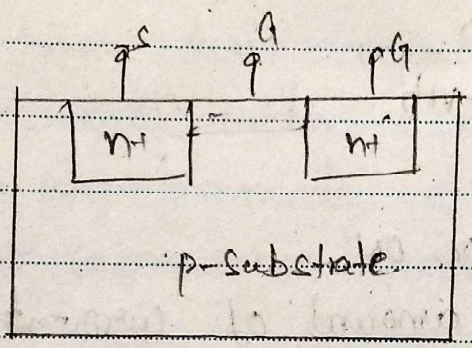
Q.No	Marks

(ESTD-1995)

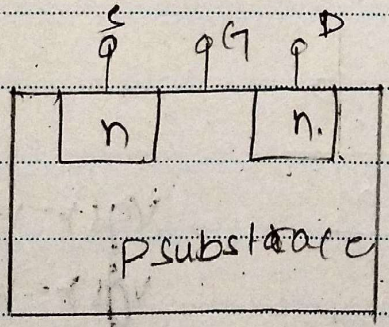
(6b)

Enchancement Mosfet

⇒ If they won't be any channel exist between drain and source it is called enhancement mosfet



Enhancement MosfET



$V_{GS} = 0$

$V_{DS} = 0$

transistor ON

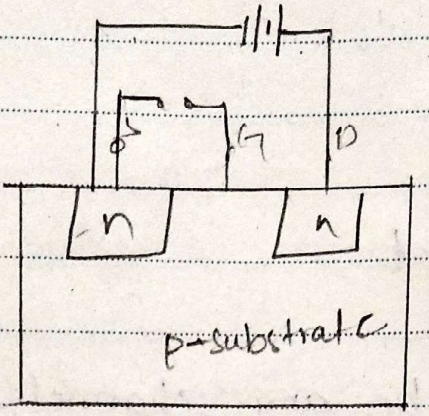
NO current flows through transistor

For the use of Evaluator Only

Q.No	Marks

Q.No	Marks

Q.No	Marks

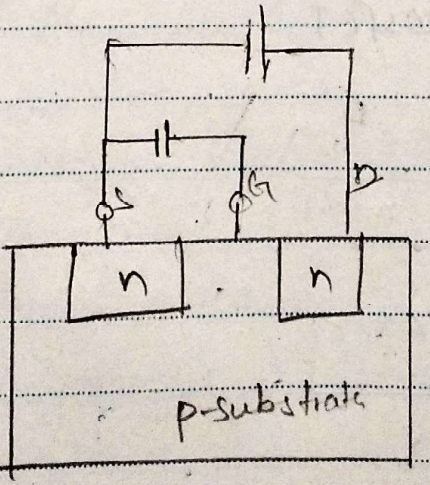


$V_{GS} = 0$

$V_{ds} > -V_{th}$

Transistor ON

small amount of current flows through the transistor.



$V_{GS} > -V_{th}$

$V_{ds} > -V_{th}$

Transistor is off

NO current

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Q.No	Marks

Q.No	Marks
26	2

Q.No	Ma

(ESTD-1995)

MOSFET

* Metal oxide semiconductor Field Effect transistor
* MOSFET unipolar device
* MOSFET does not have Junction
* MOSFET have high input imbedence
* MOSFET works under 2 modes
  - ⇒ Depletion mode
  - ⇒ Enchancement mode

For the use of Evaluator Only

Q.No	Marks

Q.No	Marks

Q.No	Marks

(ESTD-1995)

For the use of Evaluator Only

Q.No	Marks

Q.No	Marks

Q.No	Mar

UNIT-1

Semiconductor Diode

All the materials are composed of very small particles (atoms).

According to arrangement of atoms in materials, materials are divided into two types 1) Solids 2) Crystals.

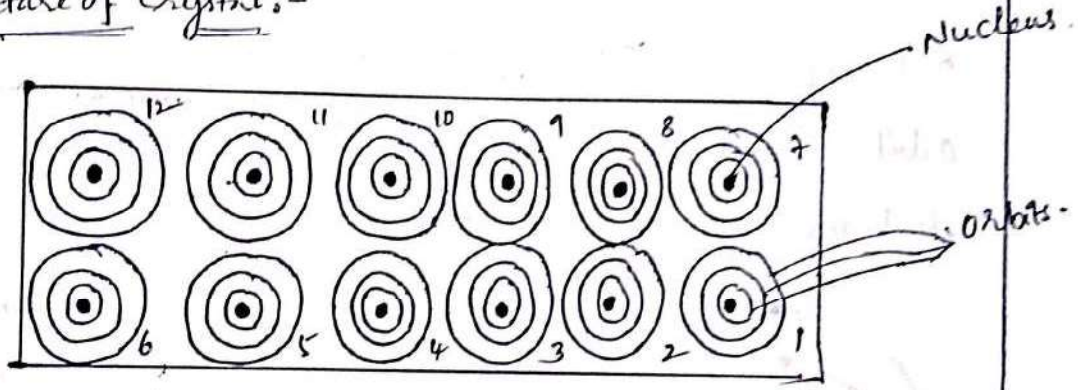
Solids :-

In Solids random arrangement of atoms are present.

Crystal :-

In crystals regular arrangement of atoms are present.

Structure of Crystal :-



Let us take one atom as reference ▶

In atoms, one nucleus is there, around the nucleus electrons are moving in different orbits.

In nucleus two types of particles are there

a) protons - protons are having +ve Charge

b) Neutrons - having no charge.

Total no. of protons = Total no. of electrons in any atom

∴ Total +ve Charge = Total -ve Charge

So that atom is said to be electrically neutral.

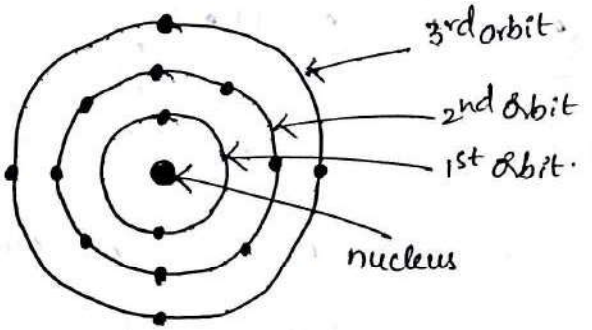
Valence electrons:-

In atoms, outermost orbital electrons are called valence electrons. This valence electrons of all atoms are electro statically interact with each other. Inner cells are uneffected.

Let us take Silicon atom as reference;

atomic number of Silicon is 14 : $1s^2 2s^2 2p^6 3s^2 3p^2$

Silicon atom having 3 orbits. In first orbit 2 electrons are rotating arounding the nucleus. In Second orbit 8 electrons are rotating around the nucleus. In third orbit 4 electrons are rotating around the nucleus. Here 3rd orbit is the outermost orbit. Electrons rotating in this orbit are called as valence electrons. So, here 4 electrons are valence electrons.



- Outermost orbital electrons are lossly attached with nucleus.
- Inner orbital electrons are tightly attached with nucleus.

All rotating electrons are having the same energy. Here energy is directly proportional to $\frac{-1}{n^2}$

$E \propto \frac{-1}{n^2}$ where E is energy

n is orbit number

When $n=1$ $E \propto -1$ $n=2$ $E \propto -0.25$ $n=3$ $E \propto -0.1$

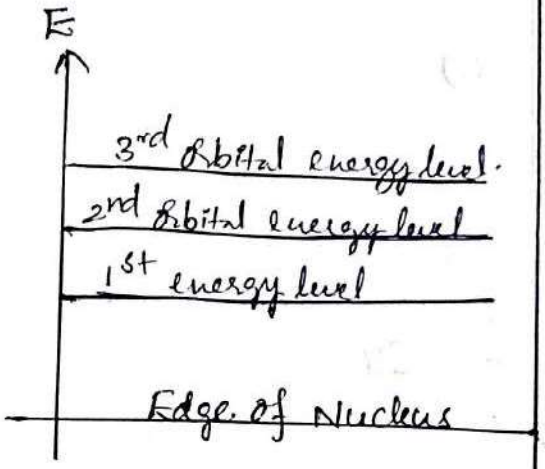
From above numericals we are concluded that outer most electrons are having very high energy.

Let E_1 is the 1st Orbital energy

E_2 is the 2nd Orbital energy

E_3 is the 3rd Orbital energy

$\therefore E_1 < E_2 < E_3$



* Inner Orbitals are having less energy and outermost Orbit are having higher energy.

When energy (Thermal energy or electrical energy) is given to first Orbital electron, So electrons are initially at exitation state, when ever Sufficient energy is given to 1st electrons, this electrons are able to move next orbit, Similarly outermost Orbital electrons are free from the nucleus attachment.

So that energy increases, free electrons are increases When free electrons increases Conductivity increases.

Free electrons:-

When energy is given to the Valence electrons, this electrons are free from the nucleus attachment, that electrons are called "free electrons".

According to no. of free electrons, material are divided as Conductors, Semiconductors, and Insulators and defined as

a) Conductors :-

Conductors is a substance, which has large number of free electrons at room temperature.

b) Semiconductors :-

Semiconductor is a substance, which has moderate free electrons at room temperature.

c) Insulator :-

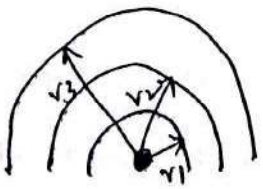
Insulator is a substance, which has practicaly no free electrons at room temperature.

Covalent bond :-

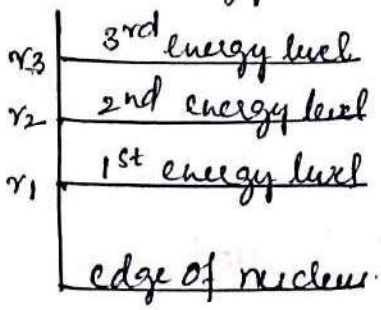
~~When~~ Sharing of energy when electrons are sharing the energy between neighbouring atoms, some bond is created that bond is called "Covalent bond".

Energy Bands :-

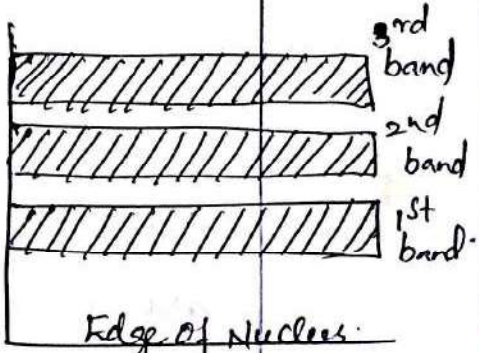
The range of energies contained by an electron in a material is known as energy band.



Fig(1).



Fig(2)



Fig(3).

The concept of energy band can be easily understood by reffering Figs. Fig(2) shows the energy levels of single

isolated atom of Silicon. Each orbit of atom having a single energy. Therefore, an electron can have only single energy. Therefore an electron can have only single energy corresponding to the orbit in which it exists.

However, when atom is in material, the electron in any orbit can have range of energies. For instance, electrons in first orbit have slightly different energies because no two electrons in this orbit having no same energy since there are millions of first orbit electrons the slightly different energy levels form a band.

Individual energy levels of an isolated atoms are converted into corresponding "bands" when atom is in material.

Energy Bands are classified into the following types:-

1) Valence Band
2) Conduction Band
3) Forbidden Energy gap.

1) Valence Band:-

In range of energies (i.e Band) contained by valence electrons is known as valence band. The electrons in the outermost orbit of an atom are known as valence electrons.

This Band may be completly or partially filled.

(2) Conduction Band :-

The certain materials, the valence electrons are loosly attached to the nucleus at ordinary temperature. Some of the "valence electrons" may get detached to become "free electrons".

This free electrons which are responsible for the conduction of current in a conductor. For this reason, they are called "conduction electrons".

* The range of energies (Band) possessed by conduction electrons is known as "conduction Band".

All electrons in conduction band are free electrons.

(3) Forbidden Energy gap :-

The seperation between conduction band and Valence band on the energy level diagram is known as "forbidden energy gap".

The greater energy gap, indicates more tightly the valence electrons are attached to the nucleus. In order to push the electron from valence band to the conduction band (i.e to make the valence electron free), external energy equal to the forbidden energy gap must be supplied.

* Forbidden energy gap is decreases with increase in temperature.

Classification of materials on the bases of energy band diagram :-

1) Insulators
2) Conductors
3) Semiconductors.

1) Insulators:-

Eg: Wood, Glass

Initialy valence band is full and conduction band is empty. And energy gap between conduction band and valence band is very high i.e nearly equal to 6ev. So that the very high energy is required to move electron from valence band to conduction band. So that for insulators conductivity is very less ($\simeq$ zero), resistivity is very high ($\simeq \alpha$).

So Insulators are not allow the passage of electric current through them.

But at very very high very temperature, Some electrons are enter into conduction band, that means conductivity is increases (but that conductivity is very less). When conductivity increases resistance decrease.

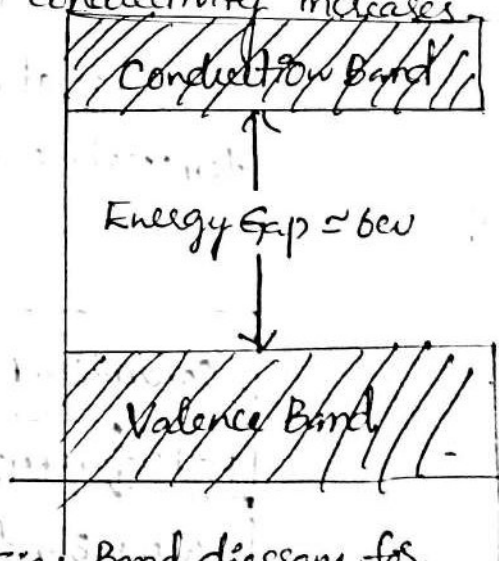


Fig: Band diagram for Insulators.

2) Conductors:-

Eg:- Coppers, Alluminium, iron etc.

Conductors are easily allow the passage of electric current through them.

Because there are large number of free electrons available in conduction Band, that means conductivity is very high ($\simeq \alpha$), resistivity is very less ($\simeq 0$).

In energy Band diagram conduction band and valence band is overlapping as shown in below Fig.

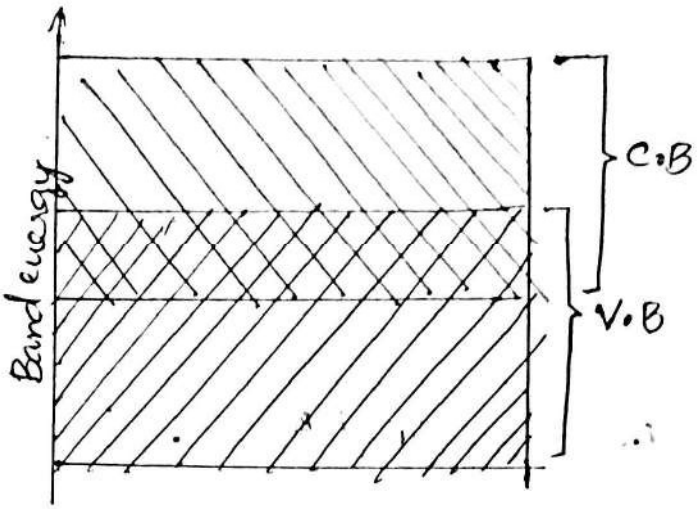


Fig: Energy Band diagram of Conductors.

3) Semiconductors:-

Eg: Carbon, Germanium, Silicon etc.

Semiconductors are those substances whose ~~electrically~~ Conductivity is lies between conductors and insulators.

In Semiconductors initialy (or at 0°c) having

i) Empty conduction band

ii) Full valence band.

So that at 0°c, Semiconductor acts as a Insulator. At room temperature some valence electrons are able to go conduction band, because energy gap between valence band and conduction band is very small (≃1ev). So that from that room temperature onwards Semi conductor acts as a conductor. But conductivity is small at room temperature.

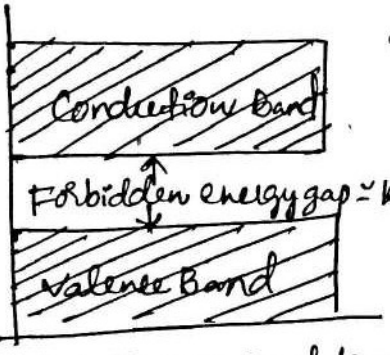


Fig: Energy Band diagram of Semiconductors.

When temperature increases no. of valence electrons are move to the conduction band is increases, i.e Conductivity increases. When Conductivity increases resistivity decreases. When temperature increases, free electrons in conduction band increases, so Conductivity increases.

Semiconductors Energy Gap:-

Carbon (06) ≃ 5ev

Silicon (14) ≃ 1.21ev

Germanium (32) ≃ 0.785ev

Thats why Semi conductors are called as Negative temperature Co-efficiant (i.e When temperature increases, Resistivity decreased)-

Carbon is normally not proffered as Semiconductor, Why because energy Gap is max.

Semiconductors are two types:-

1) Intrinsic Semi conductors
2) Extrinsic Semi conductors.

1) Intrinsic Semiconductors:-

A Semiconductor is an extremly pure form is known as intrinsic Semiconductors.

In an Intrinsic Semiconductor, at room temperature, electron-hole pairs are created. when an electric field applied across an intrinsic Semiconductor. The current conduction due to two process namely by 1) Free electrons 2) Holes.

Here number of holes = number of free electrons.

$$p = n = n_i$$

Where 'p' is Concentration of holes (no of holes / unit volume).

'n' is Concentration of electrons (no of e^-s / unit volume).

Where n_i is the intrinsic concentration.

$$\boxed{n \cdot p = n_i^2} \quad \text{--- (1)}$$

eqn(1) called as mass action law.

$n_i = 2.5 \times 10^{13}$ for Ge

$n_i = 1.5 \times 10^{10}$ for Si.

* Definition of Hole:-

Absence of the electron in Covalent Bond is called as "Hole".

2) Extrinsic Semiconductors:-

At room temperature, pure Semiconductor having poor conductivity. So, to increase the conductivity of pure Semiconductor at room temperature, we are adding small amount of impurities to the Intrinsic Semiconductor.

This process of adding impurities called as "Dopping". Based on dopping, Extrinsic Semiconductors are divided into two types

1) n-type Semiconductor
2) p-type Semiconductor.

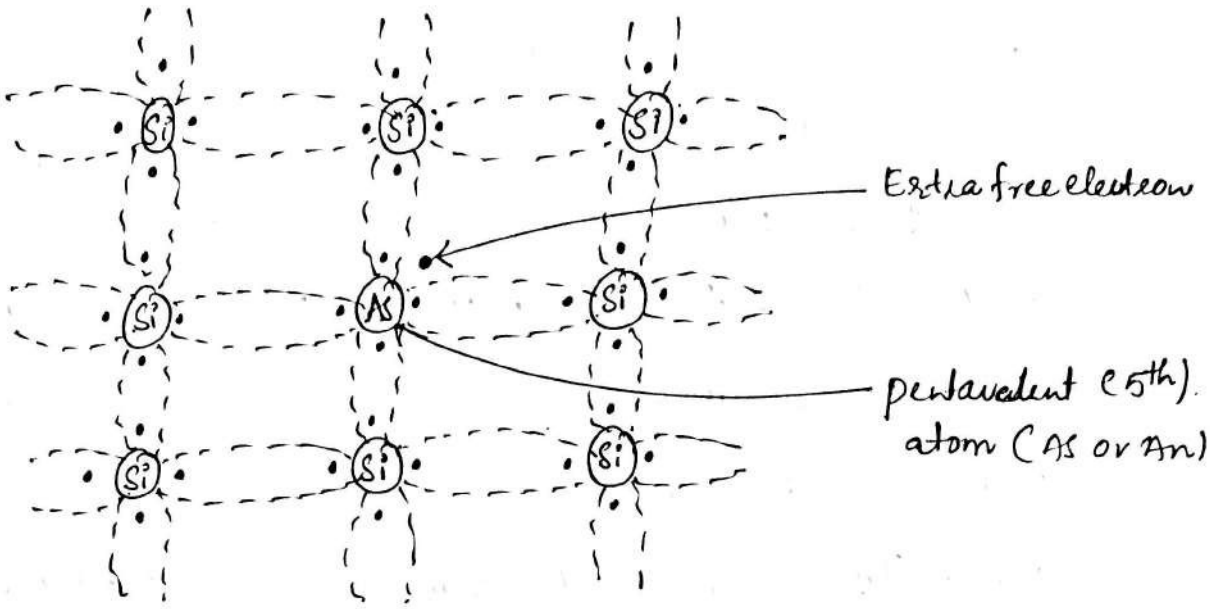
1) n-type Semiconductors:-

When small amount of pentavalent impurities (5th group is added to the pure Semiconductor, it is known as "n type" extrinsic Semiconductors.

pentavalent impurities are having 5 electrons in outermost orbit. In pure Semiconductor eg: Si or Ge, these are having 4 electrons in outermost orbit.

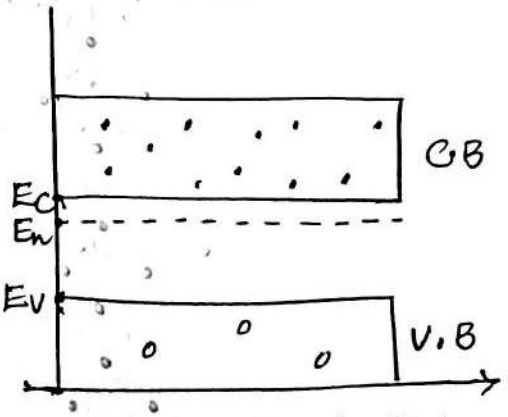
If Arsenic (atomic no: 33 i.e $1s^2 2s^2 2p^6 3s^2 3p^6 3d^{10} 4s^2 4p^3$) or antimony (atomic no: 51) is added to pure Semiconductor (which are having 4 electrons in outermost orbit). So 4 of 5 valence electrons of arsenic atom forms Covalent bond with 4 neighbouring electrons of Ge or Si atoms as shown in below Fig. So fifth valence electron of Arsenic atom has no place in covalent bonds. Therefore extra free electrons is provided in the n-type Semiconductor.

* pentavalent impurities are called "Donar impurities" because they are able to donate (or give) extra electron to Semiconductor.



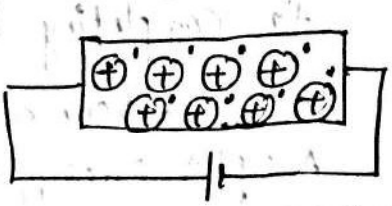
When donar impurities are added to a Semiconductor donor energy level is introduced just below the conduction band. Because the energy required to detach the fifth of electron from the "As" atom is very small i.e 0.01ev for Ge and 0.05ev for Si.

- At room temp, almost all the fifth electrons of donar are pushed into conduction band.
- In n-type Semiconductor, electrons are said to be "majority carriers" because in number electrons are high in conduction band. Holes are "minority carriers" because in number, holes are less.



n-type conductivity :-

The current conduction in an n-type Semiconductor is predominatly by free electrons i.e negative charges and is called n type or electron type conductivity.



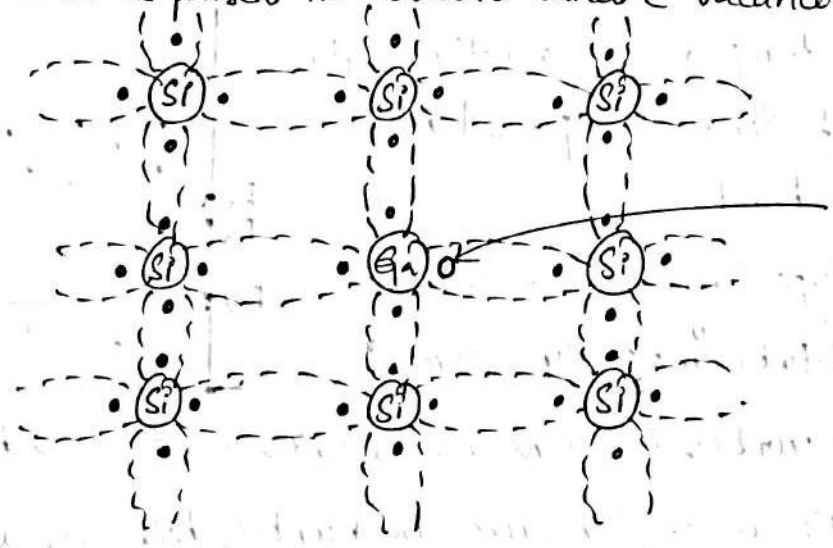
P-type Semiconductor :-

When a small amount of trivalent impurities (or 3rd group) is added to a pure semiconductor, and it is called p-type semiconductors.

Trivalent impurities are Ga(31), Indium(49).

* Addition of trivalent impurities provide large no. of holes.

In Gallium, 3 electrons are present in outermost orbit. Where as Si (or) Ge are having 4 electrons are present in outermost orbit. If Gallium is dopped in Si (or) Ge substance, 3 electoons of "Ga" sharing the energy with 3 electrons out of 4 electrons of Si as shown in Fig. So electron of Si atom doesn't having any further electron in Ga to form the covalent band, so one vacance is present in covalent band (vacance refered as Hole).

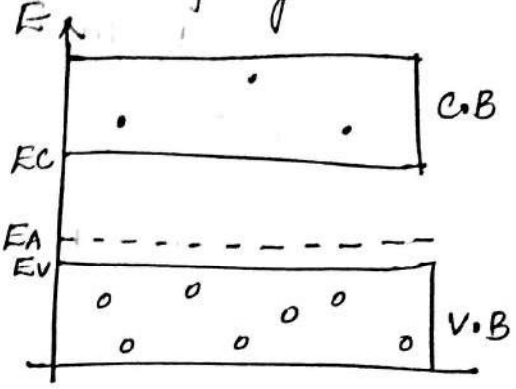


∴ For each Ga atom is added, one hole (vacance) is created. These trivalent impurities are called "Acceptor impurities". Because impurities atoms are accepting electrons for completing the covalent bond.

When acceptor impurities are added to a semiconductor Acceptor energy level introduced just above the valence Band.

Because a small amount of energy required for an electron to leave the valance band and accept the accept energy level.

In p-type Semiconductor, holes are "majority" and e's are "minority" carries.



Currents in Semiconductors:-

Currents in a Semiconductor due to "holes" and "electrons". This currents are two types 1) Drift current

2) Diffusion current.

1) Drift current:-

current due to applied potential:

current $I = \frac{Nq}{t}$ ——(1)

relation between velocity and Time is given by

Velocity $v = \frac{L}{t}$ ——(2) $\Rightarrow t = \frac{L}{v}$ ——(3)

Sub eqn(3) in eqn(1)

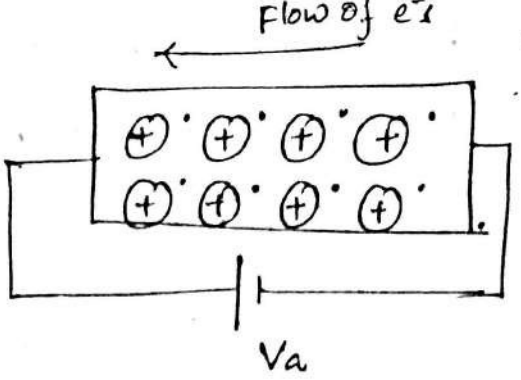
$\therefore I = \frac{Nqv}{L}$

current density $J = \frac{\text{current}}{\text{unit area}}$

$J = \frac{I}{A} = \frac{Nqv}{LA}$ ——(4).

Where LA is volume of Specimen.

$\frac{N}{LA}$ is concentration and it indicated as 'n'



$\therefore J = nqv$ — (5)

But $v \propto E$

$v = \mu E$ — (6)

$\therefore J = nq\mu E$ — (7)

Where n : Concentration of carriers

q : Charge of carriers

μ : mobility of carriers

E : applied Electric field.

For holes current density $J_p = nq\mu_p E$

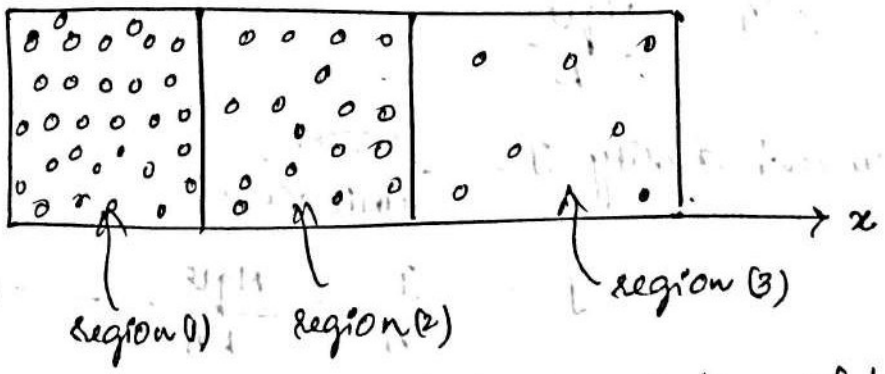
For electron current density $J_n = -nq\mu_n E$

$\therefore$ Total Drift current density $J_T = J_p + J_n$

$$\boxed{J_T = nq\mu_p E - nq\mu_n E}$$

2) Diffusion current:-

As shown in below fig, Let the concentration of free holes is not uniform in the x-direction.

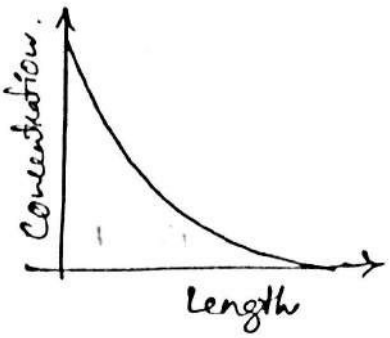


Where region (1) is having high concentration of holes.

region (2) is having medium concentration of holes.

region (3) is having Low concentration of holes.

And this represented in graph between hole concentration and distance as shown in below.



Let the rate of change of concentration

$$\frac{dp}{dx}$$

Since the concentration of holes is more in region (1) compare to region (2) and (3).

In general greater concentration carriers are move towards the area of lower concentration. So here holes are moving from area (1) to area (2) and area (3). In this situation, with out applying any voltage, the charge carriers are flowing which resulting in current flow.

This current will be more, if the rate of change of concentration is more. So that diffusion current is directly proportional to concentration gradient.

$$J_p \propto \frac{-qdp}{dx}$$ (here -ve sign indicates concentration is decreases w.r.t 'x').

$$J_p = qD_p\left[\frac{-dp}{dx}\right]$$

$$J_p = -qD_p\frac{dp}{dx} \quad \text{——— (1)}$$

where D_p is the diffusion constant for holes

q is the charge of holes i.e +ve charge.

Same phenomina applicable for electrons also.

$$J_n = qD_n\frac{dn}{dx} \quad \text{——— (2)}$$

Total diffusion current = $J_p + J_n$

$$\boxed{J_T = -qD_p\frac{dp}{dx} + qD_n\frac{dn}{dx}}$$

Junction formation (or) Junction construction:-

P-N Junction diode can be constructed by different methods they are 1) Alloy Junction
2) Grown Junction.

1) Alloy Junction:-

In this method, small block of trivalent impurities is placed on a n-type slab as shown in below Fig (1)(a).

The system is then heated to temperature of about 500°C. The Indium (trivalent impurities) and n-type are melted (i.e converted into liquid form) at that point Indium is placed into or inserted into n-type slab. This shown in Fig (1)(b).

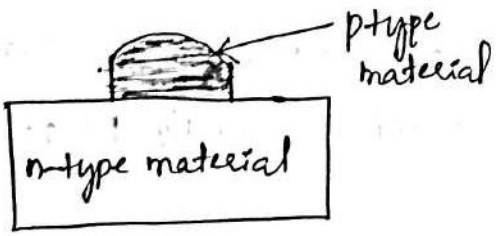


Fig (1)(a)

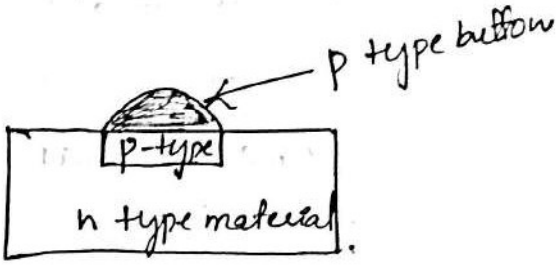


Fig (1) (b)

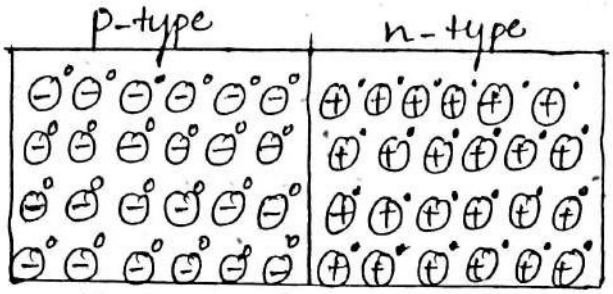
The temperature is then lowered and liquid begin to solidify. So under proper conditions, the atoms of Indium impurity will be suitably adjusted in the n-type slab to form a single crystal. The addition of Indium over comes the excess of e⁻s in the n-type to an extent that it creates a p-type region.

2) Grown Junction :-

In Grown Junction, we are taking pure Semiconductor Ge (or) Si, on that Semiconductor half of the material is dopped with p-type and half of the material is dopped with n-type.

Open circuited p-N Junction formation :-

In pure Semiconductor, half of that material dopped with p-type materials and remaining half of the material is dopped with n-type materials.



Let initialy no. of e's = no. of holes = x.

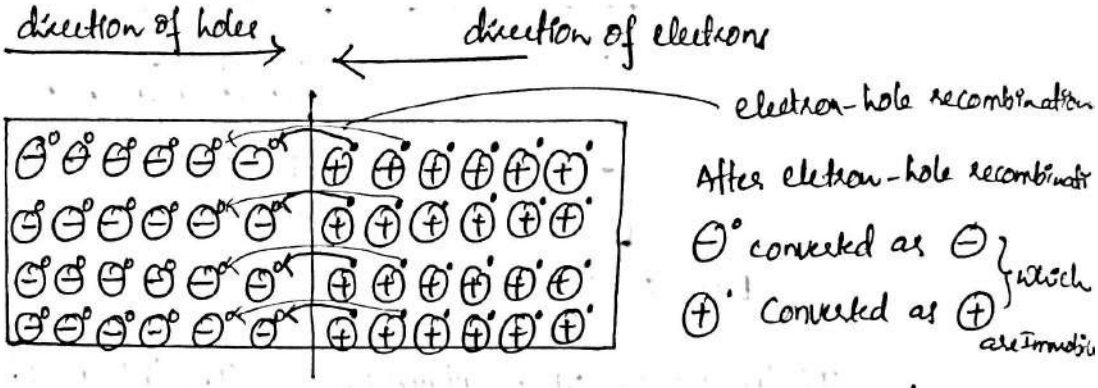
If 'n' no. of p type atoms are dopped to the pure Semiconductor
The Total no. of holes in p region becomes = x+n
Total no. of electrons in p region = x

If 'n' no of n type atoms are dopped to the pure Semiconductor
The Total no. of electrons in 'n' region becomes = x+n
Total no. of holes in 'n' region becomes = x.

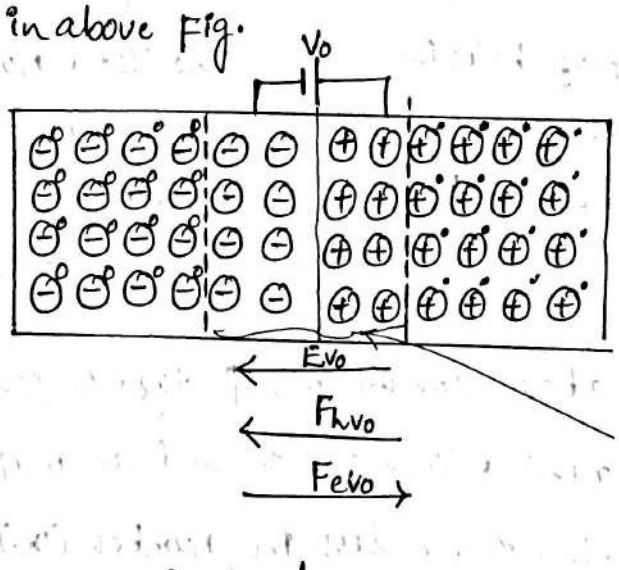
In above conditions, p-type region having the more no of holes (x+n) which are treated as majority Charge carriers, where as electron are less in number (x) which are treated as minority charge carriers. Similarly, In n-type region, electrons are majority (x+n) charge carriers and holes are minority charge carriers. Therefore Concentration gradient is exist with electrons and holes. So Higher Concentration Charge carriers are move toward lower concentration charge carriers, i.e electrons are move from n type to p type and holes are move from p type to n type. In that process p type atom accept one electron and aquire -ve charge, n type atom donate one electron and aquire

+ve charge and both atoms are becomes Immobile.

Dute to the damation of Immobile atoms, Some potential i.e in p type region -ve potential and in n-type region +ve potential is developed. That potential developed Sufficient Electric field to stop the further flow of charge carriers as shown in below Figures.



Due to the concentration gradient direction of electrons and holes are shown in above Fig.



Due to Vo, Force developed on electrons and ~~Barrier~~ holes are shown in above, if we observe the direction of electrons and holes in both figures, it is clear that, if Vo develops the Sufficient Electric field, that electric field stops the further flow.

Charge distribution with in the Junction can be explained with the help of poissons equation.

$$\frac{d^2V}{dx^2} = \frac{-\rho_v}{\epsilon}$$

Where ρ_v is volume charge density
ϵ permitivity of the medium
V: potential
x: is the distance from the Junction.

Charge distribution with in the Junction :-

Charge distribution with in the Junction can be explained with the help of poisson's equation.

$$\frac{d^2V}{dx^2} = \frac{-\rho_e}{\epsilon} \quad i.e \quad \frac{-d^2V}{dx^2} = \frac{\rho_e}{\epsilon} \cdot \text{—— (1)}$$

Where ρ_e and ϵ are constant, for analysis $\frac{\rho_e}{\epsilon}$ is treated as constant a.

$$\frac{-d^2V}{dx^2} = \frac{\rho_e}{\epsilon} = a. \text{—— (2)}$$

by apply the integration

$$\frac{-dV}{dx} = ax \text{ — (3)}$$

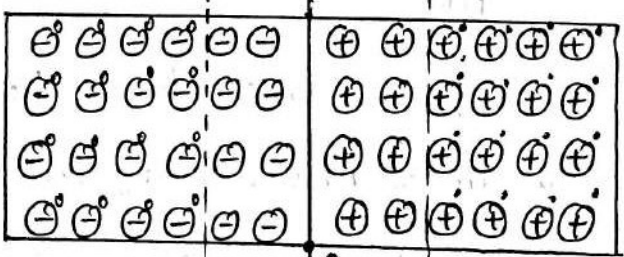
where $\frac{-dV}{dx} = E = ax$ — (4)

apply the integration for equ (3)

$$-V = \int ax = \frac{ax^2}{2}$$

$$V = -\int ax\,dx$$

voltage $V = -\int E\,dx$ [from eqn (4)]



Fig(a) $\frac{-d^2V}{dx^2} = \frac{\rho}{\epsilon} = a$

Fig(b) $\frac{-dV}{dx} = E$

Fig(c) $V = -\int E\,dx$.

Biasing:-

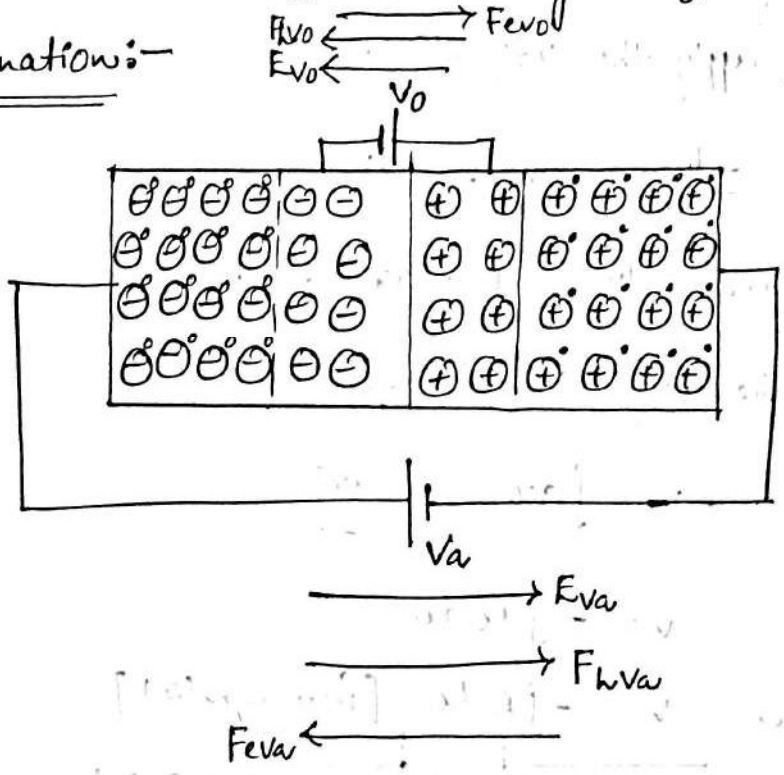
In p-n junction diode Two types of biasing techniques are present 1) Forward Bias

2) Reverse Bias.

1) Forward Bias:-

Defination:- When High potential is connected to 'P' type and Lower potential is connected to 'n' type, then majority charge carriers are crosses the junction which resulting in high current.

Explanation:-

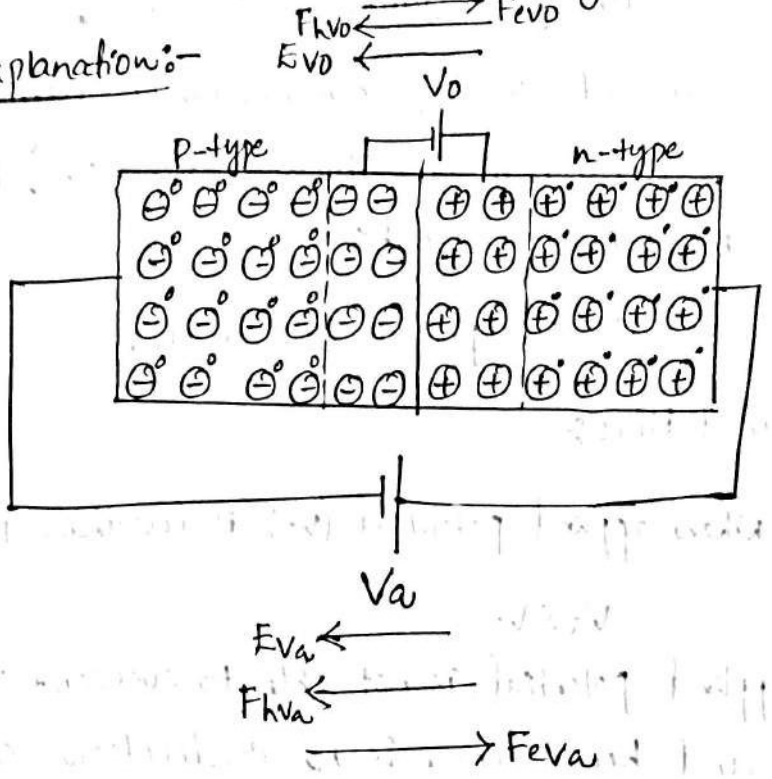


In above figure, FORCE direction due to the applied potential (V_a) and force direction due to barrier voltage (V_o) is opposite to each other. When $V_a \leq V_o$, majority charge carrier are opposed by the barrier voltage, so no current flows. When $V_a > V_o$ then majority charge carriers are cross the junction which resulting in high current. In Forward bias, junction width is ~~decrease~~ decreases as applied voltage (V_a) increases.

2) Rwese Bias :- (2)

Defination :- When Higher potential is connected to 'n' type and Lower potential is connected to 'p' type, then majority charge carriers are move above away from the junction, and only minority charge carriers are move towards the junction which resulting in small current towards junction.

Explanation :-



Majority carries move away from the junction, because holes are +ve, so that holes are attracted towards -ve terminals. Electrons are -ve charged particles, so that es are attracted towards +ve terminals. In above Fig, force direction due to junction potential (Vo) and force direction due to applied potential (Va) on carriers are same.

Conclusions from Biasing :-

Fowaard Bias :-

1) majority carriers are moving towards junction when applied force is dominating the force due to the junctions, then all majority carriers are crossing junction that means junction is going to eliminate at particular applied potential.

So Junction width is decreases in forward bias.

2) In forward bias majority carriers are crossing the junction, so current flowing is maximum and resistance offered by the junction is minimum.

Reverse Bias:-

1) All majority carriers are moving away from the junction, so width of the junction increases,

2) Current flowing is minimum (only minority charge carriers are moving towards junction), i.e resistance is max in reverse bias.

V-I Characteristics of PN Junction diode:-

1) Forward Bias:-

a) When applied potential (V_a) is less than junction potential:-

$V_a \leq V_0$.

Applied potential is not able to overcome the internal junction and hence there is no conduction so current is zero.

b) $V_0 < V_a < V_{sat}$:-

When V_a is greater than junction potential V_0 (normaly $V_0 = 0.6$ for Si, $V_0 = 0.3$ for Ge), from that potential onwards conduction starts, that potential where the conduction start called as "cutin voltage".

Here conduction is directly proportional to the potential energy that is energy developed due to applied voltage V_a. When applied voltage V_a increases, no of free carriers are emitted. Such emission is called as "primary emission".

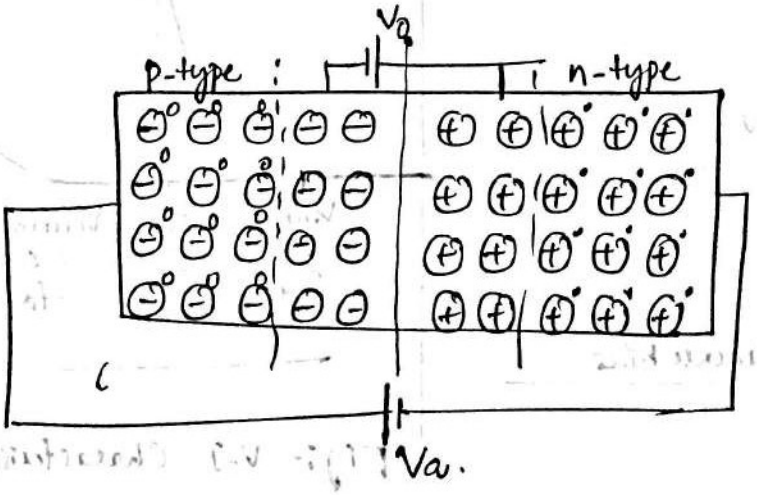
In this region for every change in voltage there is equal change in current.

c) $V_a > V_{sat}$:-

When applied potential is increases, the free carriers are generated is also increases. When keep on increasing the applied potential, very large amount of free carriers are emitted and they are moving towards junction, in that process "collisions" are taken place between the free carriers. Due to collisions, some amount of temperature is generated. That temperature provides thermal energy to the charge carriers, using thermal energy some charge carriers are becomes free, such emission is called as "Secondary emission".

In this process, when voltage increases, for primary emission, secondary emission is added, so no. of free charge carriers are drastically increases with respect to applied voltage. From that voltage onwards, small change in voltage caused to drastical change in current flow, that corresponding voltage called as "Saturation voltage".

Electrical connection for pN junction diode to observe the Forward biased V-I characteristics:-



2) Reverse Bias :-

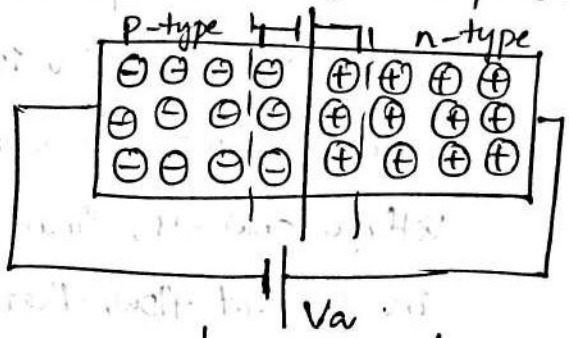
a) applied voltage (V_a) < Breakdown voltage (V_{BR}) :-

In Reverse bias, applied force is added to the force developed by junction voltage.

The applied voltage gives the emissions of free charge carriers, but it is very small because it is due to minority carriers at the order of micro amps for Ge, Nano amp for Si.

b) applied voltage (V_a) ≥ Breakdown voltage (V_{BR}) :-

The carriers that are emitted due to applied potential will collide and create secondary emission but that happens at very high voltage (>50V). At that high voltage, excess heat is developed due to collisions, that excess heat damages the pN junction diode.



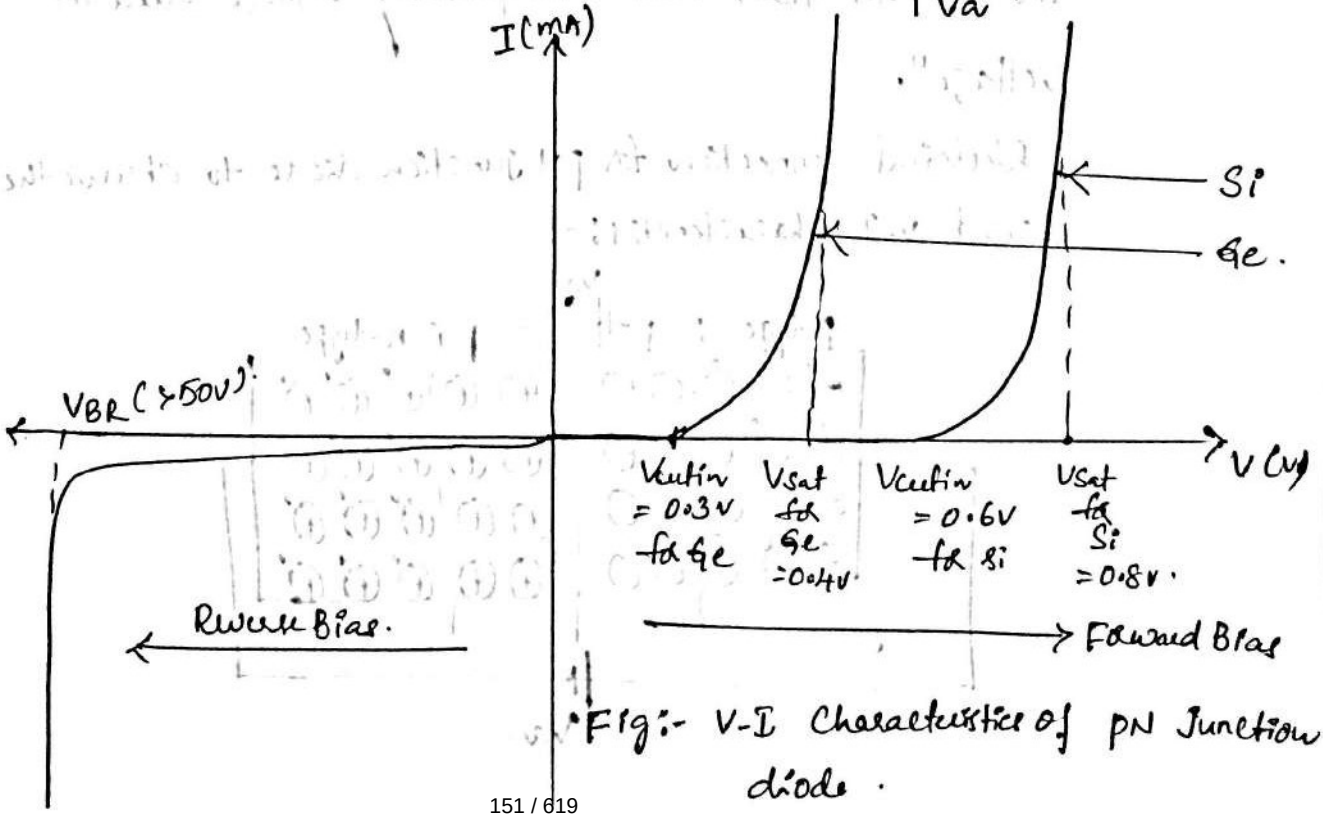
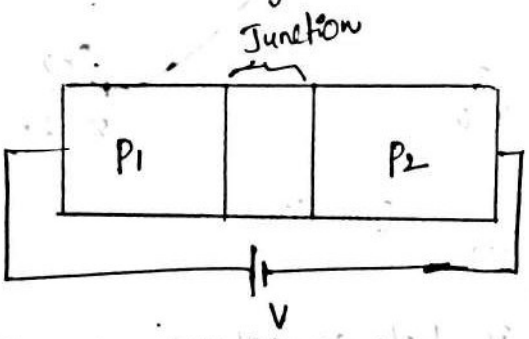


Fig:- V-I Characteristics of pN Junction diode.

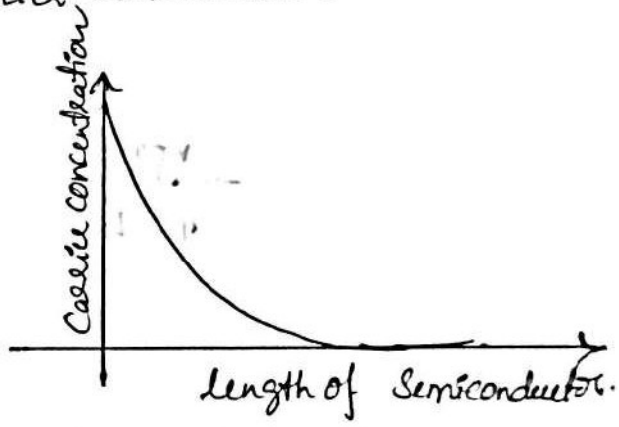
Type of PN Junction diode	Vcutin	Vcat	Reverse current	forbidden energy Gap	operating Temp	mobility of e⁻s (μ_n)	mobility of holes (μ_p)
Ge	0.3V	0.4V	1A	0.785eV	-65° to 75°C	3800	1800
Si	0.6V	0.8V	nA	1.21eV	-65° to 175°C	1300	500

Current equation of the P-N Junction diode :-

In Fig(a), where P_1 is carrier concentration of 1st region and P_2 is carrier concentration of 2nd region. Consider P_2 is low concentration compare to P_1. When ever potential is applied to the Semiconductor, at that instant carrier concentration is varies as shown in Fig(b).



Fig(a).



Fig(b).

Here Fig(b) says that whenever potential is applied at that instant, carrier concentration is high, nearer to the junction and carrier concentration is low faraway to the junction.

Low carrier concentration is expressed interms of high concentration as shown in below

Law of Junction $\Rightarrow P_2 = P_1 e^{-V/V_T}$ ——(1)

where P_2 = Low concentration

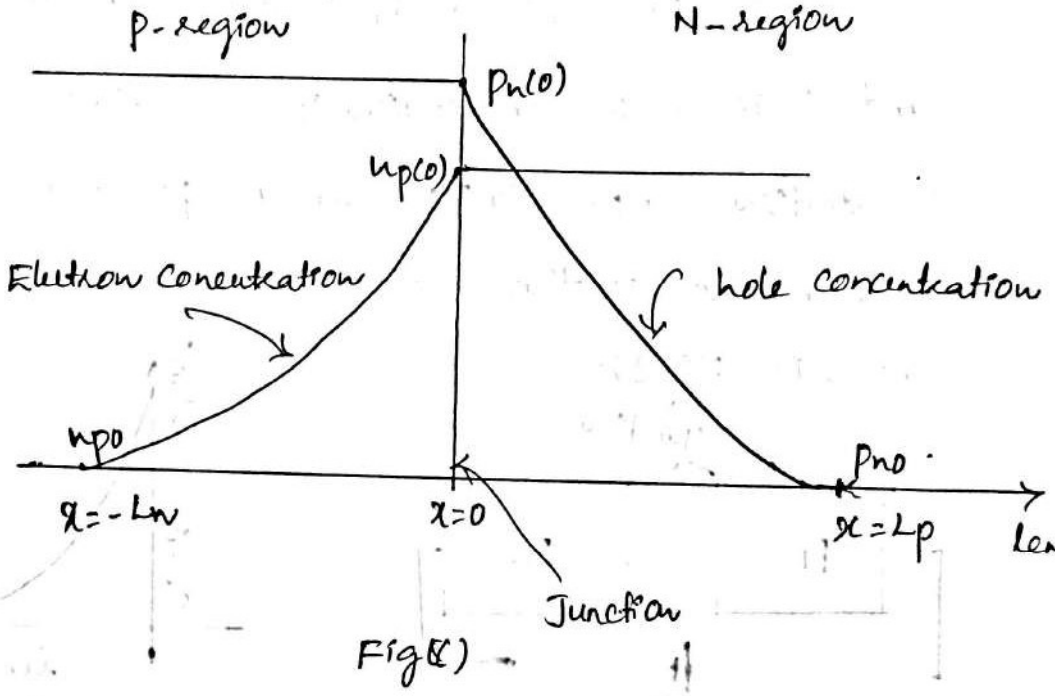
P_1 = High concentration.

In above equ(1), '-' indicates that carrier concentration is exponentially decreasing function w.r.t length of pN junction diode. And 'V' is applied voltage.

V_T is Thermal voltage i.e 26mv

Now consider pN Junction diode, in that diode hole concentration is high in p-region as compare to n-region.

Electron concentration is high in n-region compared to p-region when diode is forward biased at that instant carries concentration varies as shown in Fig(c). For analysis, here we are assuming that Junction width is zero.



Fig(c)

In above Fig(c), $P_n(0)$ is hole concentration in N-layer at $x = 0$ i.e nearer to the junction.

P_{no} is the hole concentration in ~~bay~~ N-layer at $x = L_p$ i.e far away to the junction.

$n_p(0)$ is electron concentration in p-layer at $x = 0$ i.e nearer to the junction

n_{po} is the electron concentration in p-layer at $x = -L_n$ i.e faraway to the junction.

From the law of junction

$$\therefore P_{no} = P_n(0)\, e^{-V/V_T} \quad \text{---- (1)}$$

$$P_n(0) = P_{no}\, e^{V/V_T} \quad \text{---- (1).a}$$

Similarly $n_{po} = n_p(0) e^{-V/V_T}$ —— (2)

$$n_p(0) = n_{po} e^{V/V_T} \quad \text{—— (2a)}$$

diffusion current density for holes $J_p = -qD_p \frac{dp}{dx}$ — (3)

In equation (3), "dp" is the differences between the hole concentration, where dx is the difference of lengths of pn Junction diode.

$$\therefore J_p = -qD_p \frac{(p_n(0) - p_{no})}{0 - L_p}$$

$$J_p = \frac{qD_p}{L_p} (p_n(0) - p_{no})$$

$$J_p = \frac{qD_p}{L_p} (p_{no} e^{V/V_T} - p_{no})$$

$$J_p = \frac{qD_p p_{no}}{L_p} (e^{V/V_T} - 1) \text{ —— (4)}$$

By the definition, current density $J = \frac{\text{current (I)}}{\text{Area (A)}}$

$$\therefore \text{current (I)} = J \times A$$

$$J_p = \frac{I_p}{A} = \frac{qD_p p_{no}}{L_p} (e^{V/V_T} - 1)$$

$$\therefore I_p = \frac{qD_p p_{no} A}{L_p} (e^{V/V_T} - 1) \text{ —— (5)}$$

Similary electron current density $J_n = qD_n \frac{dn}{dx}$

$$J_n = \frac{qD_n}{L_n} (n_p(0) - n_{po})$$

$$J_n = \frac{qD_n}{L_n} (n_{po} e^{V/V_T} - n_{po})$$

$$J_n = \frac{qD_n n_{po}}{L_n}\left(e^{V/V_T} - 1\right)$$

$$J_n = \frac{I_n}{A}$$

$$\therefore I_n = J_n \times A = \frac{qD_n n_{po} A}{L_n}\left(e^{V/V_T} - 1\right) \quad \text{——— (6)}$$

$\therefore$ Total current I = Electron current (I_n) + Hole current (I_p)

$$= I_n + I_p$$

$$= \frac{qD_n n_{po} A}{L_n}\left(e^{V/V_T} - 1\right) + \frac{qD_p p_{no} A}{L_p}\left(e^{V/V_T} - 1\right)$$

$$= \underbrace{\left[\frac{qD_n n_{po} A}{L_n} + \frac{qD_p p_{no} A}{L_p}\right]}_{I_0}\left(e^{V/V_T} - 1\right)$$

$$I = I_0\left[e^{V/V_T} - 1\right] \quad \text{——— (7)}$$

where $I_0 = \frac{qD_n n_{po} A}{L_n} + \frac{qD_p p_{no} A}{L_p}$

* General expression for current $\boxed{I = I_0\left[e^{V/\eta V_T} - 1\right]}$.

where η is the Ideality constant i.e 1 for Ge
2 for Si

V_T is thermal voltage = 26mV

$$= \frac{T}{11,600}$$

$$= \frac{KT}{q}$$

where T is temp in °c
K is boltzmann constant
q is charge.

Limitations in the operating conditions of PN junction:-

Every PN junction diode has limiting values of

1) Maximum forward current
2) Peak Inverse Voltage (PIV)
3) Maximum power rating

PN junction diode will give satisfactory performance if it is operated with in these limiting values. However, if these values are exceeded, the PN junction may be destroyed due to excessive heat.

1) **Maximum forward current:-**

It is the highest instantaneous forward current that a PN junction can conduct without damage to the junction. If the forward current in a PN junction is more than this rating, the junction will be destroyed due to overheating.

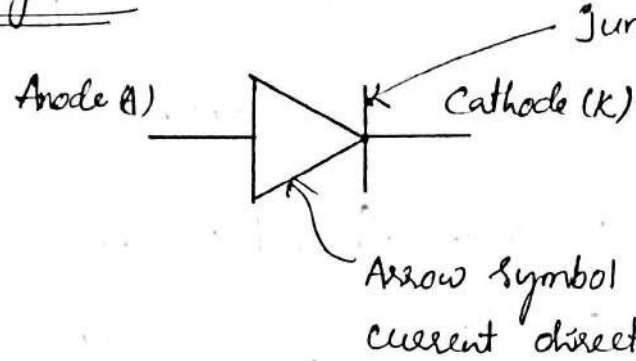
2) **Peak inverse voltage:-**

It is the maximum reverse voltage that can be applied to the PN junction without damage to this junction. If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat. The peak inverse voltage is of particular importance in rectifier application.

3) **Maximum power rating:-**

It is the maximum power that can be dissipated at the junction without damaging it. The power dissipated at the junction is equal to the product of PN junction current and the voltage across the junction.

Diode symbol:-



Equivalent Circuit model of pN Junction diode:-

1) piece-wise Linear model (or) Approximate equalent model:-

When the forward voltage V_F is applied across a diode, it will not conduct till the potential barrier 'V_0' at the junction is overcome. When the forward voltage exceeds the potential barrier voltage, the diode starts conducting. The forward current I_f flowing through the diode causes a voltage drop in its internal resistance 'r_f'.

∴ The forward voltage V_F is applied across the diode is sum of potential barrier 'V_0' and internal voltage drop "$I_f r_f$".

∴ $V_F = V_0 + I_f r_f$

∴ approximate equivalent circuit for a pN junction diode is a switch in series with a battery 'V_0' internal resistance r_f as shown in below Fig.

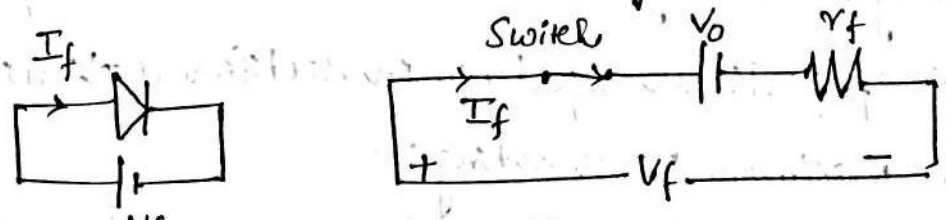


Fig:- Equivalent Circuit model.

2) Simplified equalent Circuit:-

For most applications, the Internal resistance r_f is negligible. So that equalent Circuit then reduced to shown in Fig. This simplified equalent Circuit of the pN Junction diode is frequently used in Circuit analysis.

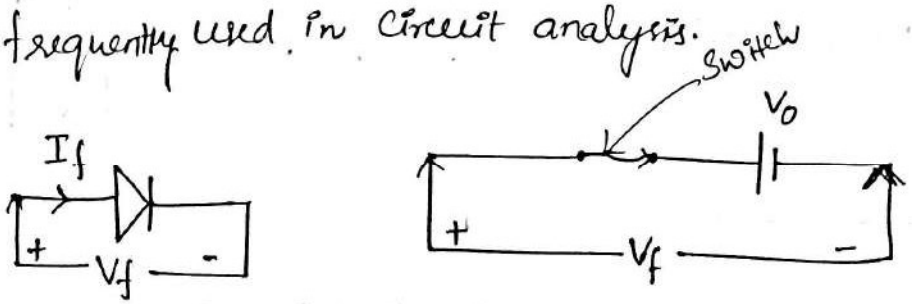


Fig: Equalent Circuit

3) Ideal diode mode:-

An ideal diode is one which behaves as a perfect Conductor when fowaard biased and a perfect Insulator when reverse bias. So that In this situation fowaard resistance $r_f = 0$ and barrier voltage 'V_o' is also negligible.

But in practical Ideal diode not exists. While discussing diode Circuits, the diode will be assumed Ideal unless and untill Stated otherwise.

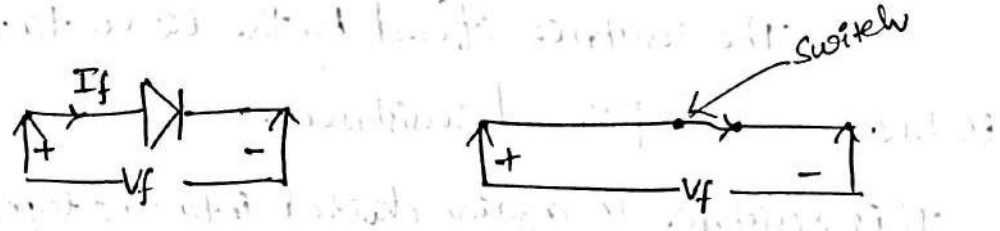
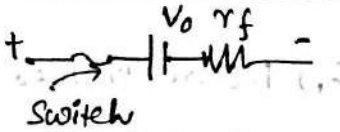
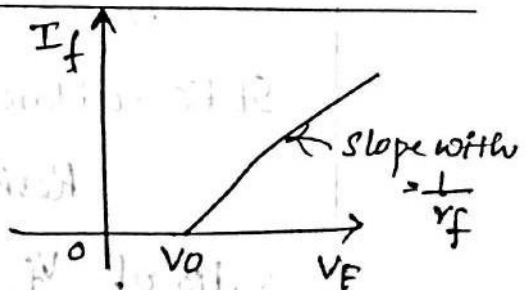
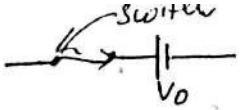
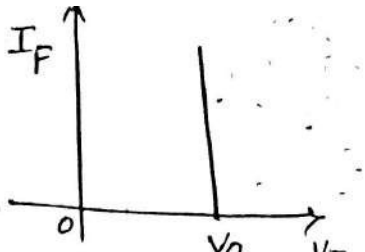
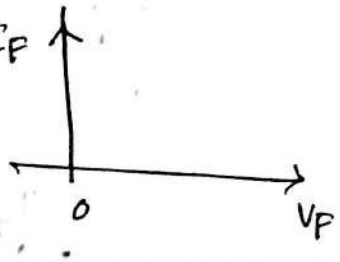
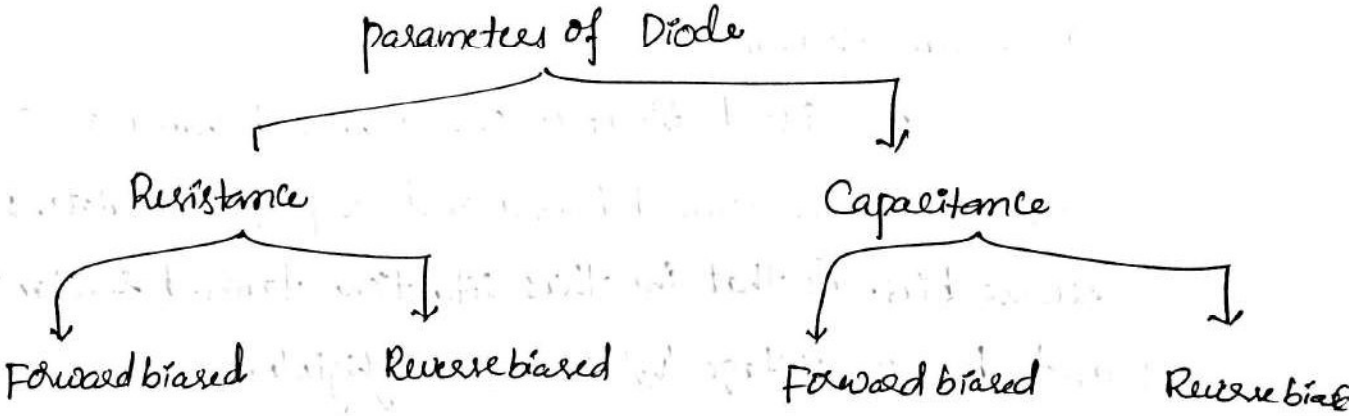


Fig:- Equalent Circuit.

Type	Equivalent model	V-I Characteristics.
1) piecewise linear model (or) Approximate model	 $V_F = V_o + I_f r_f$ $\frac{V_F - V_o}{r_f} = I_f$ Where r_f = Constant	

2) Simplified model	 $V_F = V_0$	
3) Ideal model		

Parameters calculations of PN junction diode:-



Resistance of diode:-

1) Forward resistance:-

The resistance offered by the diode to forward bias is known as "Forward resistance".

This resistance is again divided into two types:-

a) Dynamic resistance (or) AC resistance

b) Static resistance (or) DC resistance.

Static resistance (or) DC resistance:-

Resistance offered by the diode for a dc input i.e ratio of $\frac{V_f}{I_f}$ where V_f is forward voltage

I_f is forward current at V_f.

Dynamic resistance (or) AC forward resistance:-

Resistance offered by the diode for a AC input i.e ratio of $\frac{dv_f}{dI_f}$ (or) $\frac{\Delta V_f}{\Delta I_f}$

where dv_f is difference (or) Change in forward voltage

dI_f is difference (or) Change in forward current.

Consider current equation

$$I = I_0 \left(e^{V/\eta V_T} - 1\right) \quad \text{---(1)}$$

differentiating eqn(1) w.r.t V

$$\frac{dI}{dv} = \frac{I_0 e^{V/\eta V_T}}{\eta V_T}$$

where $\frac{dI}{dv}$ is the conductance i.e, inverse of resistance and that is indicated with g

$$\therefore \text{Conductance } g = \frac{I_0 e^{V/\eta V_T}}{\eta V_T} \quad \text{---(2)}$$

In eqn(2), Adding and Substracting I_0 in the numerator.

$$g = \frac{I_0 e^{V/\eta V_T} - I_0 + I_0}{\eta V_T}$$

$$g = \frac{I_0 \left(e^{V/\eta V_T} - 1\right) + I_0}{\eta V_T}$$

$$g = \frac{I + I_0}{\eta V_T} \quad \left[\because I = I_0 \left(e^{V/\eta V_T} - 1\right)\right]$$

$$\therefore \text{Resistance } R = \frac{1}{g} = \frac{\eta V_T}{I + I_0} \quad \text{---(3)}$$

In forward bias, reverse saturation current I_0 is neglected.

$$\therefore R_f = \frac{\eta V_T}{I} \quad \leftarrow (4)$$

Forward resistance of pN junction diode is very less, ranging from 1 to 100 Ω.

Reverse resistance:-

The resistance offered by the diode to the reverse bias is known as reverse resistance.

It can be 1) DC reverse resistance

2) AC reverse resistance

Ideally reverse resistance is infinity but in practical reverse resistance is very large.

1) DC reverse resistance:-

Resistance offered by the diode for a dc input in reverse bias i.e, ratio of V_R / I_R.

2) AC reverse resistance:-
(or)
Dynamic resistance

$$\text{Dynamic resistance} = \frac{dv}{dI}$$

From eqn (3)

$$R = \frac{1}{g} = \frac{\eta V_T}{I + I_0}$$

In reverse bias I is negligible

$$\therefore R = \frac{\eta V_T}{I_0} \quad \text{——— (5)}$$

∴ Reverse resistance is always in range of "MΩ".

Junction capacitance:-

Junction Capacitance

- Forward Junction Capacitance (or) Diffusion (or) Storage Capacitance
- Reverse Junction Capacitance (or) Transition capacitance
  - Step graded (unequal dopping)
  - Linear graded (Equal dopping)

Diffusion (or) Storage capacitance:-

Capacitance offered by the pN junction diode in forward bias

$$\text{Capacitance } C = \frac{\text{Charge } (Q)}{\text{Voltage } (V)}$$

When Charge is varies with respect to voltage, we are taking as

$$C_s = \frac{dQ_v}{dv} \quad \text{---(1)}$$

Where Q_v = Volume charge and current I is defined as

$$I = \frac{Q}{T} \quad \text{---(2)}.$$

$$\frac{dI}{dQ} = \frac{1}{T}$$

$$dQ = T.dI \quad \text{---(3)}.$$

Sub eqn(3) in eqn(1)

$$C_s = T.\frac{dI}{dv} \quad \text{---(4)}$$

Where $I = I_0\left(e^{V/\eta V_T} - 1\right)$; $\frac{dI}{dv} = \frac{I_0 e^{V/\eta V_T}}{\eta V_T}$

$$\frac{dI}{dv} = \frac{I_0 e^{V/\eta V_T} - I_0 + I_0}{\eta V_T}$$

$$\frac{dI}{dV} = \frac{I + I_0}{\eta V_T} \quad \text{---- (5)}$$

Sub eqn (5) into eqn (4)

$$C_s = \tau \left(\frac{I + I_0}{\eta V_T} \right) \quad \text{---- (6)}$$

Where diode is in forward bias I_0 is negligible.

$$\therefore C_s = \frac{\tau I}{\eta V_T} \quad ; \quad C_s \propto I$$

2) Reverse bias capacitance (or) Transition Capacitance:-

Transition Capacitance

a) Step graded (unequal dopping)

b) Linear graded (Equal dopping).

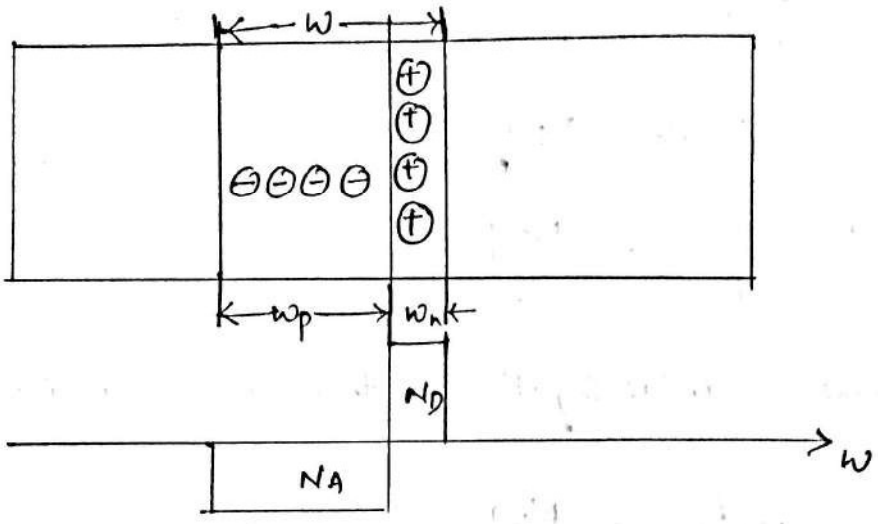
a) Step graded (or) Abrupt or) alloy (or) fusion (or) Barrier Capacitance:-

When junction in Reverse bias, the junction width increases, Let Concentration of donar atoms (N_D) is far greater than Concentration of acceptor atoms (N_A).

$$N_D >> N_A$$

In this cas junction width in n-type is decreases ($\because$ doping Concentration of N_D is greater). And junction width in p-type is increases ($\because$ doping concentration of N_A is very less).

A junction in which there an abrupt change from acceptor ions from one side to donar ions on other side Such as junction is called as "fusion or Alloy junction".



In above figure W_p : Junction width in p-type

W_n : Junction width in n-type

W : Total Junction width.

$\therefore W = W_p + W_n$

But $W_p >> W_n$ So Compare to W_p, W_n is negligible

$\therefore W \simeq W_p$

A/c to poissons eqn

$$\frac{d^2V}{dx^2} = \frac{-\rho_v}{\epsilon} \quad \text{——— (1)}$$

Above equation ~~equal~~ gives the ~~see~~ relation between Voltage and Charge density.

In eqn(1) V : applied Voltage

ρ_v : Volume Charge density

ϵ : permitivity of materials.

here $\rho_v = nq$ [$\because$ n is the Concentration of carriers that equal to $\frac{N}{LA}$]

Here $n = N_A$ or N_D [In the Junction net charge is zero i.e $N_A = N_D$]

q is charge carrier

$$\therefore \rho_v = N_D q$$

$$\therefore \frac{d^2V}{dx^2} = \frac{-N_D q}{\epsilon}$$

When considering the electron as a carrier q is "-q".

$$\therefore \frac{d^2V}{dx^2} = \frac{N_D q}{\epsilon} \quad \text{—— (2)}$$

Integrating above eqn is

$$\frac{dV}{dx} = \frac{N_D q x}{\epsilon} \quad \text{—— (3)}$$

Integrating eqn(3)

$$V = \frac{N_D q x^2}{2\epsilon} \quad \text{—— (4)}$$

Where $x = W_n + W_p$

$$= W_p$$

$$x = W \quad \text{— (5)} \qquad \because W = W_n + W_p$$

$$W = W_p \quad [\because W_p >> W_n]$$

Sub (5) in (4)

$$V = \frac{N_D q W^2}{2\epsilon} \quad \text{—— (6)}$$

$$W = \left[\frac{2V\epsilon}{N_D q}\right]^{1/2} \quad \text{—— (7)}$$

Here ϵ, N_D, q are constants

$$\boxed{\therefore W \propto V^{1/2}} \quad \text{—— (8)}$$

In Reverse bias when voltage increases the width of the junction increases.

By the definition volume charge density

$$\rho_v = \frac{\text{Charge}}{\text{Volume}}$$

$$\rho_v = \frac{Q_v}{\text{volume}}$$

Where volume $= A \cdot W$

$$\rho_v = \frac{Q_v}{A \cdot W}$$

$$Q_v = N_D q \cdot A \cdot W \quad [\because \rho_v = N_D q] \rightarrow (7).$$

Capacitance $C = \frac{dQ_v}{dV}$

$$C = \frac{dQ_v}{dW} \cdot \frac{dW}{dV} \quad \text{——— (I)}$$

differentiating eqn (7) w.r.t W

$$\frac{dQ_v}{dW} = N_D q \cdot A \quad \text{——— (8)}$$

differentiating eqn(6) w.r.t W

$$\frac{dV}{dW} = \frac{N_D \cdot q \cdot W}{\epsilon} \quad \text{— (9).}$$

from eqn (9) $\frac{dW}{dV} = \frac{\epsilon}{N_D \cdot q \cdot W}$ ——— (10).

Sub eqn (8) and (10) on eqn(I) = ~~$N_D q \cdot A \times \frac{\epsilon}{N_D q W}$~~

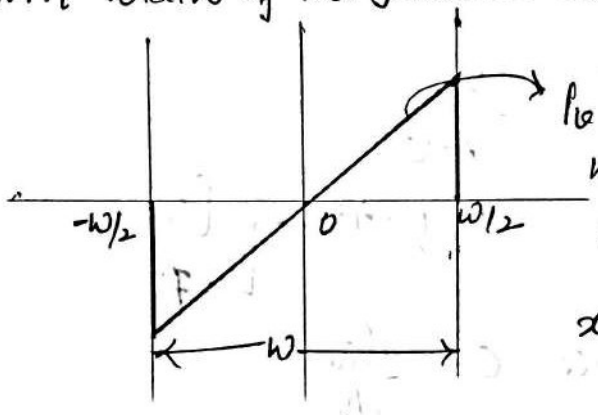
$$\boxed{C_j = \frac{\epsilon A}{W}} \quad \text{——— (11)}$$

From above equations, when voltage is increases in reverse bias width of the junction is increases, when width is increases, Transition capacitance decreases.

$V \uparrow \quad W \uparrow \quad C_T \downarrow$

Linear graded (or) Grown Junction Capacitance:-

In linear graded junction charge density is linearly increases w.r.t width of the junction as shown in below Fig.



where a is the slope of the straight line

x is length of semiconductor

A/c to poissions eqn

$$\frac{d^2V}{dx^2} = \frac{-\rho_e}{\epsilon}$$

where $\rho_e = ax$ where a is the slope of the line

$$\frac{d^2V}{dx^2} = \frac{ax}{\epsilon}$$

$$\frac{dV}{dx} = \frac{ax^2}{2\epsilon}$$

$$V = \frac{ax^3}{6\epsilon}$$

where $x = W$

$$V = \frac{aW^3}{6\epsilon} \rightarrow W = \left(\frac{6\epsilon V}{a}\right)^{1/3}$$

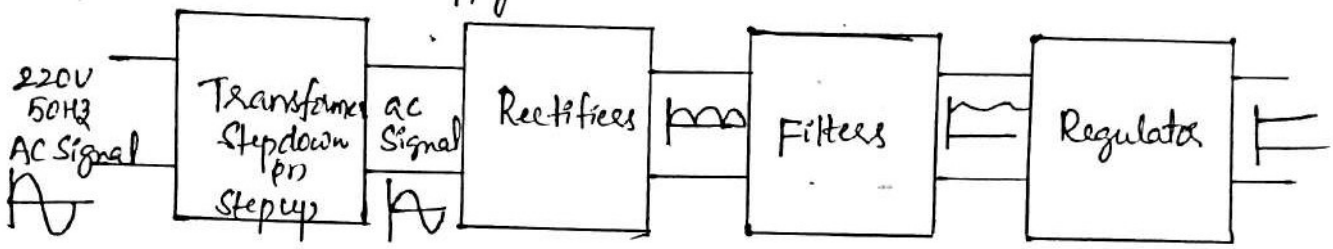
$\boxed{W \propto V^{1/3}}$ $\boxed{C_T = \frac{\epsilon A}{W}}$ But $W \propto V^{1/3}$.

UNIT-II

RECTIFIERS

For reasons associated with economics of generation and transmissio the electric power available is usually an ac Supply. Normally that ac Supply voltage varies sinusodially and has 50Hz frequency. It is used for lighting, heating and Electric motors.

But there are many applications (eg: electronics) where dc Supply is needed. When a dc Supply is needed, ac Supply is Converted into dc Supply as shown in below.



In above Fig, ac input is applied to transformer. Transformer may be Stepup (or) stepdown, generally Stepdown transformer is used. Output of transformer is ac wave form with large amplitude (or) small amplitude compared to i/p ac wave-form.

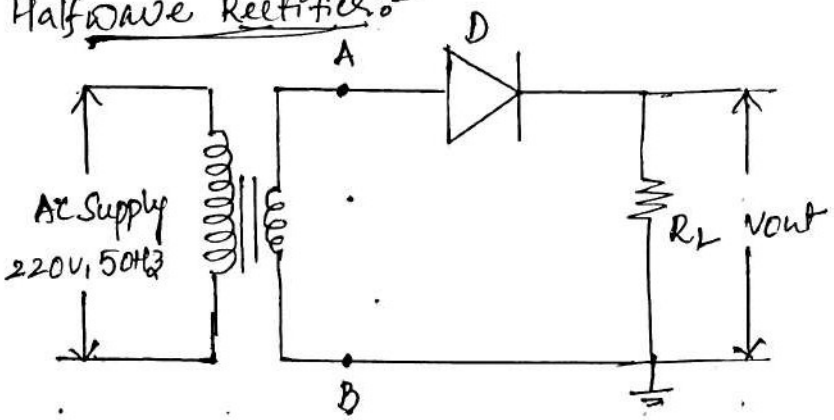
Rectifier converts ac Signal into pulsating dc (or) it converts bidirectional Signal to unidirectional Signal. o/p of Rectifier having small ac component and large dc component. Small ac component of o/p is filtered (or removed) by using Filters. But even in output of Filters is also having very small ac Component (ripple), that is smoothen by using voltage Regulator. output of Regulator is pure DC Signal. Normally that DC Signals are used to activating the Electronic devices. Now we consider Rectifier.

Purpose of the Rectifier is "Converting Bidirectional Signal into unidirectional Signal" by using diodes Switching property.

Generally Rectifiers are 3 types:-

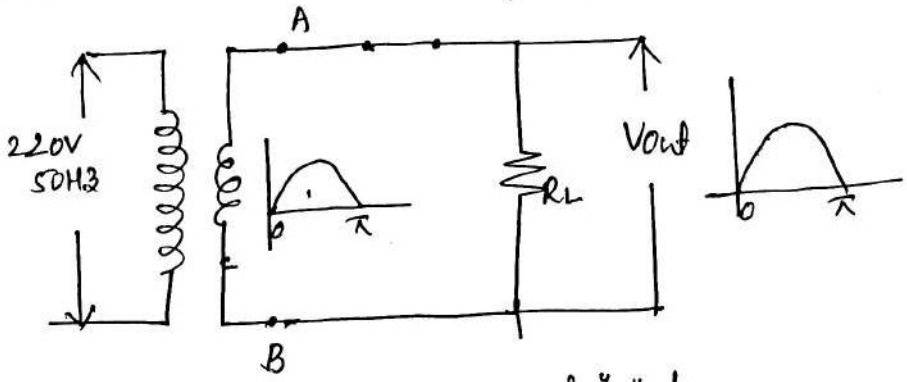
1) Halfwave Rectifier
2) Fullwave Rectifier with Center tapped
3) Bridge Rectifier.

Halfwave Rectifier:-

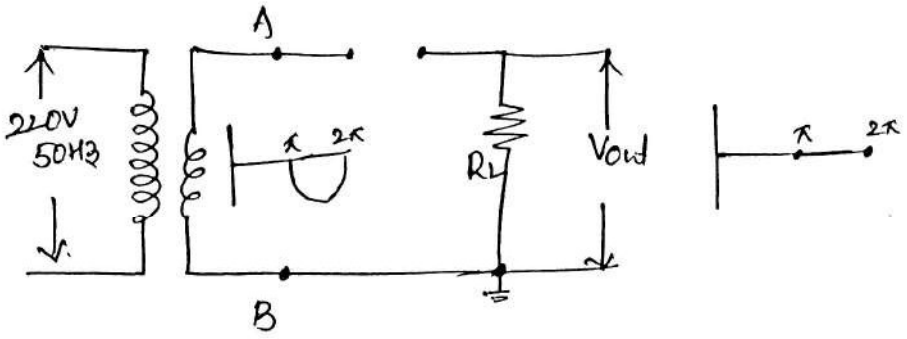


Operation:-

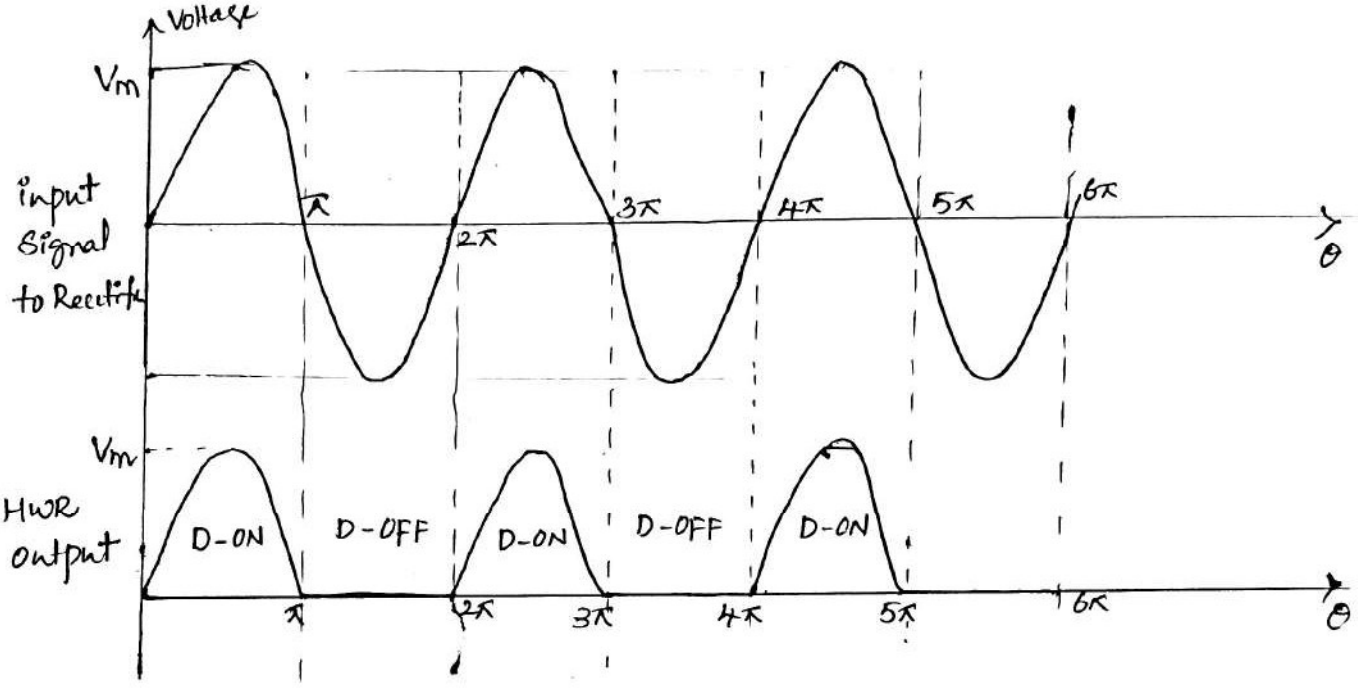
For positive cycle of input ac voltage, end 'A' becomes +ve w.r.t 'B', so that diode is operated in Forward bias i.e ideally it is treated as "ON" Switch. So it passes the entire positive cycle to load as shown in below Fig.



For Negative cycle, End 'A' becomes -ve w.r.t B, so that diode is operated in Reverse bias i.e ideally it is treated as "OFF" Switch. So that total voltage drop across the diode i.e no current flows through the R_L for -ve half cycle as shown in below Fig.



Operation of the Halfwave Rectifier is illustrated using following waveforms.



Input Signal $V_{in} = V_m \sin\theta \qquad 0 < \theta < 2\pi$

For Input Signal, Avg (or) DC Value is defined as

$$V_{DC} \text{ (or) } V_{Avg} = \frac{1}{T}\int_0^T V_{in} \cdot d\theta$$

Where T is Time period

$$V_{DC} = \frac{1}{2\pi}\int_0^{2\pi} V_m \sin\theta \cdot d\theta$$

$$= \frac{V_m}{2\pi}\left[-\cos\theta\Big|_0^{2\pi}\right] = \frac{V_m}{2\pi}\left[-(1-1)\right]$$

For Input Signal

$V_{DC} = 0$

For Input Signal Root Mean Square (RMS) Value is defined as

$$= \sqrt{\frac{1}{T}\int_0^T V_{in}^2 d\theta}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(V_m \sin\theta)^2 d\theta}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\int_0^{2\pi}\sin^2\theta\, d\theta} = \sqrt{\frac{V_m^2}{2\pi}\int_0^{2\pi}\left(\frac{1-\cos 2\theta}{2}\right)d\theta}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\int_0^{2\pi}(1-\cos 2\theta)\,d\theta}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\left\{\int_0^{2\pi}1\cdot d\theta - \int_0^{2\pi}\cos 2\theta\, d\theta\right\}}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\left\{2\pi - \frac{\sin 2\theta}{2}\Big|_0^{2\pi}\right\}}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\{2\pi - 0\}}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\times\frac{2\pi}{2}}$$

For input signal, RMS value.

$$V_{RMS} = \frac{V_m}{\sqrt{2}}$$

By the definition

$$V_{RMS}^2 = V_{dc}^2 + V_{acrms}^2$$

$$V_{RMS}^2 = V_{acrms}^2 \quad [\because V_{dc} = 0 \text{ for input signal}]$$

For i/p signal $\therefore V_{RMS} = V_{acrms}$.

For Halfwave Rectifier output :-

$$V_{dc} = \frac{1}{T}\int_0^T V_m \sin\theta\, d\theta$$

For HWR output Time period is 2π

$$V_{DC} = \frac{1}{2\pi}\left\{\int_0^{\pi} V_m \sin\theta\, d\theta + \int_{\pi}^{2\pi} 0 \cdot d\theta\right\}$$

$$= \frac{1}{2\pi}\int_0^{\pi} V_m \sin\theta\, d\theta$$

$$= \frac{V_m}{2\pi}\cdot\int_0^{\pi} \sin\theta\, d\theta$$

$$= \frac{V_m}{2\pi}\left[-\cos\theta\Big|_0^{\pi}\right]$$

$$= \frac{V_m}{2\pi}\left[-(-1-1)\right]$$

$$= \frac{V_m}{2\pi} \times 2$$

$$\boxed{V_{DC} = \frac{V_m}{\pi}}$$

$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T (V_m \sin\theta)^2 d\theta}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} V_m^2 \sin^2\theta\, d\theta}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\int_0^{\pi}\left(\frac{1-\cos 2\theta}{2}\right) d\theta}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\int_0^{\pi}(1-\cos 2\theta)\, d\theta}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\left\{\theta\Big|_0^{\pi} - \frac{\sin 2\theta}{2}\Big|_0^{\pi}\right\}}$$

$$= \sqrt{\frac{V_m^2}{4\pi}\cdot\pi} = \frac{V_m}{2}$$

$$\therefore V_{RMS} = \frac{V_m}{2}$$

By the definition

$$V_{RMS}^2 = V_{DC}^2 + V_{acrms}^2$$

$$V_{acrms}^2 = V_{RMS}^2 - V_{DC}^2$$

$$V_{acrms}^2 = V_{DC}^2 \left[\frac{V_{RMS}^2}{V_{DC}^2} - 1 \right]$$

$$\left(\frac{V_{acrms}}{V_{DC}} \right)^2 = \left[\frac{V_{RMS}^2}{V_{DC}^2} - 1 \right]$$

$$\therefore \quad \frac{V_{acrms}}{V_{DC}} = \sqrt{\frac{V_{RMS}^2}{V_{DC}^2} - 1}$$

For HWR, $V_{RMS} = \frac{V_m}{2}$ and $V_{DC} = \frac{V_m}{\pi}$

$$\frac{V_{acrms}}{V_{DC}} = \sqrt{\left(\frac{\frac{V_m}{2}}{\frac{V_m}{\pi}} \right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1}$$

$$= 1.21$$

$$\boxed{\text{Ripple factor} = \frac{V_{acrms}}{V_{DC}} = 1.21}$$

From above expression we concluded that, in output of HWR, ac component (Ripple) is dominated than the DC component.

- Efficiency $\eta = \dfrac{\text{DC power delivered to the load}}{\text{Rms power}} \times 100$

$$= \frac{P_{dc}}{P_{RMS}} \times 100$$

$$P_{dc} = \frac{V_{dc}^2}{R_L} \; ; \quad P_{RMS} = \frac{V_{RMS}^2}{R_L}$$

$$\eta = \frac{P_{dc}}{P_{rms}} \times 100 = \frac{\frac{V_{dc}^2}{R_L}}{\frac{V_{RMS}^2}{R_L}} \times 100$$

$$= \left(\frac{V_{dc}}{V_{RMS}}\right)^2 \times 100$$

$$= \left(\frac{\frac{V_m}{\pi}}{\frac{V_m}{2}}\right)^2 \times 100 = \left(\frac{2}{\pi}\right)^2 \times 100$$

$$= 40.6\%$$

$\therefore$ Efficiency η of HWR = 40.6%.

peak Inverse Voltage :-

V_m is the maximum voltage across the secondary winding.

PIV means, max voltage drop across the reverse biased diode.

In Halfwave Rectifier

$$PIV = V_m$$

$$*\text{Form factor} = \frac{V_{RMS}\text{ Value}}{V_{DC}\text{ Value}} = \frac{\frac{V_m}{2}}{\frac{V_m}{\pi}} = \frac{\pi}{2} = 1.57$$

$$*\text{peak factor} = \frac{\text{peak Value}}{\text{RMS Value}} = \frac{V_m}{\frac{V_m}{2}} = 2$$

*Output Frequency of HWR = Input Frequency of Rectifier

$F_{out} = F_{in}$ $\therefore$ Time period is same for both input and output of the waveform

* Transformer utilization factor (TUF) = $\frac{P_{dc}}{V_{rms} \cdot I_{rms}}$ → for Secondary

Where $P_{dc} = \frac{V_{dc}^2}{R_L} = \frac{\left(\frac{V_m}{\pi}\right)^2}{R_L}$

Vrms of Secondary terminal is = $\frac{V_m}{\sqrt{2}}$

Irms of Secondary terminal is = $\frac{I_m}{2}$

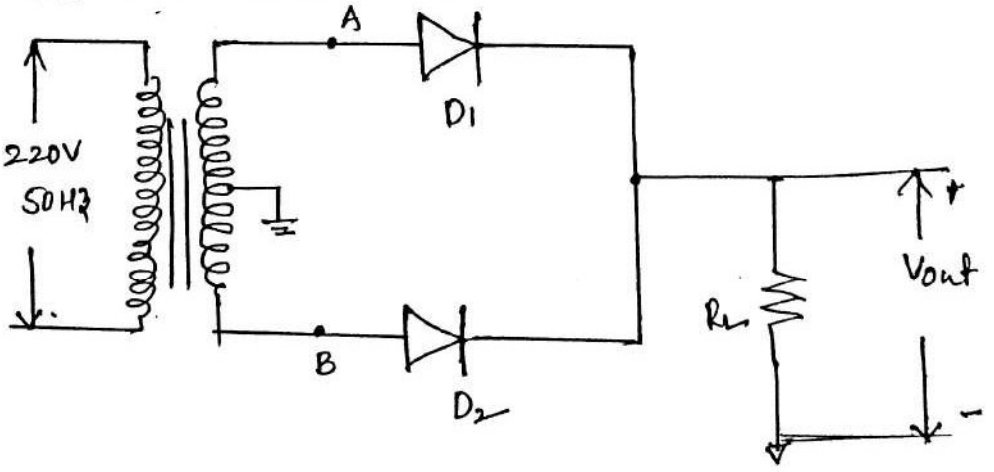
Where $I_m = \frac{V_m}{R_L}$

Irms of Secondary terminal is = $\frac{V_m}{2R_L}$

$V_{rms} \times I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{V_m}{2R_L} = \frac{V_m^2}{2\sqrt{2}R_L}$

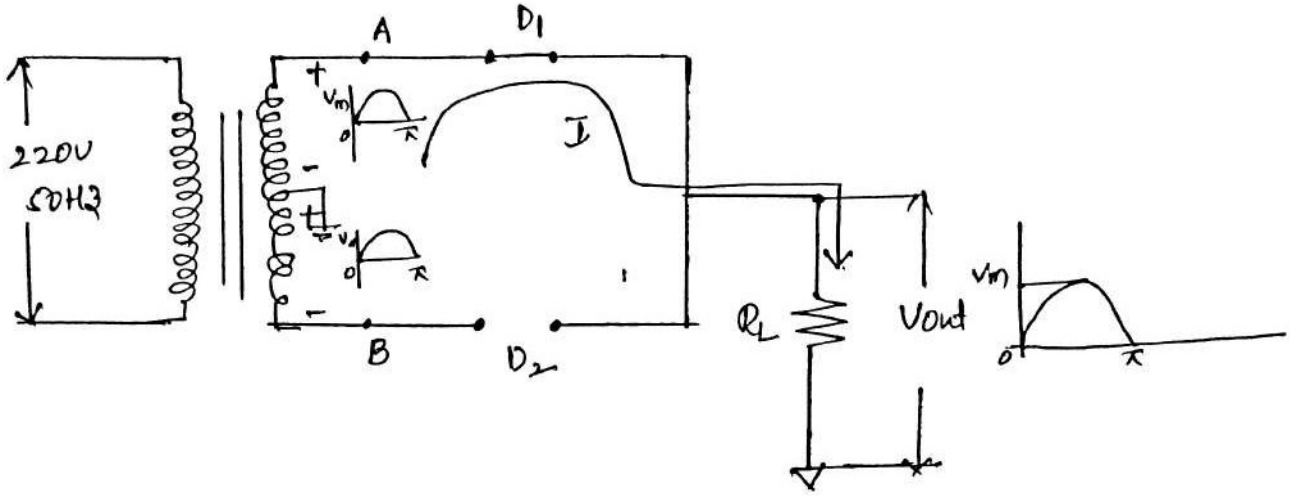
$\therefore$ TUF = $\frac{\left(\frac{V_m}{\pi}\right)^2}{\frac{R_L}{\frac{V_m^2}{2\sqrt{2}R_L}}} = \frac{\frac{V_m^2}{\pi^2}}{\frac{V_m^2}{2\sqrt{2}}} = \frac{2\sqrt{2}}{\pi^2} = 0.287.$

Full wave Rectifier with Center tapped :-



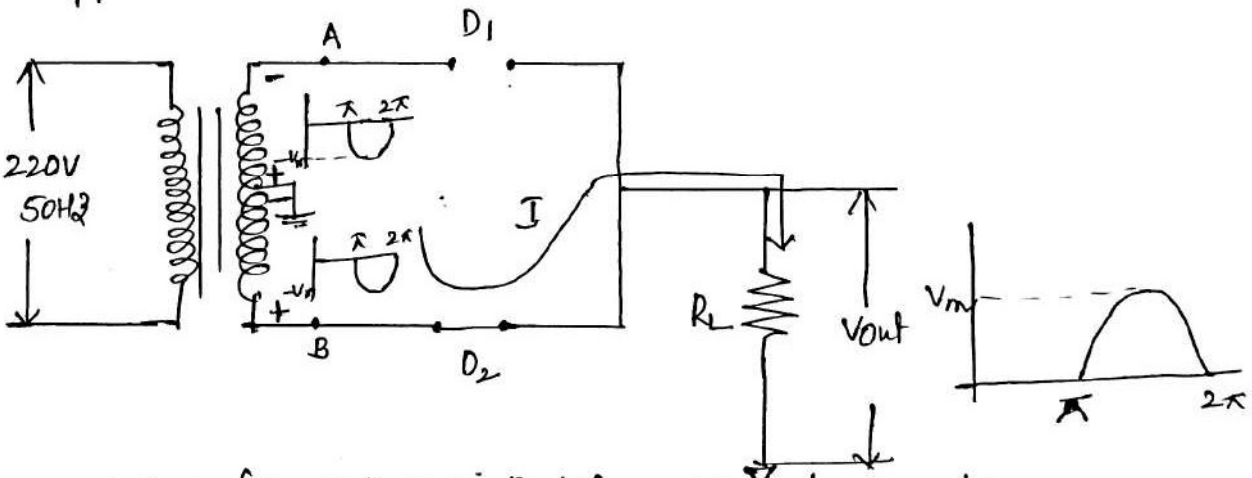
Operation of Fullwave Rectifier :-

For +ve cycle End "A" becomes +ve w.r.t B. So that diode D_1 is conducted (or) "ON", D_2 is in reverse bias, So it is "OFF". Current direction is shown in below Fig.

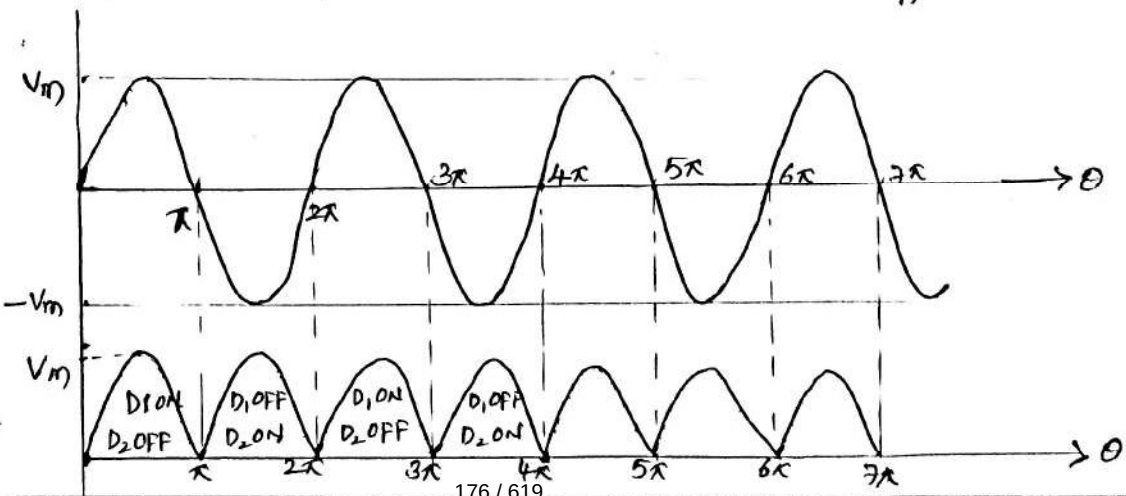


For negative cycle:-

End "B" becomes +ve w.r.t "A", So that diode D_1 is OFF and D_2 is ON. Current direction is shown in below



Wave Forms for Fullwave Rectifier with Center tapped :-



Output of FWR is expressed as

$$V_m \sin\theta \qquad 0 < \theta < \pi$$

$$V_{dc} = \frac{1}{T}\int_0^T V_m \sin\theta \, d\theta$$

$$= \frac{1}{\pi}\int_0^{\pi} V_m \sin\theta \, d\theta = \frac{V_m}{\pi}\int_0^{\pi} \sin\theta \, d\theta$$

$$= \frac{V_m}{\pi}\left[-\cos\theta\Big|_0^{\pi}\right]$$

$$\therefore V_{dc} = \frac{2V_m}{\pi}$$

$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T (V_m \sin\theta)^2 d\theta} = \sqrt{\frac{1}{\pi}\int_0^{\pi} (V_m \sin\theta)^2 d\theta}$$

$$= \sqrt{\frac{V_m^2}{\pi}\int_0^{\pi} \sin^2\theta \, d\theta}$$

$$= \sqrt{\frac{V_m^2}{\pi}\int_0^{\pi} \left(\frac{1-\cos 2\theta}{2}\right) d\theta}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\int_0^{\pi} (1-\cos 2\theta) \, d\theta}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\left\{\theta\Big|_0^{\pi} - \frac{\sin 2\theta}{2}\Big|_0^{\pi}\right\}}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\{\pi - 0\}}$$

$$V_{RMS} = \frac{V_m}{\sqrt{2}}$$

Ripple factor :-

$$V_{RMS}^2 = V_{DC}^2 + V_{ACrms}^2$$

$$V_{ACrms}^2 = V_{RMS}^2 - V_{DC}^2$$

$$V_{ACrms}^2 = V_{DC}^2 \left[\left(\frac{V_{RMS}}{V_{DC}}\right)^2 - 1\right]$$

$$\left(\frac{V_{ACrms}}{V_{DC}}\right)^2 = \left[\left(\frac{V_{RMS}}{V_{DC}}\right)^2 - 1\right]$$

$$\therefore \frac{V_{ACrms}}{V_{DC}} = \sqrt{\left(\frac{V_{RMS}}{V_{DC}}\right)^2 - 1}$$

$$= \sqrt{\frac{\left(\frac{V_m}{\sqrt{2}}\right)^2}{\left(\frac{2V_m}{\pi}\right)^2} - 1}$$

$$RF = \frac{V_{ACrms}}{V_{DC}} = \sqrt{\frac{\pi^2}{8} - 1} = \underline{0.482}$$

From above expression we are concluded that dc component is dominated compare to ac component in output waveform of Full wave Rectifier with center tapped.

* Efficiency $\eta = \frac{P_{dc}}{P_{Rms}} \times 100 = \frac{\frac{V_{dc}^2}{R_L}}{\frac{V_{RMS}^2}{R_L}} \times 100$

$$= \frac{\left(\frac{2V_m}{\pi}\right)^2}{\left(\frac{V_m}{\sqrt{2}}\right)^2} \times 100 = \frac{8}{\pi^2} = 0.812 \times 100$$

$$= \underline{81.2\%}$$

PIV :-

In center tapped transformer across the secondary winding is available, So max voltage drop across the reverse biased diode is $2V_m$ that is PIV.

$$\boxed{PIV = 2V_m}$$

* Form factor = $\frac{V_{RMS}}{V_{avg}} = \frac{\frac{V_m}{\sqrt{2}}}{\frac{2V_m}{\pi}} = 1.11$

* peak factor = $\frac{\text{Peak value}}{V_{RMS}} = \frac{V_m}{\frac{V_m}{\sqrt{2}}} = \sqrt{2}$

* $\boxed{F_{out} = 2 \times F_{in}}$

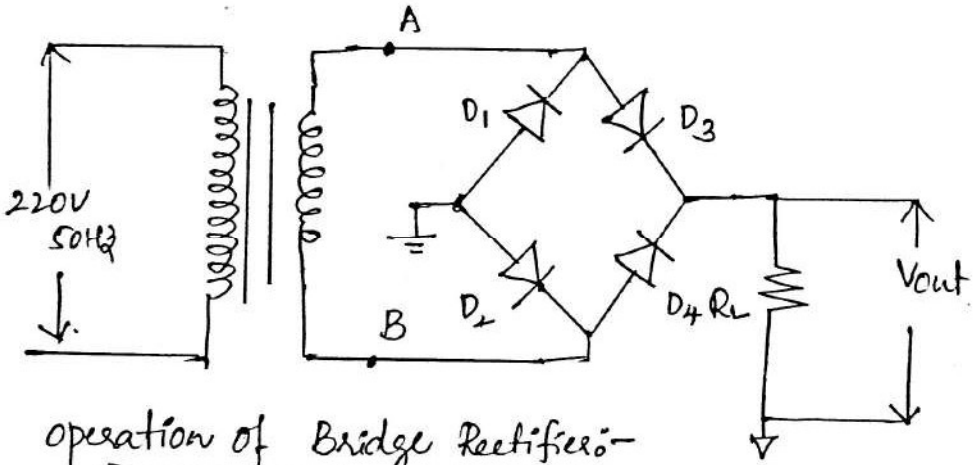
Advantages of FWR with center tapped:-

1) AC component (Ripple) is less in output
2) Efficiency is max

Disadvantages:-

1) It is difficult to locate the center tap
2) Cost of centertap transformer is high
3) Diode experiences the $2V_m$ voltage in Reverse bias, So there is a chance of damage of diode i.e PIV = $2V_m$

Fullwave Bridge Rectifier:-

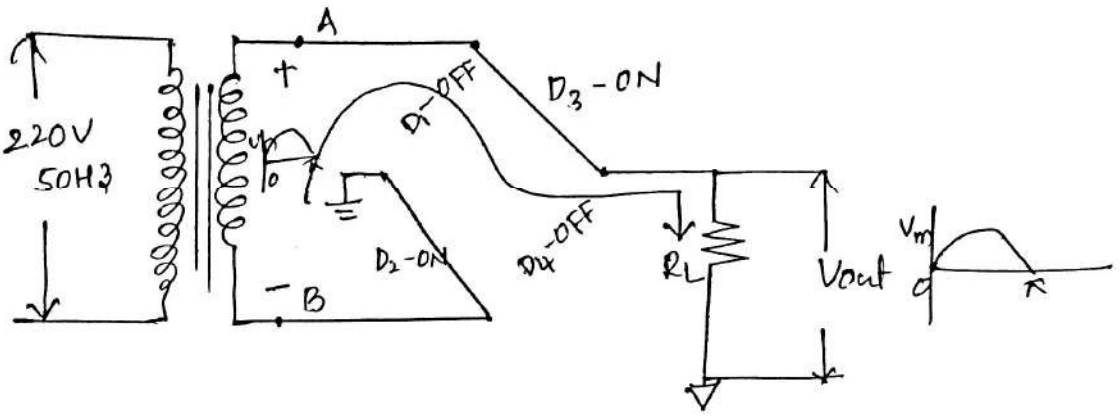


operation of Bridge Rectifier:-

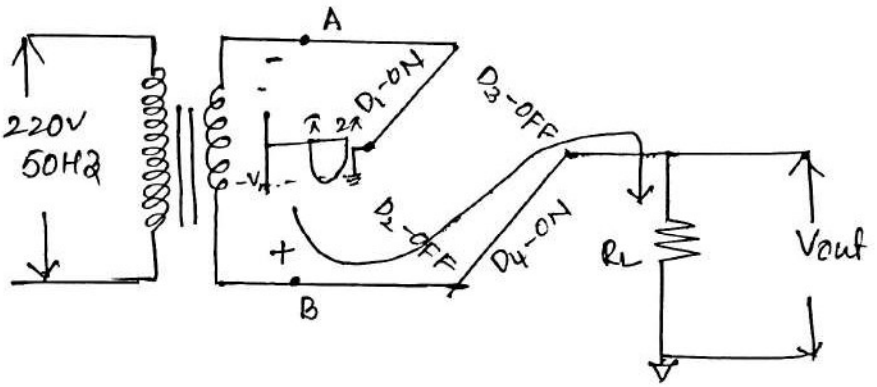
For +ve cycle:-

For +ve cycle End "A" becomes +ve w.r.t B

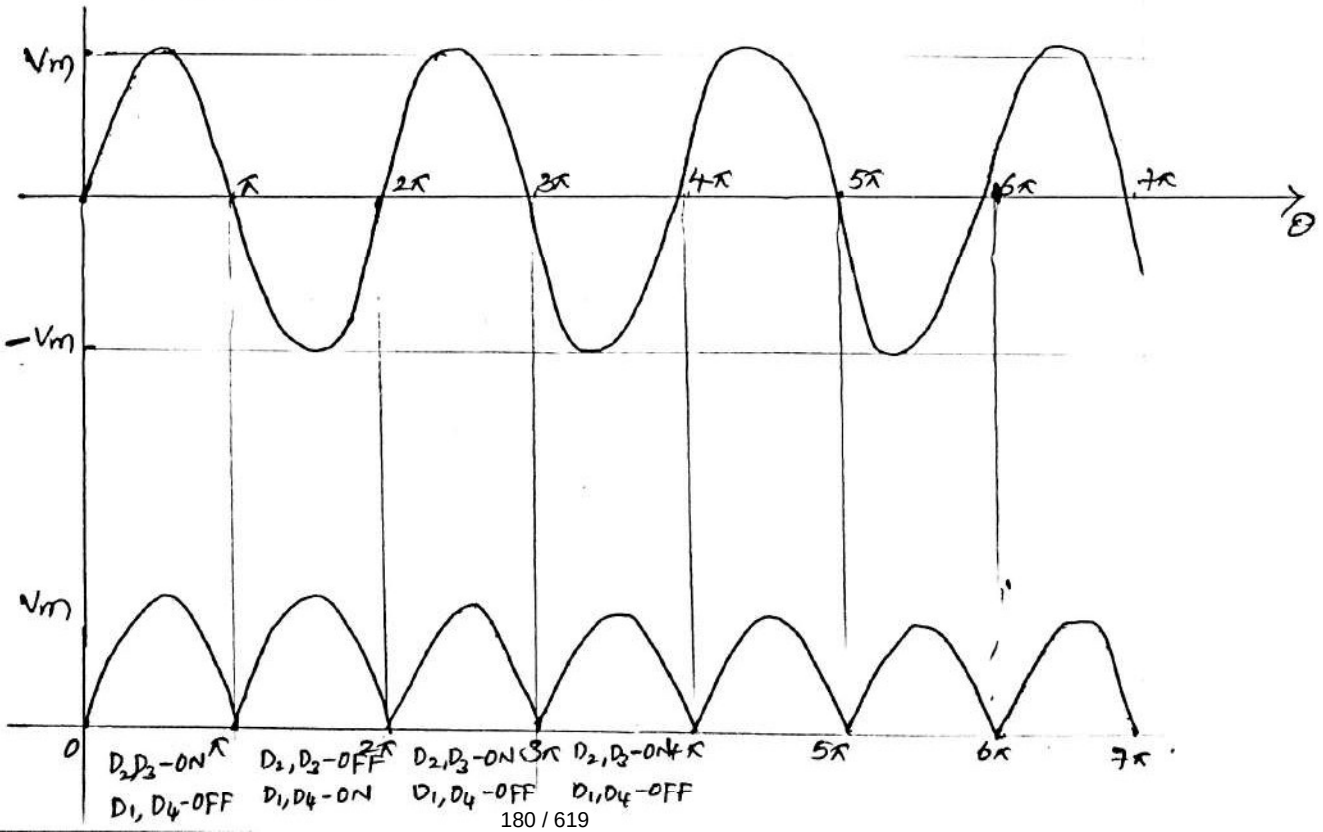
So D3 and D_2 are ON and D_1 and D_4 are OFF. And Current direction, flowing through R_L is indicated in below Fig.



For -ve cycle, end 'A' is -ve w.r.t "B" so D_1 and D_4 are "ON," D_3 and D_2 are "OFF". And current direction flowing through R_L is indicated in below Fig.



Waveforms of Bridge Rectifier:-



Output of Bridge Rectifier is expressed as:

$V_m \sin\theta \quad 0 < \theta < \pi$

** this is same as FWR with centre tapped. So all parameters are same except PIV of Bridge Rectifier is same as FWR with centre tapped except PIV, TUF.

Where PIV for Bridge rectifier is only "V_m", because across the secondary only V_m is available.

* Transformer utilization Factor TUF $= \dfrac{P_{dc}}{V_{rms} \cdot I_{rms}}$ → secondary

Where $P_{dc} = \dfrac{V_{dc}^2}{R_L} = \dfrac{\left(\frac{2V_m}{\pi}\right)^2}{R_L}$

V_{rms} of Secondary terminal of transformer is $\frac{V_m}{\sqrt{2}}$

I_{rms} of Secondary terminal of transformer is $\frac{I_m}{\sqrt{2}}$

Where $I_m = \frac{V_m}{R_L}$

$\therefore I_{rms}$ of Secondary $= \dfrac{V_m}{\sqrt{2} \cdot R_L}$

$\therefore V_{rms} \times I_{rms} = \dfrac{V_m}{\sqrt{2}} \times \dfrac{V_m}{\sqrt{2} R_L} = \dfrac{V_m^2}{2R_L}$

$\therefore$ TUF $= \dfrac{P_{dc}}{P_{acrated}} = \dfrac{\frac{\left(\frac{2V_m}{\pi}\right)^2}{R_L}}{\frac{V_m^2}{2R_L}} = \underline{0.812}$

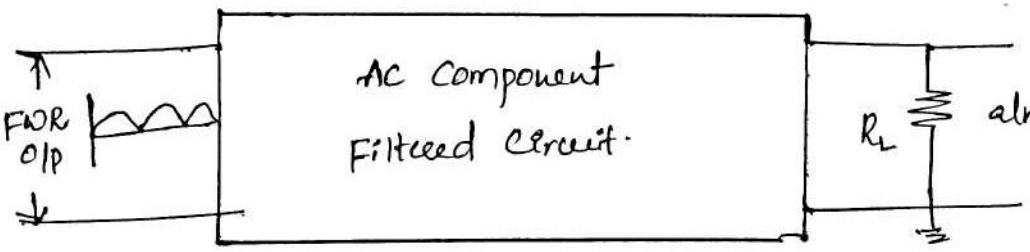
Comparison of Rectifier

Particulars	Type of Rectifier		
	Halfwave	Fullwave	Bridge
• No of Diodes	1	2	4
• V_{dc}	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
• I_{dc}	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$ where $I_m = \frac{V_m}{R_L}$
• V_{RMS}	$\frac{V_m}{2}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
• I_{RMS}	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
• Ripple factor	1.21	0.48	0.48
• Efficiency η	40.6%	81.2%	81.2%
• Form factor	1.57	1.11	1.11
• peak factor	2	$\sqrt{2}$	$\sqrt{2}$
• PIV	V_m	$2V_m$	V_m
• Fout	F_{in}	$2 \times F_{in}$	$2 \times F_{in}$
• TUF	0.287	0.693	0.812

Filters

For reasons associated with economics of generation and transmission the electric power available is usually an ac supply. Normally that supply voltage varies sinusoidally and has a frequency of 50Hz. Normally ac signal is used for heating, lighting, and rotating motors. But there are many applications (for example electronic circuits) where dc supply is needed. When such a dc supply required, the ac signal is converted into dc by using Rectifier. But Rectifier output is having both ac and dc components. AC component is undesirable to do so, a filter circuit is used which removes the a.c component and allows only the dc component to reach the load.

A Filter Circuit is a device which removes the ac component of the rectifier output but allows the dc component to reach the load. Filter should be installed between the rectifier as shown in below.



A Filter Circuit is generally Constructed by using Frequency Sensitive devices i.e "Capacitors" and "Inductors". The Filtering action of 'L' and 'C' depends upon the electrical principles.

$$\text{Reactance of capacitor} = \frac{1}{\omega C}$$

Where $\omega = 2\pi f$

For DC signal, frequency is '0' [$\because$ Time periode of dc is ∞]

$$\therefore \text{Reactance of capacitor} = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 0 \times C} = \infty$$

So, capacitor doesn't allow the dc signal (i.e it offers ∞ reactance to the dc signal) and it allows ac signal (it offers low reactance for ac signal).

Reactance of the Inductor is "ωL", where $\omega = 2\pi f$

$= 2\pi f L$

For dc signal, frequency is '0'

$\therefore$ Reactance of Inductor $= 2\pi \times 0 \times L$

$= 0$

So, it allows the dc signal, but for ac, Inductor offers high reactance, so hence it drops the ac.

Capacitor allows AC, Blocks DC

Inductor allows DC, Blocks AC

By using Inductor and Capacitor principles, we are going to design the filters.

Types of Filters :-

1) Capacitor filter
2) Inductor (or) Choke Filter
3) L - Section (or) Inductor input filter (or) LC Filter
4) π - Section (or) Capacitor input filter (or) CLC Filters.

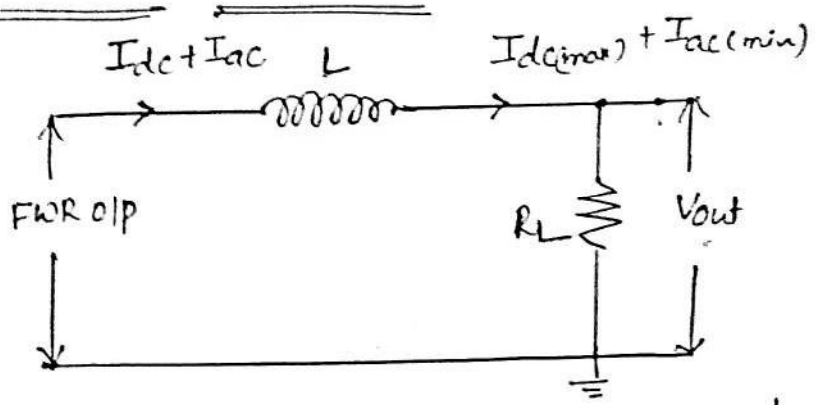
Fourier Series of FWR output is :

$$\frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\theta$$ (for this derivation ref Gate class notes).

$$V_{ac\,rms} = \frac{4V_m}{3\sqrt{2}\pi} \; ; \; V_{dc} = \frac{2V_m}{\pi}$$

$$\therefore \; V_{ac\,rms} = \frac{\sqrt{2}}{3} V_{dc}$$

Inductance (or) Choke Filter:-



FWR output ~~Condition~~ Contains both ac and dc components. Inductor is offered very high reactance for ac and very small reactance for dc component. So Inductor allows max dc component and Smaller ac component.

FWR o/p is expressed by using Fourier series expansion.

Fourier Series of FWR o/p is

$$= \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left[\frac{1}{3}\cos 2\omega t + \frac{1}{15}\cos 4\omega t + \frac{1}{35}\cos 6\omega t + \cdots\right]$$

$$= \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t$$

$$= \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\theta$$

($\frac{4V_m}{3\pi}$ → magnitude of AC component.)

$\frac{2V_m}{\pi}$ ↓ dc component

$\frac{4V_m}{3\pi}\cos 2\theta$ — AC component

From above expansion,

$$V_{dc} = \frac{2V_m}{\pi} \quad \text{——— (1)}$$

$$\text{Mag. of ac component} = \frac{4V_m}{3\pi}$$

$$V_{acrms} = \frac{\text{Magnitude of ac component}}{\sqrt{2}}$$

$$* V_{acrms} = \frac{\frac{4V_m}{3\pi}}{\sqrt{2}} = \frac{4V_m}{3\sqrt{2}\pi} \quad \text{——— (2)}$$

For above Filter Circuit, Impedance ~~Reactance affected by~~ $Z = \sqrt{R_L^2 + X_L^2}$

$$Z = \sqrt{R_L^2 + X_L^2} \quad \text{——— (3)}$$

Where $X_L = 2\omega L$ ——— (3a)

$$\therefore Z = \sqrt{R_L^2 + (2\omega L)^2} \quad \text{——— (4)}$$

$$I_{acrms} = \frac{V_{acrms}}{Z}$$

$$= \frac{4V_m}{\sqrt{2}3\pi\sqrt{R_L^2 + (2\omega L)^2}} \quad (\text{from eqn (2)})$$

$$= \frac{2 \times \overbrace{2V_m}^{V_{dc}}}{3\sqrt{2}\,\pi} \times \frac{1}{\sqrt{R_L^2 + (2\omega L)^2}}$$

$$= \frac{2}{3\sqrt{2}} \cdot V_{dc} \cdot \frac{1}{\sqrt{R_L^2 + (2\omega L)^2}} \quad \left[\because \frac{2V_m}{\pi} = V_{dc}\right]$$

$$= \frac{\sqrt{2}}{3} \cdot V_{dc} \cdot \frac{1}{R_L\sqrt{1 + \left(\frac{2\omega L}{R_L}\right)^2}}$$

$$= \frac{\sqrt{2}}{3} \cdot \frac{V_{dc}}{R_L} \cdot \frac{1}{\sqrt{1 + \left(\frac{2\omega L}{R_L}\right)^2}}$$

$$I_{acrms} = \frac{\sqrt{2}}{3} \cdot I_{dc} \cdot \frac{1}{\sqrt{1 + \left(\frac{2\omega L}{R_L}\right)^2}}$$

$$\frac{I_{acrms}}{I_{dc}} = \frac{\sqrt{2}}{3} \times \frac{1}{\sqrt{1 + \left(\frac{2\omega L}{R_L}\right)^2}} \quad \text{——— (5)}$$

In above equation if $\frac{2\omega L}{R_L} << 1$

$$\therefore \frac{I_{acrms}}{I_{dc}} = \frac{\sqrt{2}}{3} = 0.47$$ (i.e approximately equal to Ripple factor of FWR).

in equations if $\frac{2\omega L}{R_L} \gg 1$

$$\frac{I_{ac\,rms}}{I_{dc}} = \frac{\sqrt{2}}{3 \times \frac{2\omega L}{R_L}}$$

$$\frac{I_{ac\,rms}}{I_{dc}} = \frac{\sqrt{2}\, R_L}{3 \times 2 \times \omega \times L}$$

$$= \frac{R_L}{3\sqrt{2}\,\omega L}$$

$$= \frac{R_L}{3\sqrt{2} \times 2\pi f L}$$

$$\text{Ripple factor} = \frac{I_{ac\,rms}}{I_{dc}} = \frac{R_L}{6\sqrt{2}\,\pi f L} \quad \text{——— (6)}$$

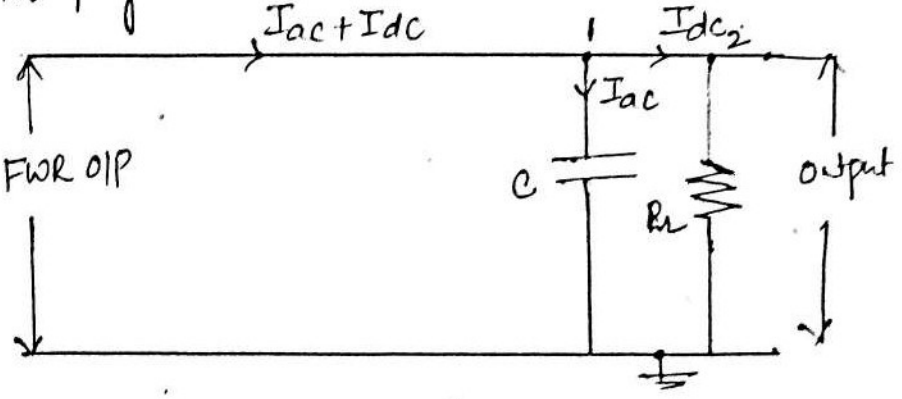
From equ (6) : Ripple factor $\propto R_L$

Ripple factor $\propto \frac{1}{L}$

To get the less ripple factor, we have to chose low value of R_L and High value of Inductance L.

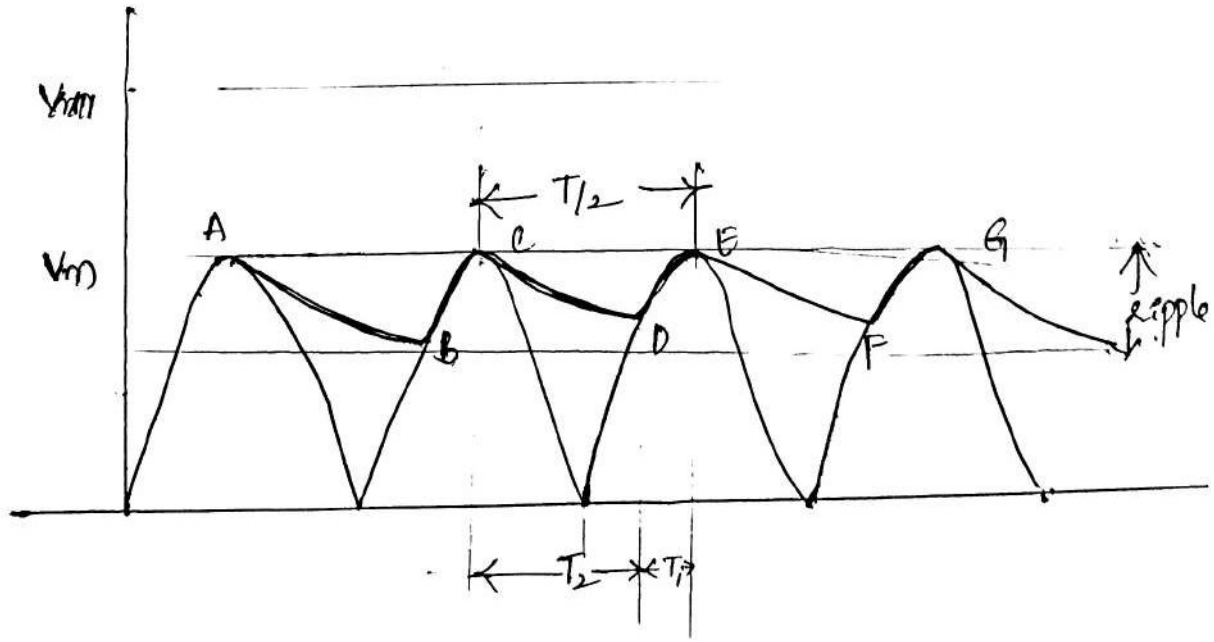
Capacitor Filter :-

Capacitor filter circuit consists of a capacitor 'C' is placed across the rectifier output in parallel with load R_L as shown in Fig.



FWR o/p contains both dc component and some ac component. Capacitor offers low reactance for 'ac' and high reactance for 'dc'. So maximum ac component is passed through capacitor and goes to ground and dc component is not allowed by the capacitor. After node '1', only dc component and small ac component is present.

As the rectifier voltage increases, it charges the capacitor and also supplies current to the load. At the end of the quarter cycle (point 'A' in Fig(2)), the capacitor is charged to the peak value 'V_m' of the rectified voltage. Now the rectified voltage starts to decrease. When voltage starts to decrease capacitor discharges through load and voltage across it decreases as shown by the line AB shown in Fig (2). The voltage across load will decrease only slightly because immediately the next voltage peak comes and so again charges the capacitor. This process is repeated again and again and the output voltage wave form becomes ABCDEFG... as shown in Fig(2) Seen that very small ripple is left in the output.



Capacitance $C = \frac{Q_{charge}}{V_m}$

$$Q_{charge} = C \cdot V_m \quad \text{——— (1)}$$

discharging current i.e $I_{dc} = \frac{Q_{discharge}}{\text{discharge Time}}$

$$I_{dc} = \frac{Q_{discharge}}{T_2}$$ where T_2 is the discharge time as shown in Fig 2.

$$Q_{discharge} = I_{dc} \cdot T_2 \quad \text{——— (2)}$$

From above Fig 2, Time period is $T/2 = T_2 + T_1$ → Charging time
↙ discharging time

From above fig(2), charging time is negligible as compare to discharging time

$$\therefore T/2 \simeq T_2 \quad \text{— (3)}$$

Sub eqn(3) in eqn(2)

$$Q_{discharge} = I_{dc} \cdot T/2$$

$$= \frac{I_{dc} \cdot T}{2} \quad \text{where } T = \frac{1}{f}$$

$$Q_{discharge} = \frac{I_{dc}}{2f} \quad \text{— (4)}$$

equating (1) and (4)

$$C \cdot V_m = \frac{I_{dc}}{2f}$$

$$V_m = \frac{I_{dc}}{2fC} \quad \text{— (5)}$$

Ripple of the output is approximately triangular wave.

RMS value of triangular wave $= \frac{V_m}{2\sqrt{3}}$

$$V_{acrms} = \frac{V_m}{2\sqrt{3}} \quad \text{— (6)}$$

Sub eqn (5) in eqn (6)

$$V_{acrms} = \frac{I_{dc}}{4\sqrt{3}fC} \quad \text{— (7)}$$

Where $I_{dc} = \frac{V_{dc}}{R_L}$ — (8)

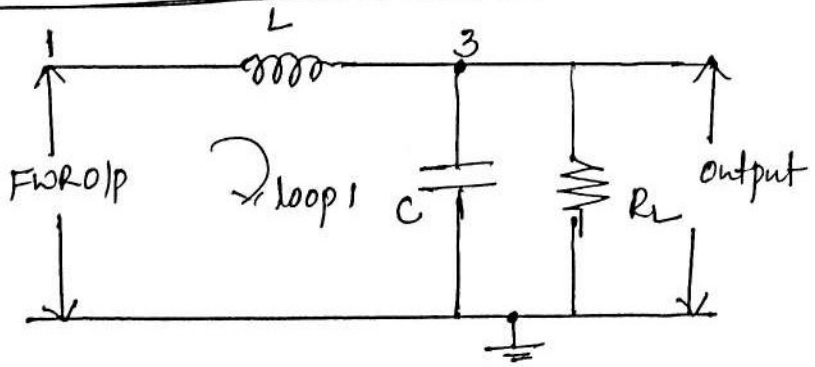
Substitute eqn (8) in eqn (7)

$$\therefore V_{acrms} = \frac{V_{dc}}{4\sqrt{3}fCR_L}$$

$$\text{Ripple factor} = \frac{V_{acrms}}{V_{dc}} = \frac{1}{4\sqrt{3}fCR_L}$$

Capacitor filter is extremly popular because of its low cost, small size, little weight and good characteristics. For small load currents (upto 50mA) this type of filter is preferred.

L-section (or) LC (or) Inductor Input Filter:-



at node 1: $V_{1acrms} = \frac{4V_m}{3\pi\sqrt{2}}$

V_{1acrms} in Loop 1 is $V_{1acrms} = I_{1acrms} \cdot Z$

Where $Z = \sqrt{X_L^2 + X_C^2}$

For ac X_C is negligible as compared to X_L [$\because X_L \propto f$; $X_C \propto \frac{1}{f}$]

$\therefore Z = X_L$

$$I_{1acrms} = \frac{V_{1acrms}}{X_L} \quad \text{where } V_{1acrms} = \frac{4V_m}{3\sqrt{2}\pi}$$

$$\text{where } X_L = 2\omega L$$

Voltage drop across the capacitor $V_{3acrms} = I_{1acrms} \cdot X_C$

$$V_{3acrms} = \frac{V_{1acrms}}{X_L} \cdot X_C \quad \left[\because I_{1acrms} = \frac{V_{1acrms}}{X_L}\right]$$

$$V_{3acrms} = \frac{4V_m}{3\sqrt{2}\pi} \cdot \frac{X_C}{X_L}$$

$$= \frac{\pi\sqrt{2}}{3\sqrt{2}} \times \frac{2V_m}{\pi} \cdot \frac{X_C}{X_L}$$

$$= \frac{\sqrt{2}}{3} \cdot V_{dc} \cdot \frac{X_C}{X_L} \quad \text{where } V_{dc} = \frac{2V_m}{\pi}$$

$$\therefore \text{Ripple factor} = \frac{V_{3acrms}}{V_{dc}} = \frac{\sqrt{2}}{3} \cdot \frac{X_C}{X_L}$$

$$= \frac{\sqrt{2}}{3} \cdot \frac{1}{2\omega C \cdot 2\omega L}$$

$$= \frac{\sqrt{2}}{3 \times 4\omega^2 C^2 L^2}$$

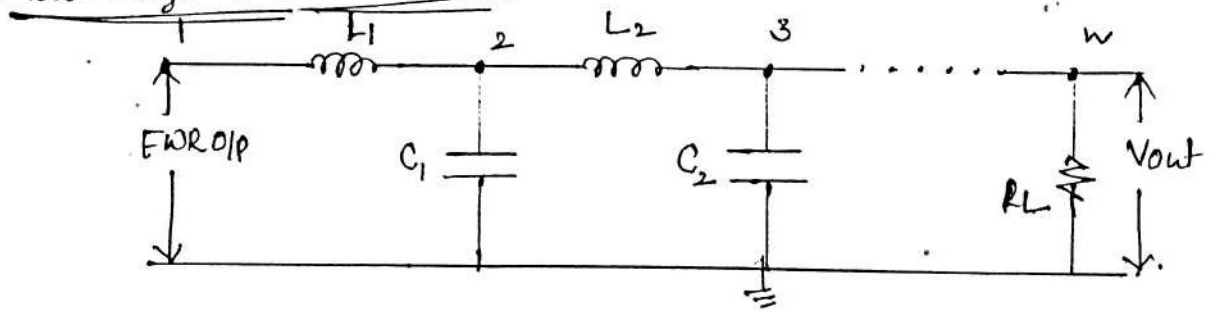
$$= \frac{\sqrt{2}}{3} \cdot \frac{1}{4(2\pi f)^2 \cdot LC}$$

$$= \frac{\sqrt{2}}{3} \cdot \frac{1}{16\pi^2 f^2 LC}$$

$$\text{Ripple factor} = \frac{V_{3acrms}}{V_{dc}} = \frac{1}{24\sqrt{2}\pi^2 f^2 LC}$$

In L section filters to get minimum ripple factor L and C values are selected as high values.

Multi Stage L-section Filters:-



$$V_{1acrms} = I_{1acrms} \cdot Z$$

$$= I_{1acrms} \cdot \sqrt{X_{L_1}^2 + X_{C_1}^2}$$

$$V_{1acrms} = I_{1acrms} \cdot X_{L_1}.$$

$$I_{1acrms} = \frac{V_{1acrms}}{X_{L_1}} \quad \text{——— (1)}$$

$$V_{2acrms} = I_{1acrms} \cdot X_{C_1}$$

$$V_{2acrms} = \frac{V_{1acrms}}{X_{L_1}} \cdot X_{C_1} \quad \text{——— (2)}$$

$$V_{2acrms} = I_{2acrms} \cdot X_{L_2}$$

$$I_{2acrms} = \frac{V_{2acrms}}{X_{L_2}} \quad \text{——— (3)}$$

$$V_{3acrms} = I_{2acrms} \cdot X_{C_2}$$

$$= \frac{V_{2acrms}}{X_{L_2}} \cdot X_{C_2} \text{ (from equ (2))}$$

$$= V_{1acrms} \cdot \frac{X_{C_1}}{X_{L_1}} \cdot \frac{X_{C_2}}{X_{L_2}}$$

$$V_{1acrms} = \frac{4V_m}{3\sqrt{2}\pi} = \frac{\sqrt{2}}{3} V_{dc}.$$

$$V_{3acrms} = \frac{\sqrt{2}}{3} V_{dc} \cdot \frac{X_{C_1}}{X_{L_1}} \cdot \frac{X_{C_2}}{X_{L_2}}$$

Ripple factor $= \frac{V_{2acrms}}{V_{dc}} = \frac{\sqrt{2}}{3} \frac{X_{C_1}}{X_{L_1}} \cdot \frac{X_{C_2}}{X_{L_2}}$ where $X_{C_1} = X_{C_2} = X_C$.

$X_{L_1} = X_{L_2} = X_L$.

Ripple factor $= \frac{\sqrt{2}}{3} \left(\frac{X_C}{X_L}\right)^2$ for two stages

For 'n' Stage :

Ripple factor $= \frac{\sqrt{2}}{3} \left(\frac{X_C}{X_L}\right)^n$ where 'n' is no. of stages.

CRITICAL INDUCTANCE :-

Fourier Series of FWR is $\frac{2V_m}{\pi} - \frac{4V_m}{3\pi} \cos 2\omega t$.

In above expression first term corresponds to dc voltage. Second term corresponds to ac voltage. Magnitude of dc voltage is greater than the magnitude of ac voltage in Fourier Series of FWR output. So current due to dc component is greater than the magnitude of ac component.

$I_{dc} \geq I_m$

$I_{dc} \geq \sqrt{2} I_{acrms}$ ——— (1)

where $I_{acrms} = \frac{V_{acrms}}{X_L} = \frac{4V_m}{3\sqrt{2}\pi} \times \frac{1}{X_L}$

$I_{acrms} = \frac{\sqrt{2}}{3} \frac{V_{dc}}{X_L}$ ——— (2)

Sub equ (2) in equ (1)

$I_{dc} \geq \sqrt{2} \times \frac{\sqrt{2}}{3} \frac{V_{dc}}{X_L}$

$I_{dc} \geq \frac{2}{3} \frac{V_{dc}}{X_L}$

$\frac{V_{dc}}{R_L} \geq \frac{2}{3} \frac{V_{dc}}{X_L}$

$$X_L \geq \frac{2}{3} \cdot R_L$$

Where X_L is the reactance of Inductance i.e $2\pi L$

$$2\pi L \geq \frac{2}{3} \cdot R_L$$

$$L \geq \frac{R_L}{3\omega}$$

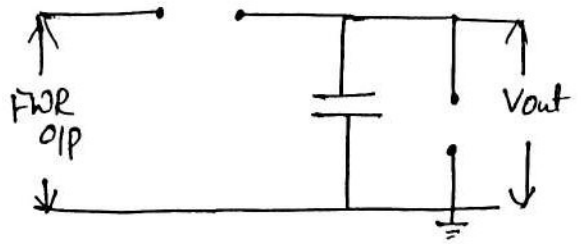
The value of Inductance 'L' in L-section filter must be kept above certain minimum value i.e $\frac{R_L}{3\omega}$ which is called "Critical Inductance". Critical Inductance depends on load resistance and Supply frequency ω i.e $2\pi f$

$$\therefore \text{Critical Inductance } L_C \geq \frac{R_L}{3\omega}$$

BLEEDER RESISTANCE :-

$$\text{Critical Inductance } L_C \geq \frac{R_L}{3\omega}$$

Where R_L is '∞' i.e load terminal is opened, L value also becomes infinite from above expression. So for R_L is ∞, in L-Section filter L is also open as shown in below.



When both terminals are opened there is no current flowing in the ckt and for capacitor there is no discharging path.

For avoiding above problem, Resistance is connected in parallel to load resistance. That resistance is called as "Bleeder resistance".

If/16ad When Bleeder resistance is connected, even Load Resistance becomes ∞, Inductance value not ∞ as shown in below.

Total load Resistance is considered as R_L in parallel with R_B.

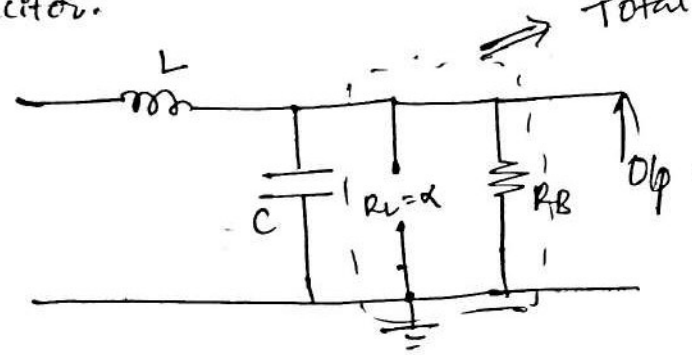
i.e $\frac{R_L R_B}{R_L + R_B} \quad \frac{R_L R_B}{R_L(1 + R_B/R_L)}$ When $R_L \to \infty$.

$R_{eqn} = R_B$

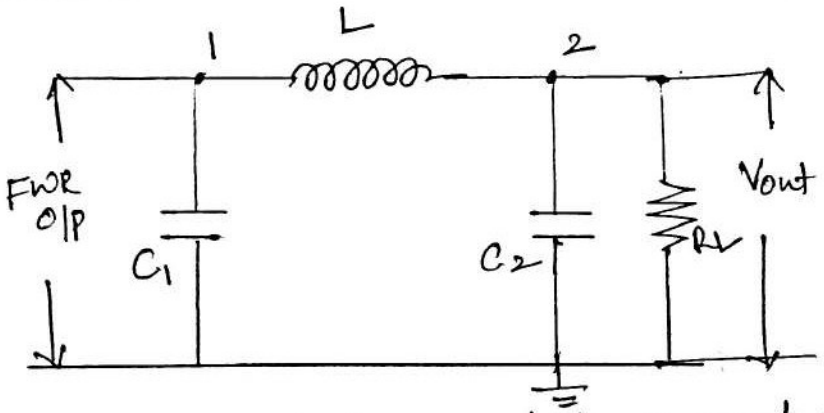
∴ According to critical Inductance.

$$L_C \geq \frac{R_B}{3\omega}$$

If load is opened, Inductance is not opened because R_B is exist in o/p. So current is Bleeding (flowing) through the resistance R_B, and R_B providing the discharging path to Capacitor.



TT-section Filter :-



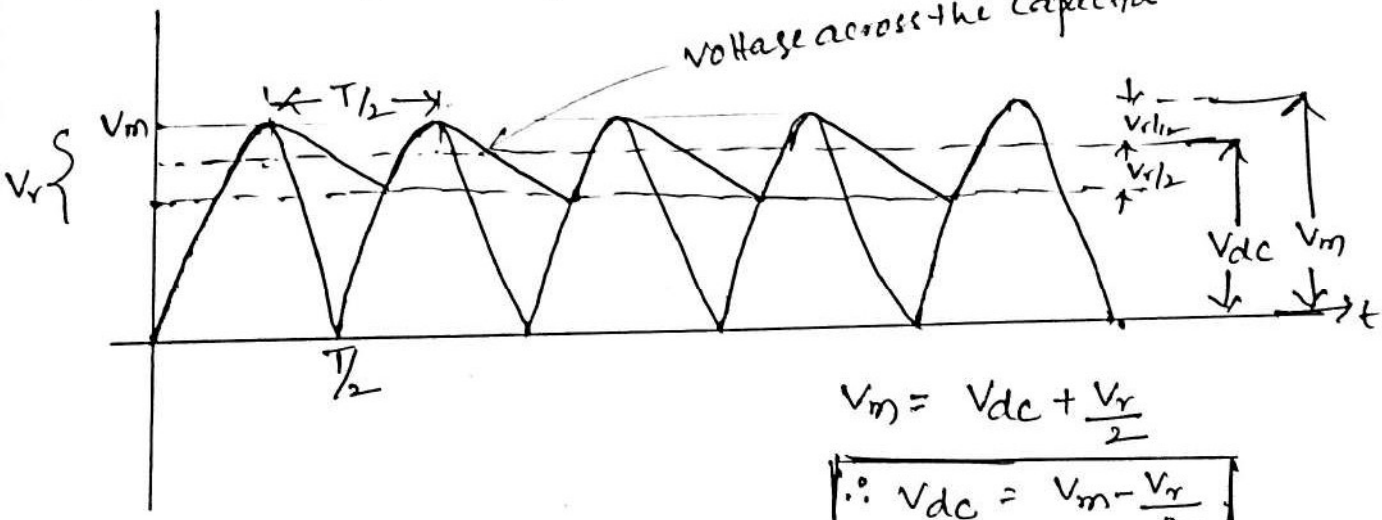
FWR output Contains both ac and dc component is applied to i/p terminals of the filter. Here the filtering action of three Components C_1, L, C_2 is discussed in below.

a) Capacitor 'C_1' offers Low reactance to ac component of FWR output, while it offers Infinite reactance to the dc component of FWR output. Therefore, Capacitor 'C_1' allows maximum ac component while the dc component move towards Inductor L.

b) The Inductor 'L' offers high reactance to the dc component. Therefore, it allows the dc component, while the un bypassed ac component is blocked.

c) The capacitor 'C_2' by passes the ac component which the inductor has failed to block. Therefore, only dc component appears across the load and that is what we desire.

In π section filter voltage appears across the capacitor 'C_1' terminal is approximately triangular wave is shown in fig(2).



$$V_m = V_{dc} + \frac{V_r}{2}$$

$$\therefore V_{dc} = V_m - \frac{V_r}{2}$$

Fig2: Voltage across the capacitor C_1.

Fourier Series of Triangular wave is given by

$$= \underbrace{\frac{V_r}{2}}_{dc} - \underbrace{\frac{V_r}{\pi} \sin 2\omega t}_{\text{neg of ac}} \rightarrow ac$$

Where $V_r = \frac{I_{dc}}{2fC_1}$ (ref Capacitor filter derivation)

$\therefore$ Magnitude of ac component is $\frac{V_r}{\pi} = \frac{I_{dc}}{2\pi f C_1}$.

$$\text{Vacrms value} = \frac{\text{Magnitude of 'ac' component}}{\sqrt{2}} = \frac{V_r}{\sqrt{2}\pi}$$

$$= \frac{I_{dc}}{\sqrt{2}\, 2\pi f C_1}$$

$$V_{1acrms} = \frac{I_{dc} \times 2}{\sqrt{2} \times 2\pi f C_1 \times 2}$$ multiply and divide by 2

$$V_{1acrms} = \frac{I_{dc} \times 2}{\sqrt{2} \times 2\pi f C_1 \times 2}$$

$$= \frac{I_{dc} \times 2}{\sqrt{2} \times 2 \times \omega C_1}$$ where $2\pi f = \omega$

$$= \frac{2 I_{dc}}{\sqrt{2} \times 2\omega C_1}$$ where $\frac{1}{2\omega C_1} = X_{C_1}$

$$V_{1acrms} = \sqrt{2}\, I_{dc} \cdot X_{C_1} \quad \text{——— (1)}$$

For From first loop of the Filter

$$V_{1acrms} = I_{1acrms} \cdot Z$$ where I_{1acrms} is current flowing in first loop

$$Z = \sqrt{X_{L_1}^2 + X_{C_2}^2}$$

for ac component X_{C_2} is negligible.

$\therefore Z = X_{L_1}$.

$$V_{1acrms} = I_{1acrms} \cdot X_{L_1}$$

$$\therefore I_{1acrms} = \frac{V_{1acrms}}{X_{L_1}} \quad \text{——— (2)}$$

Subsequently

And voltage across the 'C_2' i.e at node 2 is

$$V_{2\,acrms} = V_{1acrms} \cdot XC_2 \quad \text{---- (3)}$$

Sub eqn (2) in eqn (3)

$$V_{2\,acrms} = \frac{V_{1acrms}}{XL_1} \cdot XC_2 \quad \text{---- (4)}$$

Sub eqn (1) in eqn (4)

$$\therefore V_{2\,acrms} = \frac{V_2 \cdot I_{dc} \cdot XC_1 \cdot XC_2}{XL_1}$$

where $I_{dc} = \frac{V_{dc}}{R_L}$

$$\therefore V_{2\,acrms} = \frac{\sqrt{2} \cdot V_{dc} \cdot XC_1 \cdot XC_2}{R_L \cdot XL_1}$$

$$\therefore \text{Ripple factor} = \frac{V_{2acrms}}{V_{dc}} = \frac{\sqrt{2} \cdot XC_1 \cdot XC_2}{R_L \cdot XL_1}$$

where $XC_1 = \frac{1}{2\omega C_1}$; $XC_2 = \frac{1}{2\omega C_2}$ and $XL_1 = 2\omega L_1$.

In all filters π-section ~~filter~~ filter gives almost dc wave to the load. If any small ripple is presenting in output of the π section filter, that ripple is eliminating by using "Regulators".

Problems

1. Half wave rectifier, having a resistance load of 1000Ω, rectifies an alternating voltage of 325V peak value and the diode has a forward resistance of 100Ω. Calculate:
   a) peak, average and rms value of current.
   b) dc power output
   c) ac input power and
   (d) efficiency of the rectifier.

2. A HWR has a load of 3.5KΩ. If the diode resistance and secondary coil resistance together have a resistance of 800Ω and the input voltage has a signal voltage of peak value 240V, Calculate:
   i) peak, average and rms value of current flowing
   ii) DC power output
   iii) ac power input
   iv) efficiency of the rectifier.

3. A HWR is used to supply 24VDC to a resistive load of 500Ω and the diode has a forward resistance of 50Ω. Calculate the maximum value of the ac voltage required at input.

4. An ac supply of 230V is supplied to a HWR circuit through transformer of turns ratio 5:1. Assume the diode is an ideal one. The load resistance is 300Ω. Find i) dc output voltage ii) PIV iii) maximum and average values of power delivered to the load.

5. A 230V, 60Hz voltage is applied to the primary of a 5:1 stepdown, center-tap transformer used in a FWR having a load of 900Ω. If the diode resistance and secondary

Coil resistance together has a resistance of 1Ω, determine a) dc voltage across the load, b) dc current flowing through the load, c) dc power delivered to the load d) PIV across each diode e) ripple voltage, and its frequency.

6. In a Bridge rectifier, the transformer is connected to 200 V, 60Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diode is ideal, find a) I_{dc} b) voltage across the load c) PIV.

7. Calculate the value of Inductance to use in the Inductor filter connected to a FWR operating at 60Hz to provide a dc output with 4% ripple for a load of 100Ω.

8. Calculate the value of Capacitance to use in a Capacitor filter connected to a fullwave rectifier operating at a Standard aircraft power frequency of 400Hz, if the ripple factor is 10% for a load of 500Ω.

9. A 15-0-15 volts (rms) ideal transformer is used with a FWR circuit with diodes having forward drop of 1volts. The load is a resistance of 100Ω and a Capacitor of 10,000μF is used as a filter across the load resistance. Calculate the dc load current and voltage.

10. Design a filter for fullwave circuit with LC filter to provide an output voltage of 10V with a load current of 200mA and the ripple is limited to 2%.

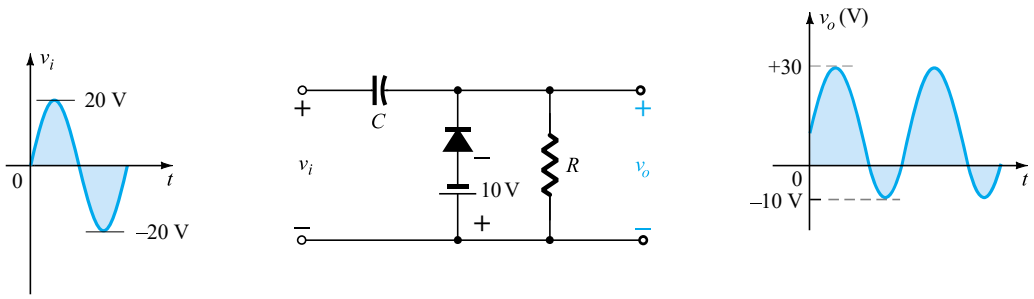


Figure 2.104 Clamping network with a sinusoidal input.

2.11 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to that applied to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Unless otherwise specified, the Zener model to be employed for the "on" state will be as shown in Fig. 2.105a. For the "off" state as defined by a voltage less than V_Z but greater than 0 V with the polarity indicated in Fig. 2.105b, the Zener equivalent is the open circuit that appears in the same figure.

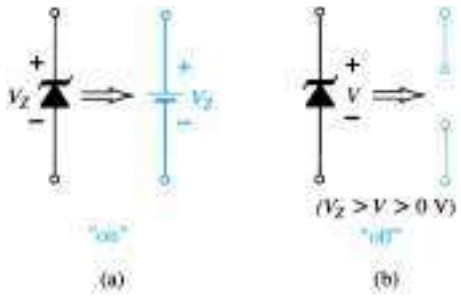


Figure 2.105 Zener diode equivalents for the (a) "on" and (b) "off" states.

V_i and R

The simplest of Zener diode networks appears in Fig. 2.106. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. *Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.*

Applying step 1 to the network of Fig. 2.106 will result in the network of Fig. 2.107, where an application of the voltage divider rule will result in

$$V = V_L = \frac{R_L V_i}{R + R_L} \tag{2.16}$$

If $V \geq V_Z$, the Zener diode is "on" and the equivalent model of Fig. 2.105a can be substituted. If $V < V_Z$, the diode is "off" and the open-circuit equivalence of Fig. 2.105b is substituted.

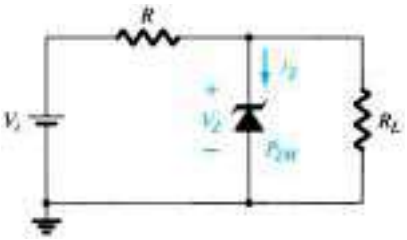


Figure 2.106 Basic Zener regulator.

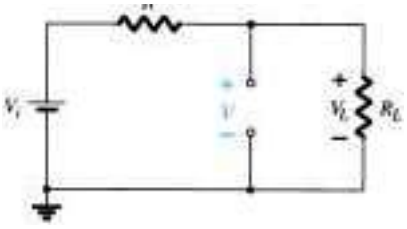


Figure 2.107 Determining the state of the Zener diode.

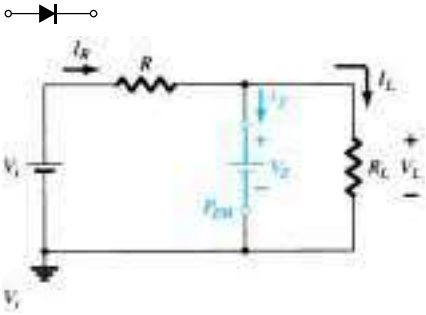


Figure 2.108 Substituting the Zener equivalent for the "on" situation.

2. Substitute the appropriate equivalent circuit and solve for the desired unknowns.

For the network of Fig. 2.106, the "on" state will result in the equivalent network of Fig. 2.108. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \tag{2.17}$$

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and

$$I_Z = I_R - I_L \tag{2.18}$$

where

$$I_L = \frac{V_L}{R_L} \quad \textit{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z \tag{2.19}$$

which must be less than the P_{ZM} specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the *state of the Zener diode.* If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn "on" as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.

Zener diodes are most frequently used in *regulator* networks or as a *reference* voltage. Figure 2.106 is a simple regulator designed to maintain a fixed voltage across the load R_L. For values of applied voltage greater than required to turn the Zener diode "on," the voltage across the load will be maintained at V_Z volts. If the Zener diode is employed as a reference voltage, it will provide a level for comparison against other voltages.

EXAMPLE 2.26

(a) For the Zener diode network of Fig. 2.109, determine V_L, V_R, I_Z, and P_Z.
(b) Repeat part (a) with $R_L = 3\ \text{k}\Omega$.

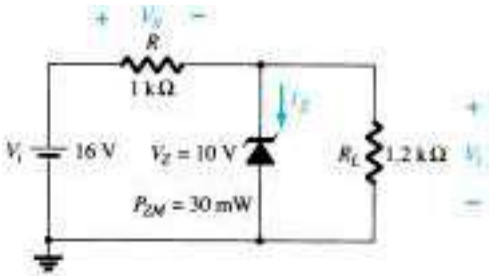


Figure 2.109 Zener diode regulator for Example 2.26.

Solution

(a) Following the suggested procedure the network is redrawn as shown in Fig. 2.110. Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 1.2\ \text{k}\Omega} = 8.73\ \text{V}$$

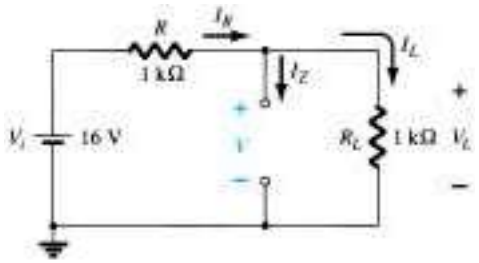


Figure 2.110 Determining V for the regulator of Fig. 2.109.

Since $V = 8.73$ V is less than $V_Z = 10$ V, the diode is in the "off" state as shown on the characteristics of Fig. 2.111. Substituting the open-circuit equivalent will result in the same network as in Fig. 2.110, where we find that

$$V_L = V = \mathbf{8.73\ V}$$

$$V_R = V_i - V_L = 16\ V - 8.73\ \text{V} = \mathbf{7.27\ V}$$

$$I_Z = \mathbf{0\ A}$$

and

$$P_Z = V_Z I_Z = V_Z(0\ \text{A}) = \mathbf{0\ W}$$

(b) Applying Eq. (2.16) will now result in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 3\ \text{k}\Omega} = 12\ \text{V}$$

Since $V = 12$ V is greater than $V_Z = 10$ V, the diode is in the "on" state and the network of Fig. 2.112 will result. Applying Eq. (2.17) yields

$$V_L = V_Z = \mathbf{10\ V}$$

and

$$V_R = V_i - V_L = 16\ \text{V} - 10\ \text{V} = \mathbf{6\ V}$$

with

$$I_L = \frac{V_L}{R_L} = \frac{10\ \text{V}}{3\ \text{k}\Omega} = 3.33\ \text{mA}$$

and

$$\text{I}_R = \frac{V_R}{R} = \frac{6\ \text{V}}{1\ \text{k}\Omega} = 6\ \text{mA}$$

so that

$$I_Z = I_R - I_L\ \text{[Eq. (2.18)]}$$

$$= 6\ \text{mA} - 3.33\ \text{mA}$$

$$= \mathbf{2.67\ mA}$$

The power dissipated,

$$P_Z = V_Z I_Z = (10\ \text{V})(2.67\ \text{mA}) = \mathbf{26.7\ mW}$$

which is less than the specified $P_{ZM} = 30$ mW.

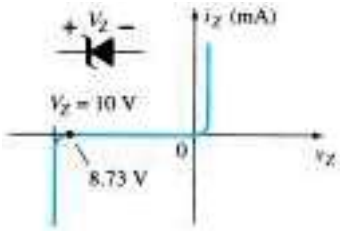


Figure 2.111 Resulting operating point for the network of Fig. 2.109.

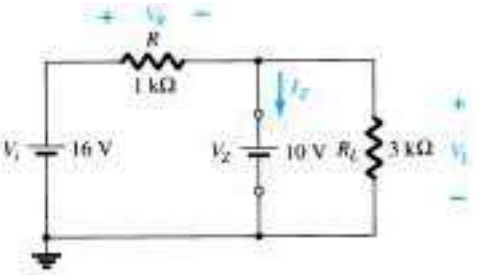


Figure 2.112 Network of Fig. 2.109 in the "on" state.

Fixed V_i, Variable R_L

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) which will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z, and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.106 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} \tag{2.20}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent.

The condition defined by Eq. (2.20) establishes the minimum R_L but in turn specifies the maximum I_L as

$$I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}} \tag{2.21}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z \tag{2.22}$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R} \tag{2.23}$$

The Zener current

$$I_Z = I_R - I_L \tag{2.24}$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{\min}} = I_R - I_{ZM} \tag{2.25}$$

and the maximum load resistance as

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} \tag{2.26}$$

EXAMPLE 2.27

(a) For the network of Fig. 2.113, determine the range of R_L and I_L that will result in V_{R_L} being maintained at 10 V.
(b) Determine the maximum wattage rating of the diode.

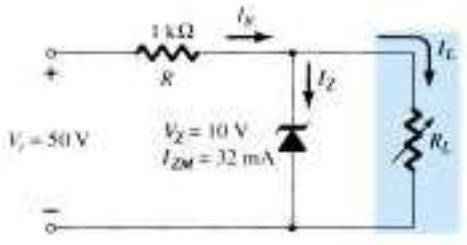


Figure 2.113 Voltage regulator for Example 2.27.

Solution

(a) To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\text{ k}\Omega)(10\text{ V})}{50\text{ V} - 10\text{ V}} = \frac{10\text{ k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\text{ V} - 10\text{ V} = \mathbf{40\ V}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\text{ V}}{1\text{ k}\Omega} = \mathbf{40\ mA}$$

The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{\min}} = I_R - I_{ZM} = 40\text{ mA} - 32\text{ mA} = \mathbf{8\ mA}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} = \frac{10\text{ V}}{8\text{ mA}} = \mathbf{1.25\ k\Omega}$$

A plot of V_L versus R_L appears in Fig. 2.114a and for V_L versus I_L in Fig. 2.114b.

(b) $P_{\max} = V_Z I_{ZM}$
$= (10\text{ V})(32\text{ mA}) = \mathbf{320\ mW}$

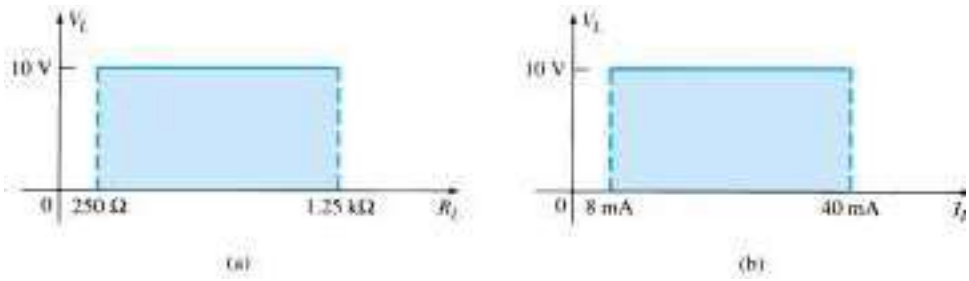


Figure 2.114 V_L versus R_L and I_L for the regulator of Fig. 2.113.

Fixed R_L, Variable V_i

For fixed values of R_L in Fig. 2.106, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

and

$$V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} \tag{2.27}$$

The maximum value of V_i is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$I_{R_{max}} = I_{ZM} + I_L \tag{2.28}$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i_{max}} = V_{R_{max}} + V_Z$$

$$V_{i_{max}} = I_{R_{max}}R + V_Z \tag{2.29}$$

EXAMPLE 2.28

Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.115 in the "on" state.

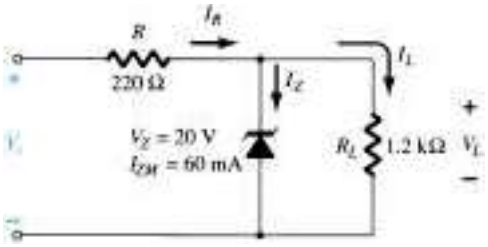


Figure 2.115 Regulator for Example 2.28.

Solution

$$\text{Eq. (2.27):}\quad V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\ \Omega + 220\ \Omega)(20\ \text{V})}{1200\ \Omega} = \mathbf{23.67\ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\ \text{V}}{1.2\ \text{k}\Omega} = 16.67\ \text{mA}$$

$$\text{Eq. (2.28):}\quad I_{R_{max}} = I_{ZM} + I_L = 60\ \text{mA} + 16.67\ \text{mA}$$

$$= 76.67\ \text{mA}$$

$$\text{Eq. (2.29):}\quad V_{i_{max}} = I_{R_{max}}R + V_Z$$

$$= (76.67\ \text{mA})(0.22\ \text{k}\Omega) + 20\ \text{V}$$

$$= 16.87\ \text{V} + 20\ \text{V}$$

$$= \mathbf{36.87\ V}$$

A plot of V_L versus V_i is provided in Fig. 2.116.

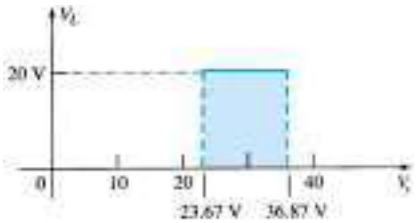


Figure 2.116 V_L versus V_i for the regulator of Fig. 2.115.

2.9 CLIPPERS

There are a variety of diode networks called *clippers* that have the ability to "clip" off a portion of the input signal without distorting the remaining part of the alternating waveform. The half-wave rectifier of Section 2.7 is an example of the simplest form of diode clipper—one resistor and diode. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off.

There are two general categories of clippers: *series* and *parallel*. The series configuration is defined as one where the diode is in series with the load, while the parallel variety has the diode in a branch parallel to the load.

Series

The response of the series configuration of Fig. 2.67a to a variety of alternating waveforms is provided in Fig. 2.67b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper. The addition of a dc supply such as shown in Fig. 2.68 can have a pronounced effect on the output of a clipper. Our initial discussion will be limited to ideal diodes, with the effect of V_T reserved for a concluding example.

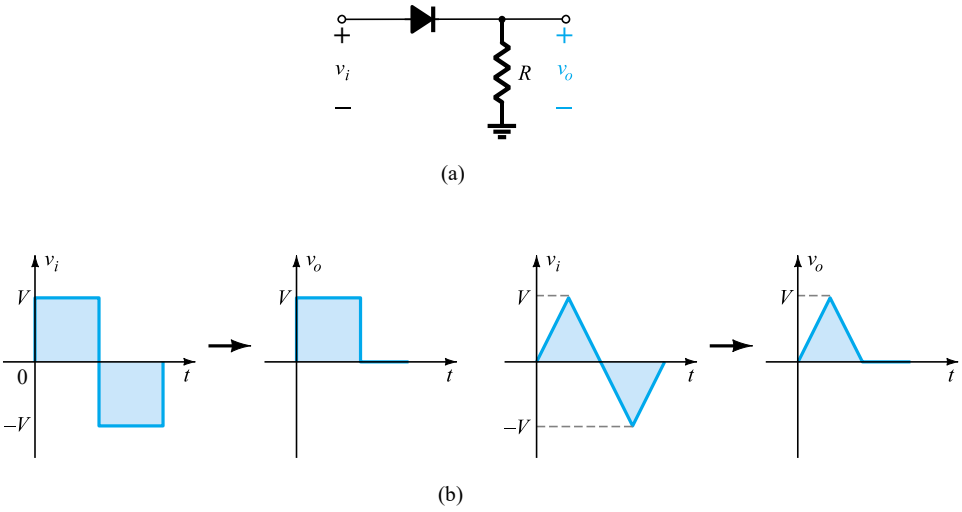


Figure 2.67 Series clipper.

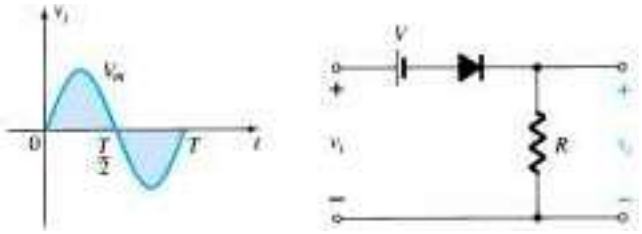


Figure 2.68 Series clipper with a dc supply.

There is no general procedure for analyzing networks such as the type in Fig. 2.68, but there are a few thoughts to keep in mind as you work toward a solution.

1. *Make a mental sketch of the response of the network based on the direction of the diode and the applied voltage levels.*

For the network of Fig. 2.68, the direction of the diode suggests that the signal v_i must be positive to turn it on. The dc supply further requires that the voltage v_i be greater than V volts to turn the diode on. The negative region of the input signal is

"pressuring" the diode into the "off" state, supported further by the dc supply. In general, therefore, we can be quite sure that the diode is an open circuit ("off" state) for the negative region of the input signal.

2. *Determine the applied voltage (transition voltage) that will cause a change in state for the diode.*

For the ideal diode the transition between states will occur at the point on the characteristics where $v_d = 0$ V and $i_d = 0$ A. Applying the condition $i_d = 0$ at $v_d = 0$ to the network of Fig. 2.68 will result in the configuration of Fig. 2.69, where it is recognized that the level of v_i that will cause a transition in state is

$$v_i = V \tag{2.14}$$

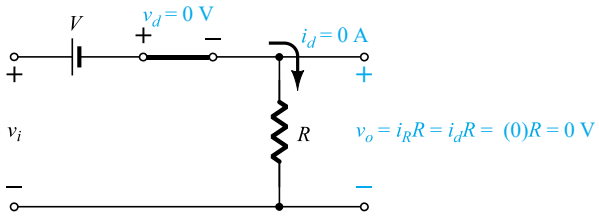


Figure 2.69 Determining the transition level for the circuit of Fig. 2.68.

For an input voltage greater than V volts the diode is in the short-circuit state, while for input voltages less than V volts it is in the open-circuit or "off" state.

3. *Be continually aware of the defined terminals and polarity of v_o.*

When the diode is in the short-circuit state, such as shown in Fig. 2.70, the output voltage v_o can be determined by applying Kirchhoff's voltage law in the clockwise direction:

$$v_i - V - v_o = 0 \text{ (CW direction)}$$

and

$$v_o = v_i - V \tag{2.15}$$

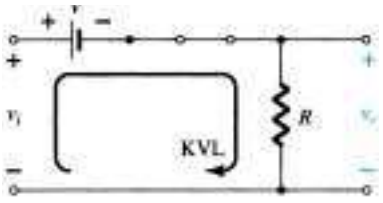


Figure 2.70 Determining v_o.

4. *It can be helpful to sketch the input signal above the output and determine the output at instantaneous values of the input.*

It is then possible that the output voltage can be sketched from the resulting data points of v_o as demonstrated in Fig. 2.71. Keep in mind that at an instantaneous value of v_i the input can be treated as a dc supply of that value and the corresponding dc value (the instantaneous value) of the output determined. For instance, at $v_i = V_m$ for the network of Fig. 2.68, the network to be analyzed appears in Fig. 2.72. For $V_m > V$ the diode is in the short-circuit state and $v_o = V_m - V$, as shown in Fig. 2.71.

At $v_i = V$ the diodes change state; at $v_i = -V_m$, $v_o = 0$ V; and the complete curve for v_o can be sketched as shown in Fig. 2.73.

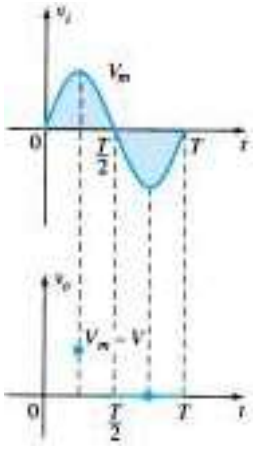


Figure 2.71 Determining levels of v_o.

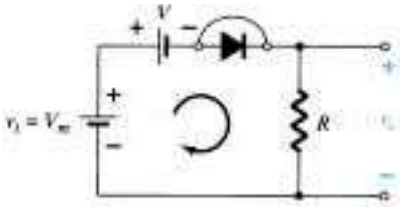


Figure 2.72 Determining v_o when $v_i = V_m$.

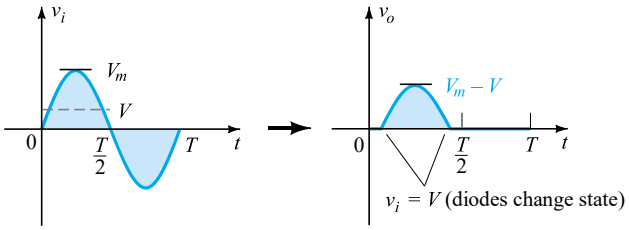


Figure 2.73 Sketching v_o.

EXAMPLE 2.20

Determine the output waveform for the network of Fig. 2.74.

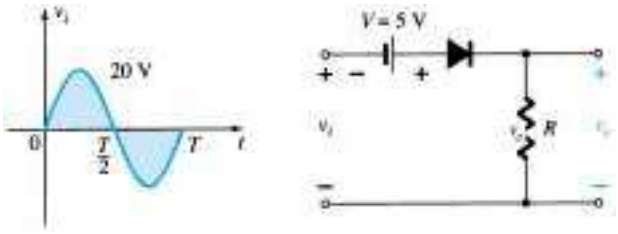


Figure 2.74 Series clipper for Example 2.20.

Solution

Past experience suggests that the diode will be in the "on" state for the positive region of v_i—especially when we note the aiding effect of $V = 5$ V. The network will then appear as shown in Fig. 2.75 and $v_o = v_i + 5$ V. Substituting $i_d = 0$ at $v_d = 0$ for the transition levels, we obtain the network of Fig. 2.76 and $v_i = -5$ V.

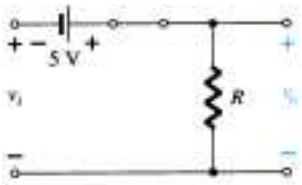


Figure 2.75 v_o with diode in the "on" state.

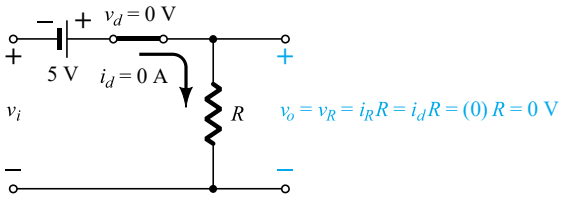


Figure 2.76 Determining the transition level for the clipper of Fig. 2.74.

For v_i more negative than -5 V the diode will enter its open-circuit state, while for voltages more positive than -5 V the diode is in the short-circuit state. The input and output voltages appear in Fig. 2.77.

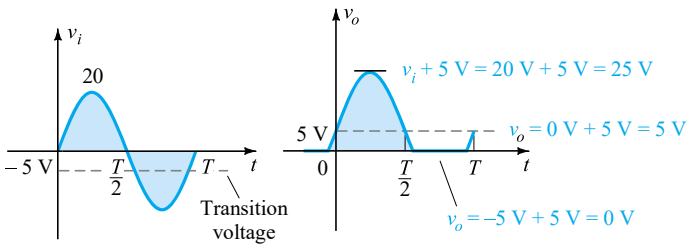


Figure 2.77 Sketching v_o for Example 2.20.

The analysis of clipper networks with square-wave inputs is actually easier to analyze than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting output v_o plotted in the proper time frame.

Repeat Example 2.20 for the square-wave input of Fig. 2.78.

EXAMPLE 2.21

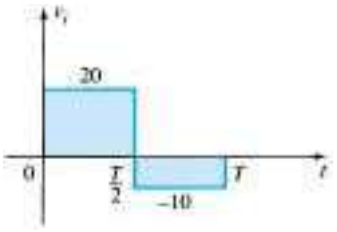


Figure 2.78 Applied signal for Example 2.21.

Solution

For $v_i = 20$ V $(0 \rightarrow T/2)$ the network of Fig. 2.79 will result. The diode is in the short-circuit state and $v_o = 20$ V + 5 V = 25 V. For $v_i = -10$ V the network of Fig. 2.80 will result, placing the diode in the "off" state and $v_o = i_R R = (0)R = 0$ V. The resulting output voltage appears in Fig. 2.81.

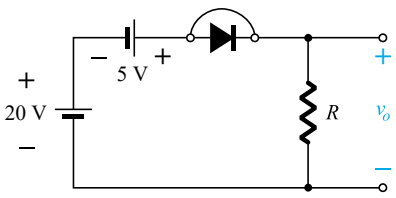


Figure 2.79 v_o at $v_i = +20$ V.

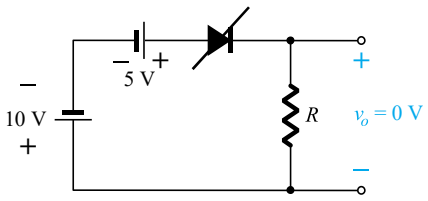


Figure 2.80 v_o at $v_i = -10$ V.

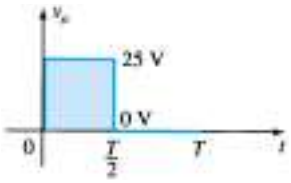


Figure 2.81 Sketching v_o for Example 2.21.

Note in Example 2.21 that the clipper not only clipped off 5 V from the total swing but raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.82 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.67. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

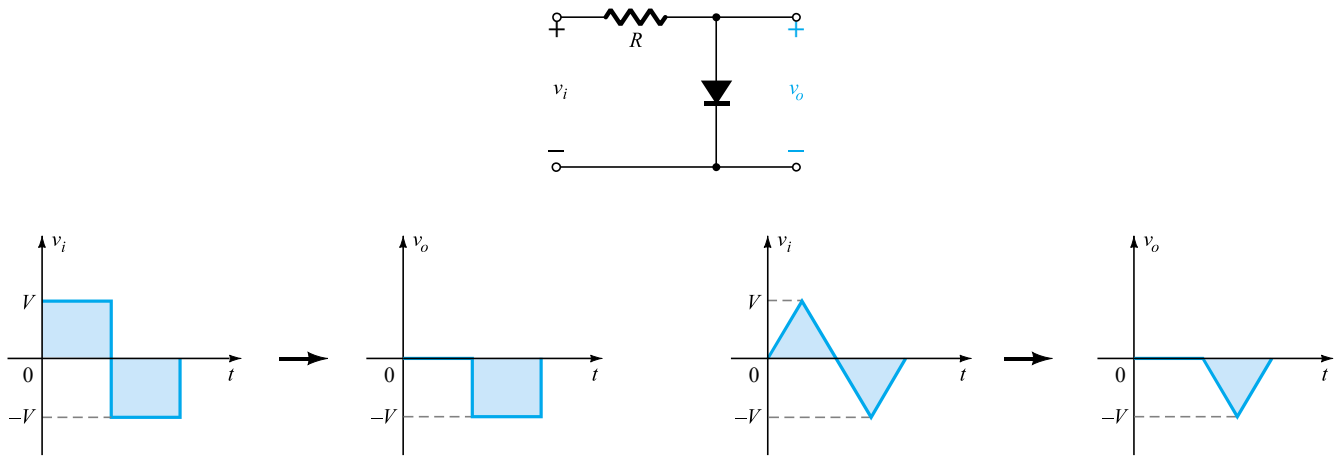


Figure 2.82 Response to a parallel clipper.

EXAMPLE 2.2

Determine v_o for the network of Fig. 2.83.

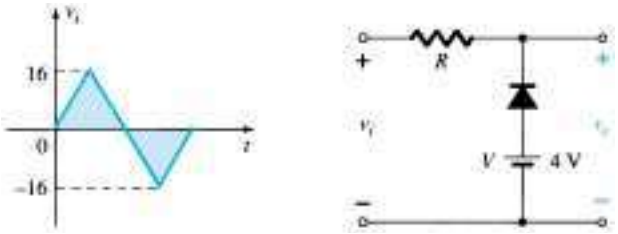


Figure 2.83 Example 2.22.

Solution

The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for the negative region of the input signal. For this region the network will appear as shown in Fig. 2.84, where the defined terminals for v_o require that $v_o = V = 4$ V.

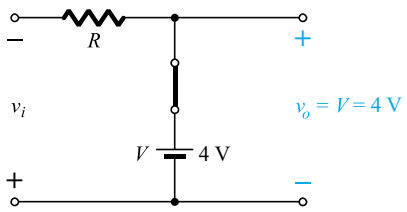


Figure 2.84 v_o for the negative region of v_i.

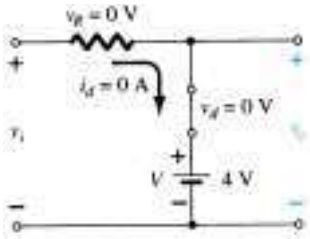


Figure 2.85 Determining the transition level for Example 2.22.

The transition state can be determined from Fig. 2.85, where the condition $i_d = 0$ A at $v_d = 0$ V has been imposed. The result is v_i (transition) $= V = 4$ V.

Since the dc supply is obviously "pressuring" the diode to stay in the short-circuit state, the input voltage must be greater than 4 V for the diode to be in the "off" state. Any input voltage less than 4 V will result in a short-circuited diode.

For the open-circuit state the network will appear as shown in Fig. 2.86, where $v_o = v_i$. Completing the sketch of v_o results in the waveform of Fig. 2.87.

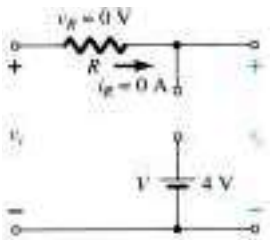


Figure 2.86 Determining v_o for the open state of the diode.

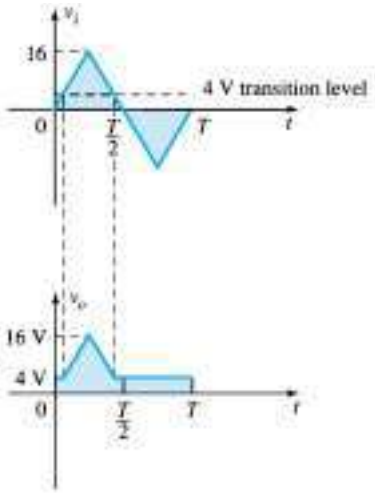


Figure 2.87 Sketching v_o for Example 2.22.

To examine the effects of V_T on the output voltage, the next example will specify a silicon diode rather than an ideal diode equivalent.

Repeat Example 2.22 using a silicon diode with $V_T = 0.7$ V. *EXAMPLE 2.23*

Solution

The transition voltage can first be determined by applying the condition $i_d = 0$ A at $v_d = V_D = 0.7$ V and obtaining the network of Fig. 2.88. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_T - V = 0$$

and

$$v_i = V - V_T = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3 \text{ V}}$$

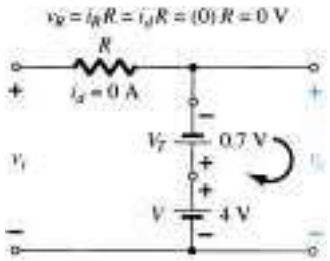


Figure 2.88 Determining the transition level for the network of Fig. 2.83.

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages of less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.89 results, where

$$v_o = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3 \text{ V}}$$

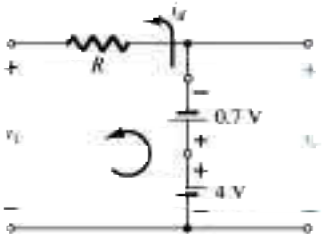


Figure 2.89 Determining v_o for the diode of Fig. 2.83 in the "on" state.

The resulting output waveform appears in Fig. 2.90. Note that the only effect of V_T was to drop the transition level to 3.3 from 4 V.

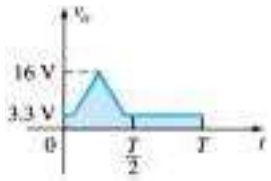


Figure 2.90 Sketching v_o for Example 2.23.

There is no question that including the effects of V_T will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_T, will not be that difficult.

Summary

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.91. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

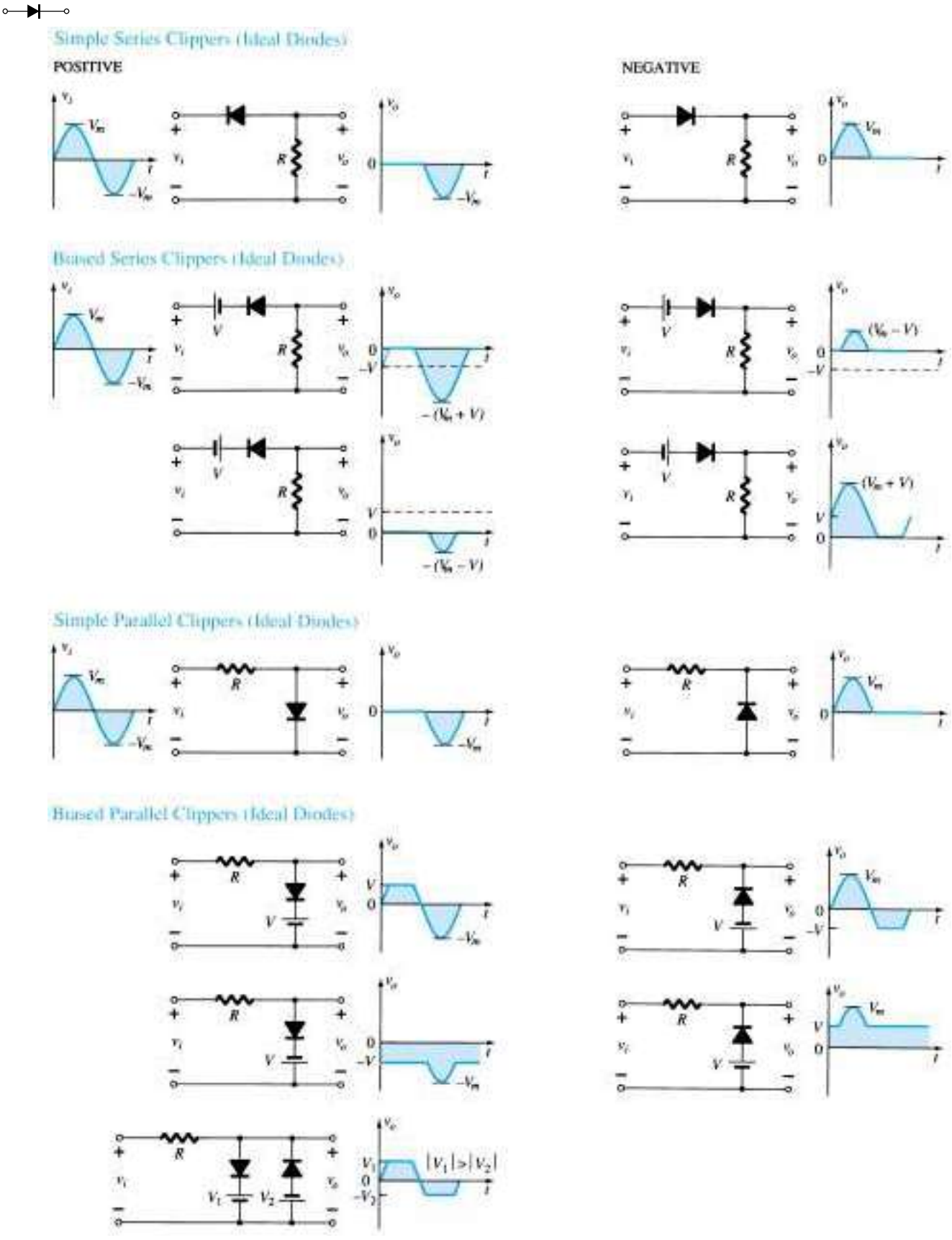


Figure 2.91 Clipping circuits.

2.10 CLAMPERS

The *clamping* network is one that will "clamp" a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants.

The network of Fig. 2.92 will clamp the input signal to the zero level (for ideal diodes). The resistor R can be the load resistor or a parallel combination of the load resistor and a resistor designed to provide the desired level of R.

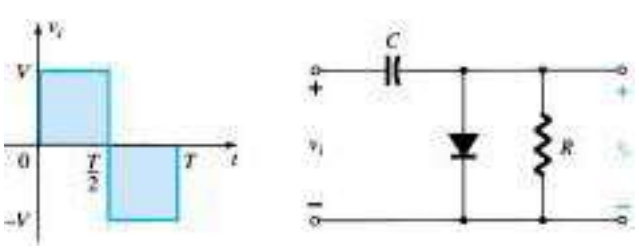


Figure 2.92 Clamper.

During the interval $0 \rightarrow T/2$ the network will appear as shown in Fig. 2.93, with the diode in the "on" state effectively "shorting out" the effect of the resistor R. The resulting RC time constant is so small (R determined by the inherent resistance of the network) that the capacitor will charge to V volts very quickly. During this interval the output voltage is directly across the short circuit and $v_o = 0$ V.

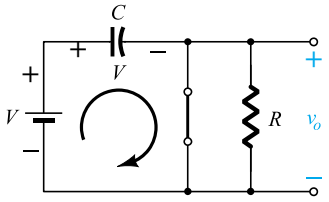


Figure 2.93 Diode "on" and the capacitor charging to V volts.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.94, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

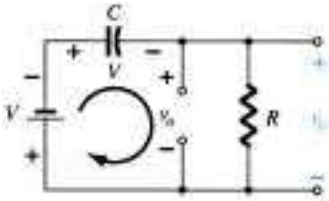


Figure 2.94 Determining v_o with the diode "off."

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.94. Applying Kirchhoff's voltage law around the input loop will result in

$$-V - V - v_o = 0$$

and

$$v_o = -2V$$

The negative sign resulting from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o. The resulting output waveform appears in Fig. 2.95 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

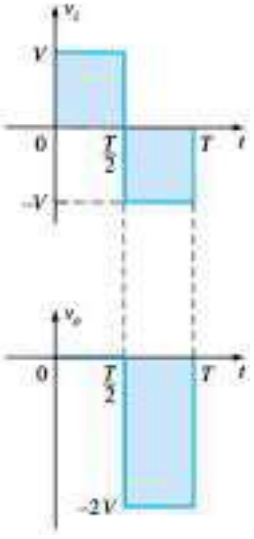


Figure 2.95 Sketching v_o for the network of Fig. 2.92.

For a clamping network:

The total swing of the output is equal to the total swing of the input signal.

This fact is an excellent checking tool for the result obtained.

In general, the following steps may be helpful when analyzing clamping networks:

1. *Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.*

The statement above may require skipping an interval of the input signal (as demonstrated in an example to follow), but the analysis will not be extended by an unnecessary measure of investigation.

2. *During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.*
3. *Assume that during the period when the diode is in the "off" state the capacitor will hold on to its established voltage level.*
4. *Throughout the analysis maintain a continual awareness of the location and reference polarity for v_o to ensure that the proper levels for v_o are obtained.*
5. *Keep in mind the general rule that the total swing of the total output must match the swing of the input signal.*

EXAMPLE 2.24

Determine v_o for the network of Fig. 2.96 for the input indicated.

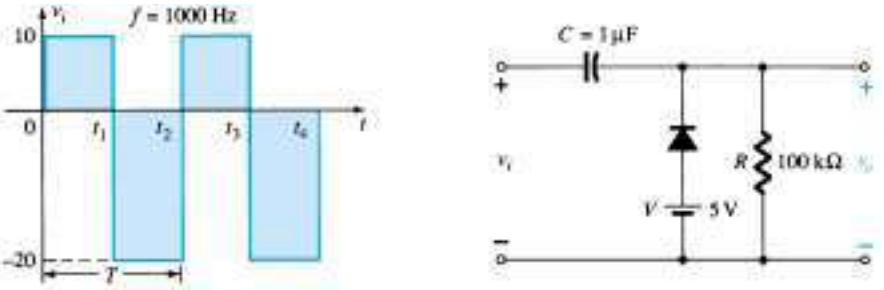


Figure 2.96 Applied signal and network for Example 2.24.

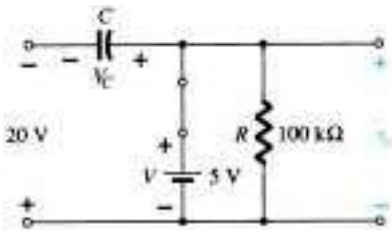


Figure 2.97 Determining v_o and V_C with the diode in the "on" state.

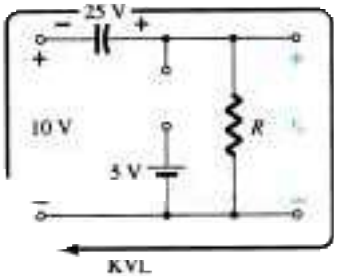


Figure 2.98 Determining v_o with the diode in the "off" state.

Solution

Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state as recommended by comment 1. For this interval the network will appear as shown in Fig. 2.97. The output is across R, but it is also directly across the 5-V battery if you follow the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop will result in

$$-20 \text{ V} + V_C - 5 \text{ V} = 0$$

and

$$V_C = 25 \text{ V}$$

The capacitor will therefore charge up to 25 V, as stated in comment 2. In this case the resistor R is not shorted out by the diode but a Thévenin equivalent circuit of that portion of the network which includes the battery and the resistor will result in $R_{\text{Th}} = 0\ \Omega$ with $E_{\text{Th}} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.98.

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network will result in

$$+10 \text{ V} + 25 \text{ V} - v_o = 0$$

and

$$v_o = 35 \text{ V}$$

The time constant of the discharging network of Fig. 2.98 is determined by the product RC and has the magnitude

$$\tau = RC = (100\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.01\ \text{s} = 10\ \text{ms}$$

The total discharge time is therefore $5\tau = 5(10\ \text{ms}) = 50\ \text{ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.99 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

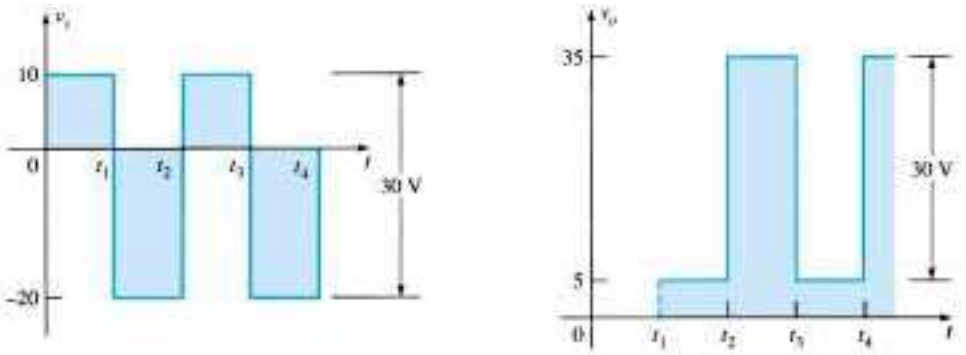


Figure 2.99 v_i and v_o for the clamper of Fig. 2.96.

EXAMPLE 2.25

Repeat Example 2.24 using a silicon diode with $V_T = 0.7$ V.

Solution

For the short-circuit state the network now takes on the appearance of Fig. 2.100 and v_o can be determined by Kirchhoff's voltage law in the output section.

$$+5\ \text{V} - 0.7\ \text{V} - v_o = 0$$

and

$$v_o = 5\ \text{V} - 0.7\ \text{V} = 4.3\ \text{V}$$

For the input section Kirchhoff's voltage law will result in

$$-20\ \text{V} + V_C + 0.7\ \text{V} - 5\ \text{V} = 0$$

and

$$V_C = 25\ \text{V} - 0.7\ \text{V} = 24.3\ \text{V}$$

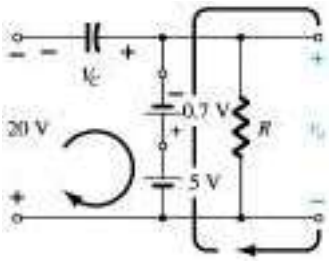


Figure 2.100 Determining v_o and V_C with the diode in the "on" state.

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.101, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\ \text{V} + 24.3\ \text{V} - v_o = 0$$

and

$$v_o = 34.3\ \text{V}$$

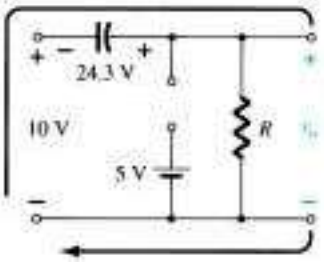


Figure 2.101 Determining v_o with the diode in the open state.

The resulting output appears in Fig. 2.102, verifying the statement that the input and output swings are the same.

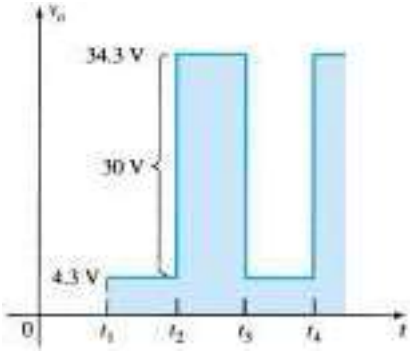


Figure 2.102 Sketching v_o for the clamper of Fig. 2.96 with a silicon diode.

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.103. Although all the waveforms appearing in Fig. 2.103 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.104 for a network appearing in the bottom right of Fig. 2.103.

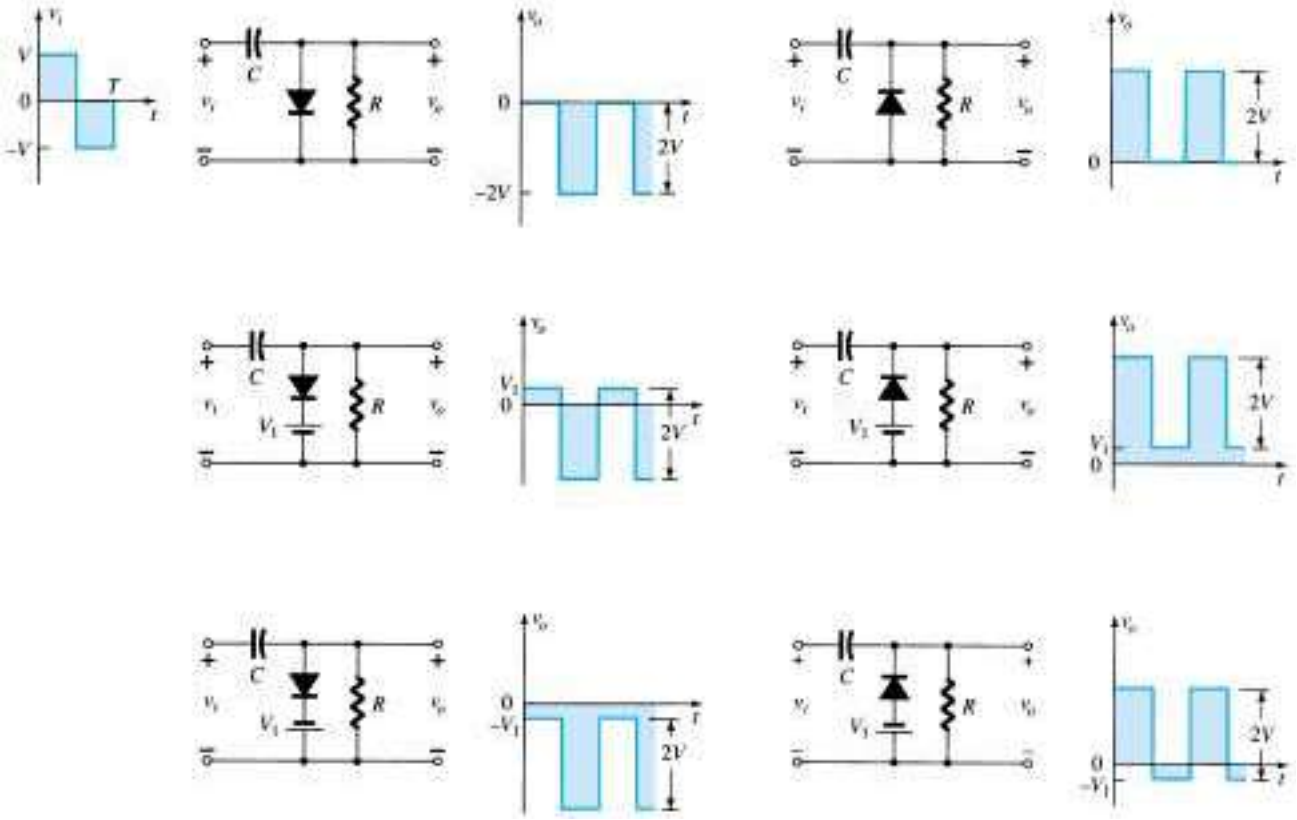


Figure 2.103 Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

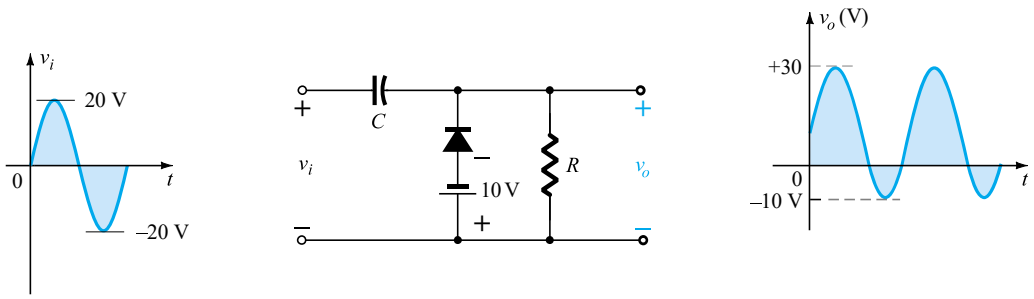


Figure 2.104 Clamping network with a sinusoidal input.

2.11 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to that applied to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Unless otherwise specified, the Zener model to be employed for the "on" state will be as shown in Fig. 2.105a. For the "off" state as defined by a voltage less than V_Z but greater than 0 V with the polarity indicated in Fig. 2.105b, the Zener equivalent is the open circuit that appears in the same figure.

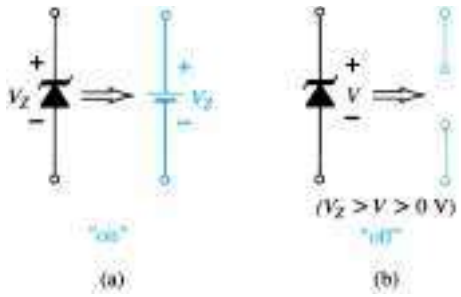


Figure 2.105 Zener diode equivalents for the (a) "on" and (b) "off" states.

V_i and R

The simplest of Zener diode networks appears in Fig. 2.106. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. *Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.*

Applying step 1 to the network of Fig. 2.106 will result in the network of Fig. 2.107, where an application of the voltage divider rule will result in

$$V = V_L = \frac{R_L V_i}{R + R_L} \tag{2.16}$$

If $V \geq V_Z$, the Zener diode is "on" and the equivalent model of Fig. 2.105a can be substituted. If $V < V_Z$, the diode is "off" and the open-circuit equivalence of Fig. 2.105b is substituted.

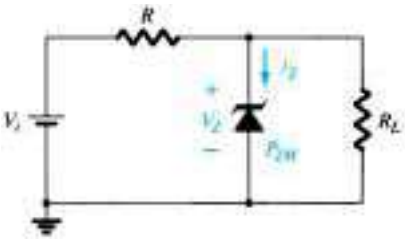


Figure 2.106 Basic Zener regulator.

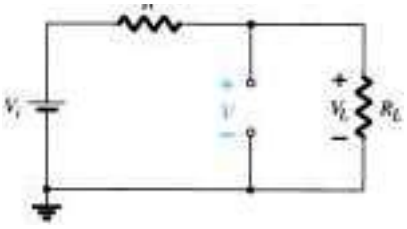


Figure 2.107 Determining the state of the Zener diode.

UNIT-III BIPOLAR JUNCTION TRANSISTORS

A transistor is a three-layer semiconductor device consisting of either two n- and one p-type layers of material or two p- and n-type layers of material.

—The former is called an npn transistor, and the latter is called an pnp transistor. Both are shown in Fig. 1a. The representations employed when transistors are used as circuit elements as shown in Fig. 1b.

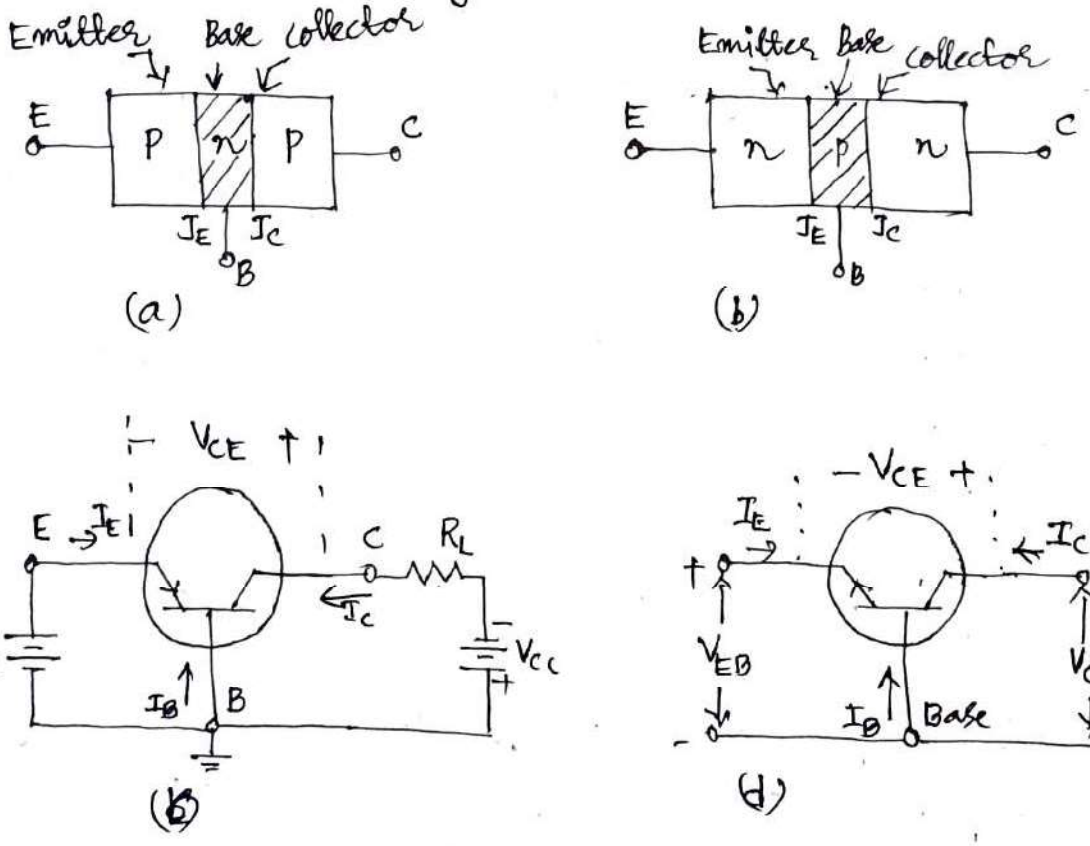


Fig. 1 (a) A p-n-p and a n-p-n- transistor. The emitter junction or collector junction is J_E or J_C.
(b) Circuit representation of the two transistor types.

Emitter: The purpose of emitter is to emit the charged particles. It is heavily doped (to emit large number of charge particles) and moderate in size.

Base: To control the current passing through the transistor. It is lightly doped (to reduce the recombination in the base region) and small in size.

Collector:

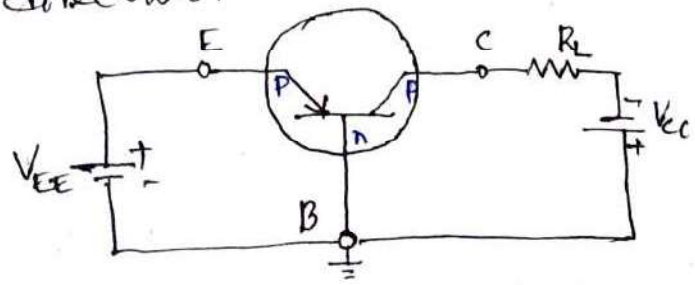
To collect the charged particles which are emitted by the emitter, moderately doped and large in size (to withstand the further raise in temperature).

→ The main purpose of transistor is to do faithful amplification.

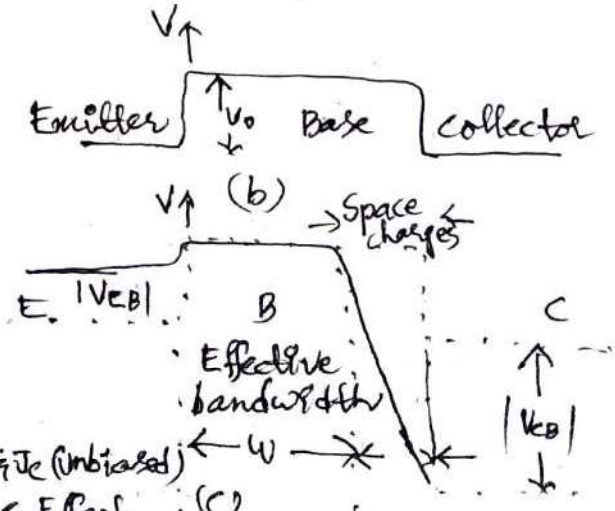
To do some operations, the transistor must be properly biased as,

S.No	Junctions	Region of operations	Applications
1.	$J_E \rightarrow R.B$ $J_C \rightarrow R.B$	cut-off	OFF-Switch
2.	$J_E \rightarrow F.B$ $J_C \rightarrow R.B$	Active	Amplification
3.	$J_E \rightarrow F.B$ $J_C \rightarrow F.F$	Saturation	ON-Switch
4.	$J_E \rightarrow R.B$ $J_C \rightarrow F.B$	Inverse-active	Attenuator.

→ If external potentials are applied for an active region by considering Fig. 2. Here a p-n-p transistor is shown with voltage sources which serve to bias the J_E (E-B junction) in the forward direction and the collector-base junction, J_C, is in the reverse direction.



(a)



(c)

Fig. 2; (a) A p-n-p transistor
(b) The potential barriers at the J_E & J_C (unbiased)
(c) V variation $|V_{CB}|$ is increased. i.e Effect B/W.

CURRENT COMPONENTS AND THEIR RELATIONSHIPS

In figure (1), we show the various current components which flow across the forward-biased emitter junction and the reverse-biased collector junction.

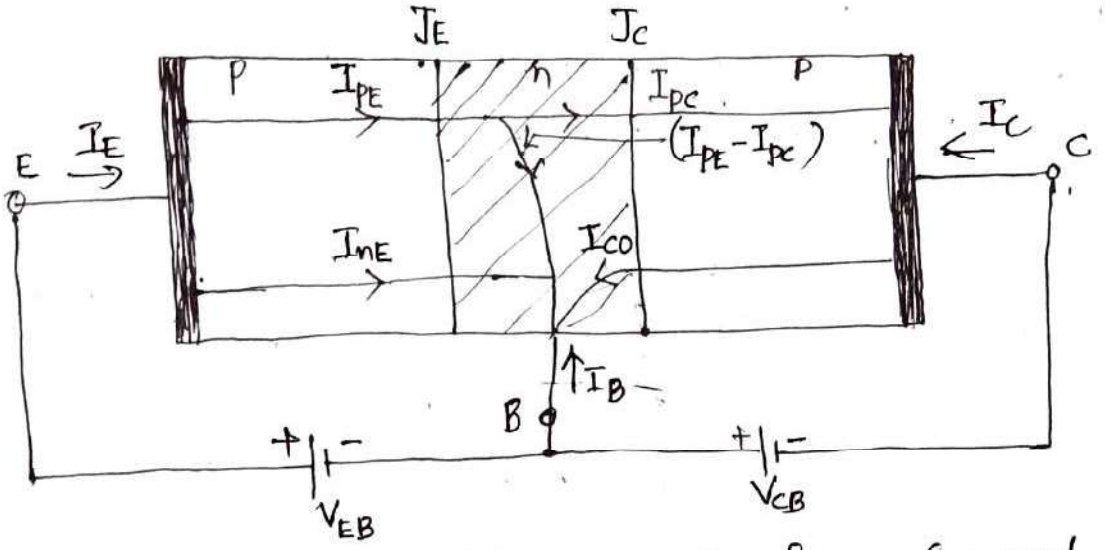


Fig. 1: Transistor current components for a forward-biased emitter junction and a reverse-biased collector junction.

The emitter current I_E consists of hole current I_{PE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into the emitter).

→ Note all the holes crossing the emitter junction J_E reach the collector junction J_C because some of them combine with the electrons in the n-type base.

– If I_{PC} is the hole current at J_C, there must be a bulk recombination current $I_{PE} - I_{PC}$ leaving the base, as indicated in Fig. 1. (actually, electrons enter the base region through the base lead to supply those charges which have been lost by recombination with the holes injected into the base across J_E).

→ If the emitter were open-circuited so that $I_E = 0$, then I_{PC} would be zero. Under these circumstances, the base and would act as a reverse-biased diode, and the collector current I_C would equal the reverse saturation current I_{CO}, i.e $\boxed{I_C = I_{CO}}$ — (1)

– If $I_E \neq 0$, we note that $I_C = I_{CO} - I_{PC}$ — (2) $\left[\because I_C + I_{PC} = I_{CO},\ I_C = I_{CO} - I_{PC}\right]$

For a p-n-p transistor, I_{CO} consists of holes moving from left to right (base to collector) and electrons crossing from right to left, then I_{CO} is negative for p-n-p transistor. For n-p-n I_{CO} is positive.

We define various parameters which relate the current components discussed above:

Emitter efficiency, γ:

The emitter, or injection, efficiency γ is defined as

$$\gamma \equiv \frac{\text{current of injected carriers}}{\text{total emitter current}}$$

In case of a p-n-p transistor, $\gamma = \frac{I_{pE}}{I_{pE}+I_{nE}} = \frac{I_{pE}}{I_E}$ — (3)

where I_{pE} is the injected hole diffusion current at emitter junction and I_{nE} is the injected electron diffusion current at emitter junction.

Transport factor, β:

The transport factor, β, is defined as

$$\beta = \frac{\text{injected carrier current reaching } J_C}{\text{injected carrier current } J_E}$$

In the case of a p-n-p transistor, we have

$$\beta = \frac{I_{pC}}{I_{pE}} \quad -(4a) \qquad \text{or} \qquad \beta = \frac{I_C}{I_B} \quad -(4b)$$

$$\left[\because I_B = I_{pE} - I_{pC} \simeq I_{pE}\right]$$

Large-signal current gain, α:

The ratio of the negative of the collector current increment to the emitter current change from zero (cut-off) to I_E as the large-signal current gain of a common-base configuration; or

$$\alpha \equiv -\frac{\Delta I_C}{(I_E - 0)} = \frac{I_{pC}}{I_E} = \left(\frac{I_{pC}}{I_{pE}}\right)\left(\frac{I_{pE}}{I_E}\right) = \beta\cdot\gamma = \gamma\cdot\beta$$

$$\boxed{\alpha = \gamma\cdot\beta} \quad -(5a) \qquad \text{or} \qquad \boxed{\alpha = \frac{I_C}{I_E}} \quad -(5b)$$

From the discussion of transistor currents we see that if the transistor is in its active region, the collector current is given by

$$I_C = -\alpha I_E + I_{CO} \quad \left[\because \alpha = -\frac{(I_C - I_{CO})}{I_E}\right.$$

$$-\alpha I_E = I_C - I_{CO}$$

$$I_C = -\alpha I_E + I_{CO}. \quad \text{— (8)}$$

— In the active region the collector current is essentially independent of collector voltage and depends only upon the emitter current.

— Suppose now consider equation (8) generalized way so that it may apply for any voltage across I_C, so replace I_{CO} by a current in a p-n diode then the complete expression for I_C for any V_C and I_E is

$$I_C = -\alpha I_E + I_{CO}(1 - e^{V_C/V_T}) \quad \text{— (9)}.$$

The equation (9) is generalised expression for collector current I_C for collector junction voltage V_C and emitter current I_E.

Relation among I_C, I_B, and I_{CO} : (Relation between α and β)

From $I_C = -\alpha I_E + I_{CO}$, — from Fig (1), since I_C and I_E are flowing in opposite directions, $I_E = -(I_C + I_B)$ — (10), then equation (9) is written as,

$$I_C = -\alpha\left[-(I_C + I_B)\right] + I_{CO}$$

$$I_C = \alpha(I_C + I_B) + I_{CO} = \alpha I_C + \alpha I_B + I_{CO}$$

$$I_E - \alpha I_C = \alpha I_B + I_{CO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CO} \Rightarrow \boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CO}}{1-\alpha}} \quad \text{— (11)}$$

When I_{CO} is neglected, $I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B$ — (12)

$$\Rightarrow \frac{I_C}{I_B} = \beta = \frac{\alpha}{1-\alpha} \quad — (13)$$

Substitute equation (13) in (11), we get $I_C = \beta I_B$ — (14)

$$I_E = I_C + I_B = \beta I_B + I_B = (1+\beta) I_B \quad — (15)$$

$$I_C = \alpha I_E \quad [\because \text{for } n\text{-}p\text{-}n]$$

$$= \frac{\beta}{1+\beta} I_E \quad — (16)$$

$[\because \beta = \frac{\alpha}{1-\alpha}$
$\beta(1-\alpha) = \alpha$
$\beta - \beta\alpha = \alpha$
$\beta = \alpha + \beta\alpha$
$\beta = (1+\beta)\alpha$
$\frac{\beta}{1+\beta} = \alpha]$

i.e

$$I_C = \beta I_B$$

$$I_E = (1+\beta) I_B$$

$$I_C = \alpha I_E$$

$$I_C = \frac{\beta}{1+\beta} I_E$$

→ All the above relations between the currents are valid only for the active region of operation.

→ The one and only equation valid for all region of operation is $I_E = I_C + I_B$ or $I_E = -(I_C + I_B)$.

TRANSISTOR STRUCTURE

Five basic techniques have been developed for the manufacture of diodes, transistors, and other semiconductor devices.

Consequently, such devices may be classified into one of the following types:

- Grown
- Alloy electro-chemical
- Diffusion or epitaxial or Planar

a) Grown:

The n-p-n grown-junction transistor is illustrated in Fig. 1a. It is made by drawing a single crystal from a melt of silicon or germanium whose impurity concentration is changed during the crystal-drawing operation by adding n- or p-type atoms as required.

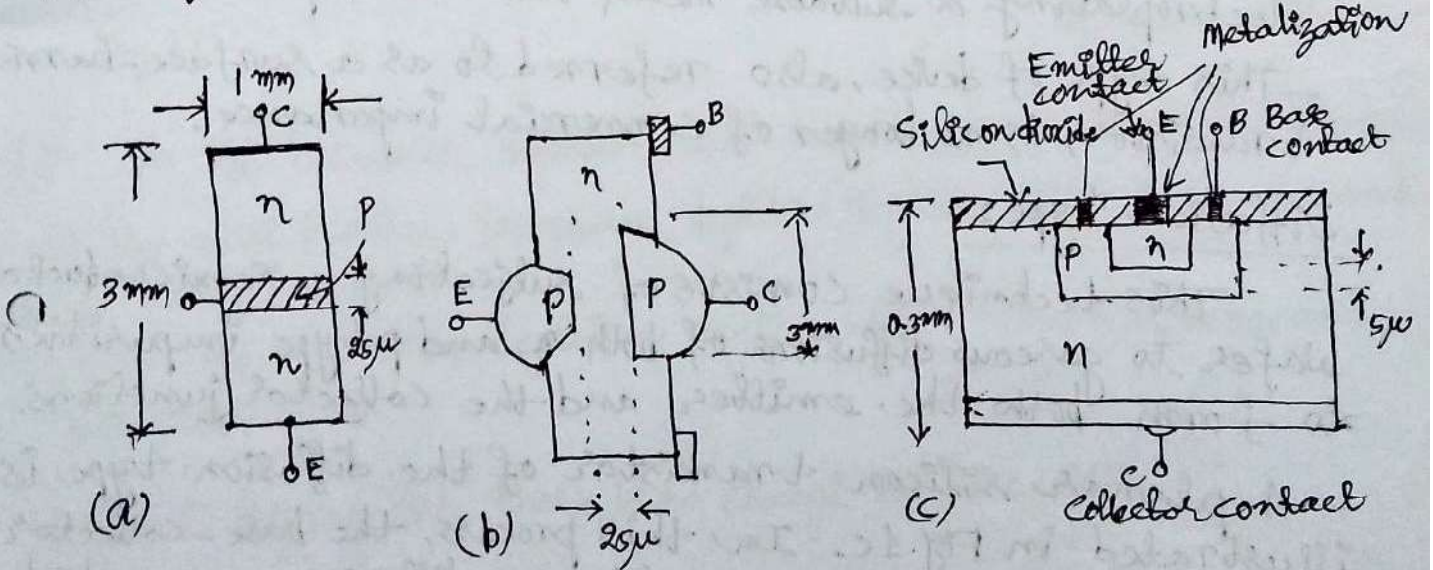


Fig. 1: Construction of transistors (a) Grown, (b) Alloy, and (c) diffused, or epitaxial, planar types

(b) Alloy type:

This technique, also called the fused construction, is illustrated in Fig. 1b for a p-n-p transistor.

—The center (base) section is a thin wafer of n-type material. Two small dots of indium are attached to the opposite of the wafer, and the whole structure is raised for a short time to a high tempera- —take

above the melting point of indium but below that of germanium.
- The indium dissolves the germanium beneath it and forms a saturation solution.
- On cooling, the germanium in contact with the base material recrystallizes with enough indium concentration to change it from n-type to p-type.
- The collector is made larger than the emitter, so that the collector subtends a large angle as viewed from the emitter.
- Because of the geometrical arrangement, very little emitter current follows a diffusion path which carries it to the base rather than to the collector.

Electrochemically etched Type:

This technique consists in etching depressions on opposite sides of a semiconductor wafer in order to reduce the thickness of the base section.
- The emitter and collector junctions are then formed by electroplating a suitable metal into the depression areas.
- This type of device, also referred to as a surface-barrier transistor, is no longer of commercial importance.

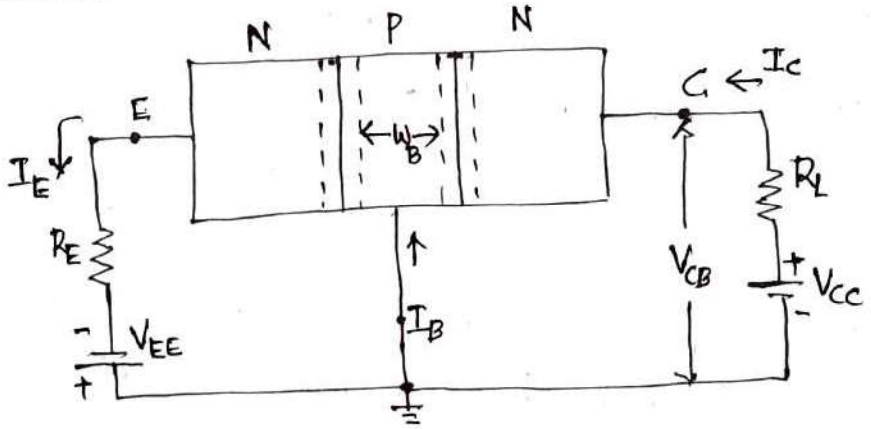
Diffusion type:

This technique consists of subjecting a semiconductor wafer to gaseous diffusions of both n- and p-type impurities to form both the emitter and the collector junctions.
- A planar silicon transistor of the diffusion type is illustrated in Fig. 1c. In this process, the base-collector junction area is determined by a diffusion mask which is photo etched just prior to the base diffusion. The emitter is then diffused on the base, and a final layer of silicon dioxide is thermally grown over the entire surface.
- Because of the passivating action of this layer, most surface problems are avoided and very low leakage current result.
- There is also an improvement in the current gain at low currents and in the noise figure.

Epitaxial type:

The epitaxial technique consists in growing a very thin, high purity, single crystal layer of Silicon or germanium on a heavily doped substrate of the same material.
- This augmented crystal forms the collector on which the base and emitter may be diffused.

BASE WIDTH MODULATION (OR) EARLY EFFECT:



W_B → Base width

Fig-1:

(i) As V_{BE} increases, depletion width decreases, and base width increases. As V_{BE} still further increases, deption region width decreases and base width increases.

→ when $V_{BE} = V_\gamma$, then depletion region width reduced to zero, an base width → W_B'.

As V_{BE} ↑ (beyond V_γ), there is no change in base width.

(ii) As V_{CB} increases, depletion region width across J_C increases and base width decreases and then temparature across junction J_C increases, which leads to decrement in the rate of recombination in base region, there by number of charged particles collected by collector increases.

→ The base width modulation is always related to the reverse bias voltage across the collector junction i.e., the variation of the base width w.r.t applied voltage across the collector junction is called Base width modulation.

Consequences of base width modulation:

(i) As V_{CB} increases:

Depletion region width across J_c increases, base width decrea rate of recombination in base decreases and collector curr increases.

As $V_{CB} \uparrow\uparrow$, $I_C \uparrow\uparrow$, the value of I_C depends on V_{CB}.

$$I_C = f[V_{CB}] \quad -(1)$$

BJT is a current controlled device, $I_C = f[I_E]$ -(2)

Therefore, $I_C = f[I_E, V_{CB}]$ -(3)

- In general, output current = f [input current, outp Volta -(4)

(ii) As $V_{CB} \uparrow$, depletion region width $\uparrow$, temp across $J_C \uparrow$, brea of covalent bonds in base and collector increases $\uparrow$, electro hole pair generation $\uparrow$.

$$I_{no} \uparrow, I_{po} \uparrow \Rightarrow I_o \uparrow$$

$$I_{PE} \uparrow \Rightarrow I_E \uparrow \quad \text{as } I_{PE} \text{ is independent.}$$

- By comparing V_{BE} and V_{CB},

$$V_{BE} = f[V_{CB}] \quad -(5)$$

By comparing V_{BE} and I_E,

$$V_{BE} = f[I_E] \quad -(6)$$

$$\therefore V_{BE} = f[I_E, V_{CB}] \quad -(7)$$

In general, input Voltage = f [input current, outpu Voltage] -(

BIASING METHODS

The biasing methods are

(i) Fixed bias method (or) Base resistance

(ii) Collector-to-base bias or Feedback resistor bias method

(iii) Voltage divider bias (or) self-bias (or) Emitter bias

FIXED BIAS (or) BASE RESISTANCE:

By applying KVL to input loop,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B R_B$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad -(1)$$

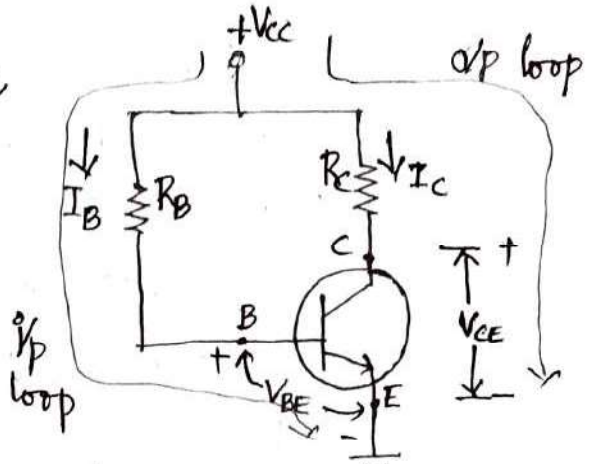


Fig. 1: Fixed bias circuit

By applying KVL to output loop,

$$V_{CC} - I_R R_C - V_{CE} = 0$$

$$V_{CC} - V_{CE} = I_R R_C \Rightarrow \boxed{V_{CE} = V_{CC} - I_C \cdot R_C} \quad -(2)$$

Assume that the transistor operated in active region,

$$\boxed{I_C = \beta I_B} \quad -(3)$$

~~Saturation~~ Stability factor, S:

To calculate S, take input loop equation, $V_{CC} - I_B R_B - V_{CE} = 0$

Differentiate w.r.t I_C, we get, $0 - \frac{dI_B}{dI_C} \cdot R_B - 0 = 0$

$$\therefore \frac{dI_B}{dI_C} = 0$$

$$\text{stability factor, } S = \frac{1+\beta}{1-\beta \cdot \frac{dI_B}{dI_C}} = \frac{1+\beta}{1-\beta \cdot 0} = 1+\beta \quad -(4)$$

→ As β is high, S is high, so the fixed bias circuit is thermally less stable.

To increase the thermal stability of the circuit, connect a resistor at emitter terminal as shown in Fig②.

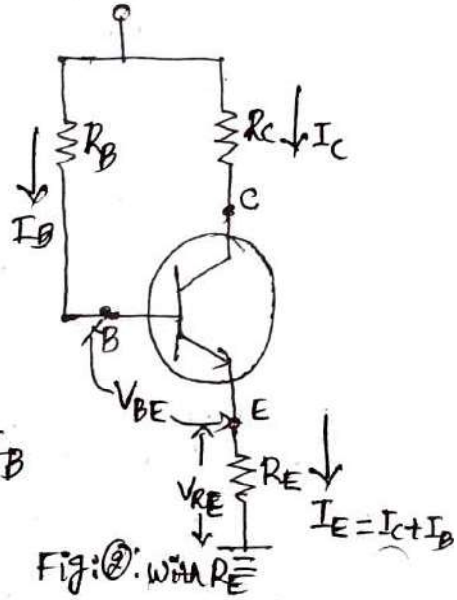


Fig:②. with R_E

Apply KVL to i/p loop,

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0 \quad -(5)$$

→ Assume transistor operated in active region,

$$I_C = \beta I_B$$

$$I_C + I_B = \beta I_B + I_B = (\beta + 1) I_B = (1+\beta) I_B$$

equation (5) becomes,

$$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$V_{CC} - V_{BE} = I_B [R_B + (1+\beta) R_E]$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E} \quad -(6)$$

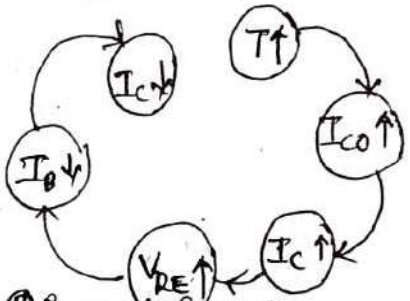


Fig:③: stabilization

Stability factor, S:

From equation (5), $V_{CC} - V_{BE} - I_B (R_B + R_E) - I_C \cdot R_E = 0$

Differentiate above equation w.r.t I_C, we get,

$$0 - 0 - \frac{dI_B}{dI_C}(R_B + R_E) - R_E \cdot \frac{dI_C}{dI_C} = 0$$

$$-\frac{dI_B}{dI_C}(R_B + R_E) = R_E$$

$$\Rightarrow \frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E} \quad -(7)$$

then $$S = \frac{1+\beta}{1 - \beta \cdot \frac{dI_B}{dI_C}} = \frac{1+\beta}{1 - \beta\left(\frac{-R_E}{R_B+R_E}\right)} = \frac{1+\beta}{1 + \beta\left(\frac{R_E}{R_B+R_E}\right)}$$

$$S = \frac{(1+\beta)(R_B + R_E)}{R_B + R_E + \beta R_E} \Rightarrow \boxed{S = \frac{(1+\beta)(R_B+R_E)}{R_B + (1+\beta) R_E}} \quad -(8)$$

As denominator > 1, $S < 1+\beta$, the circuit is more stable (9)

i.e., fixed bias circuit with R_E is thermally more stable compared to fixed bias circuit without R_E.

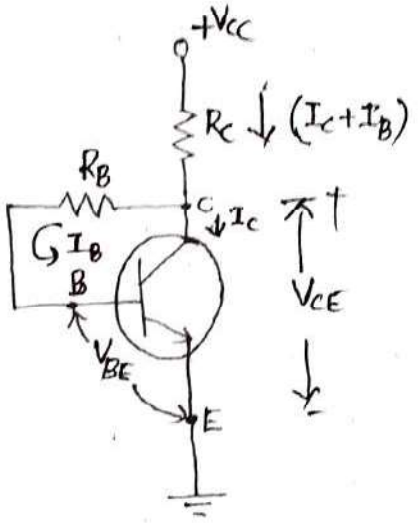
COLLECTOR - BASE (OR) FEEDBACK RESISTOR METHOD

By applying KVL to the input loop,

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_C R_C - I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_C R_C - (R_C + R_B) I_B - V_{BE} = 0 \quad -(1)$$



→ Assuming the transistor operating in active region, $I_C = \beta I_B$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \quad -(2)$$

- From equation (2), $V_{CC} - \beta \cdot I_B \cdot R_C - I_B R_C - I_B R_B - V_{BE} = 0$

$$V_{CC} - (1+\beta) I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = (1+\beta) I_B R_C + I_B R_B = [R_B + (1+\beta) R_C] I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C} \quad -(3)$$

Apply KVL to output loop

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C \quad -(4)$$

- Stability factor, S:

From equation (1), $V_{CC} - I_C R_C - (R_C + R_B) I_B - V_{BE} = 0$, apply differentiation w.r.t I_C, we get

$$0 - R_C \cdot \frac{dI_C}{dI_C} - (R_C + R_B) \frac{dI_B}{dI_C} - 0 = 0$$

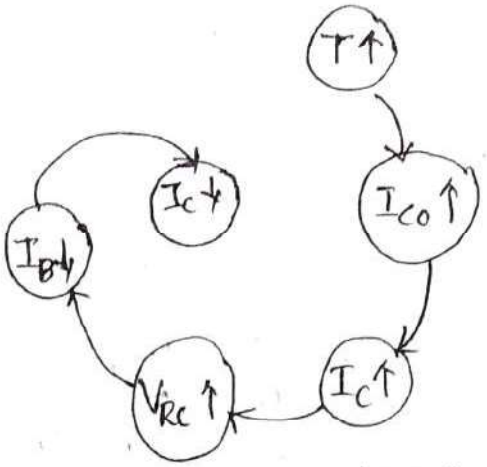
$$-R_C - (R_C + R_B) \frac{dI_B}{dI_C} = 0 \Rightarrow \frac{dI_B}{dI_C} = \frac{-R_C}{R_C + R_B} \quad -(5)$$

Substituting equation (5) in $S = \frac{1+\beta}{1 - \beta \frac{dI_B}{dI_C}}$

$$= \frac{\beta + 1}{1 - \beta \left(\frac{-R_C}{R_C + R_B}\right)} = \frac{\beta + 1}{1 + \beta \left(\frac{R_C}{R_C + R_B}\right)}$$

As denominator > 1, $S < (1+\beta)$.

→ The collector to base bias circuit more stable compared to Fixed bias circuit (for without R_E circuit).



$$V_{CC} - V_{RC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE} - V_{RC}}{R_B}$$

The resistor in which $(I_C + I_B)$ current flows, that transistor provides stability to the transistor.

→ If R_C is very low $(R_C \to 0)$, $S = \frac{1+\beta}{1+\beta} = 1+\beta$, then the circuit becomes less stable so that for collector to base bias circuit, R_C should not be very low.

VOLTAGE DIVIDER (OR) SELF BIAS (OR) EMITTER BIAS

→ The stability of circuit is independent of current passing through R_C, so it is called Self-bias circuit.

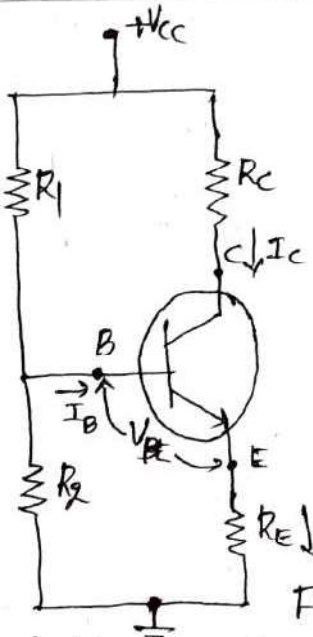


Fig.1: Self-bias.

By applying Thevenins theorem at the input of the transistor,

$$V_{Th} = V_{CC}\left(\frac{R_2}{R_1+R_2}\right) \quad -①$$

$$R_{Th} = R_1 \| R_2 = \frac{R_1 \cdot R_2}{R_1+R_2} \quad -②$$

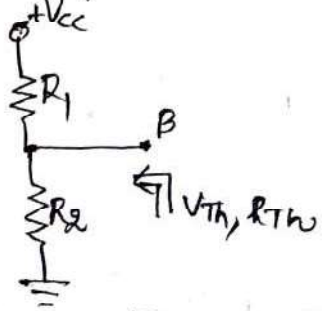
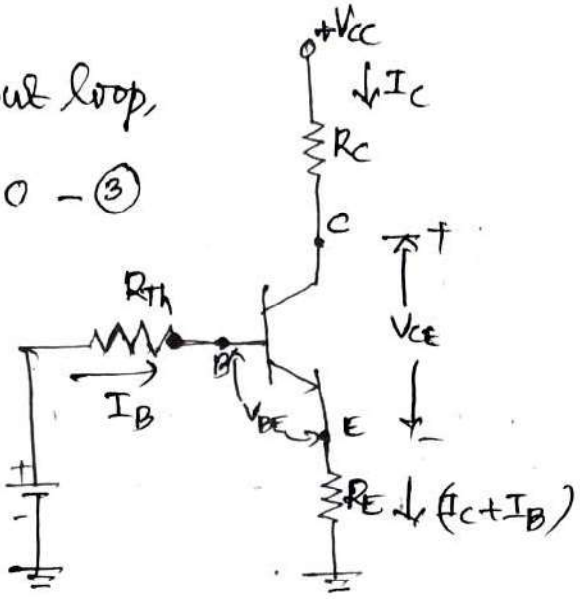


Fig.2: Equivalent circuit for i/p ckt

The equivalent circuit is given for fig.(1) as,



By applying KVL to the input loop,

$$V_{Th} - I_B R_{Th} - V_{BE} - (I_C + I_B)R_E = 0 \quad -(3)$$

→ Assume the transistor is operating in active region,

$$V_{Th} - I_B R_{Th} - V_{BE} - (\beta I_B + I_B)R_E = 0$$

$$V_{Th} - I_B \cdot R_{Th} - V_{BE} - (1+\beta) I_B R_E = 0 \quad -(4)$$

$$V_{Th} - V_{BE} = I_B R_{Th} - (1+\beta) \cdot R_E I_B$$

$$I_B \left[R_{Th} - (1+\beta) R_E \right] = V_{Th} - V_{BE}$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_E} \quad -(5)' \qquad I_C = \beta I_B \quad -(6)$$

Apply KVL to o/p loop,

$$V_{CC} - I_C R_C - V_{CE} - (I_C + I_B) R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - (I_C + I_B) R_E \quad -(7)$$

Stability factor, S:

$$S = \frac{1+\beta}{1 - \beta \cdot \frac{dI_B}{dI_C}}$$

Differentiate equation (5), w.r.t to I_C, we get

$$0 - R_{Th} \frac{dI_B}{dI_C} - 0 - R_E \cdot \frac{dI_C}{dI_C} - R_E \frac{dI_B}{dI_C} = 0$$

$$\Rightarrow \frac{dI_B}{dI_C} (R_{Th} + R_E) = -R_E \implies \frac{dI_B}{dI_C} = \frac{-R_E}{R_{Th} + R_E}$$

$$\text{then } S = \frac{1+\beta}{1 - \beta\left(\frac{-R_E}{R_{Th}+R_E}\right)} = \frac{1+\beta}{1 + \beta\left(\frac{R_E}{R_{Th}+R_E}\right)} \quad -(8)$$

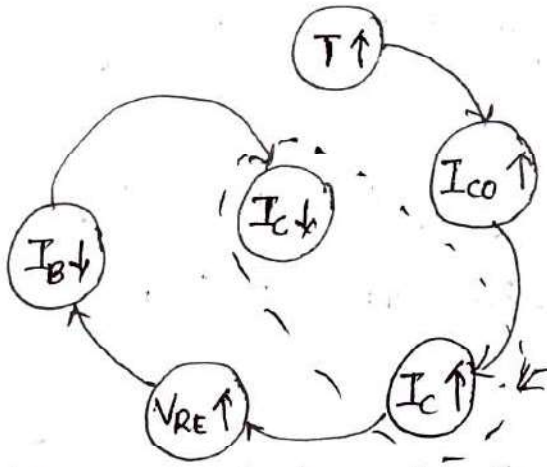


Fig.① Flow chart for self-bias

← stabilized.

→ Stability factor for biasing methods order is

{Self bias} > {collector to base bias} > {fixed bias}

VERIFICATION:

(i) If the calculated voltage V_{CE} satisfies the condition

$V_{CE(Sat)} < V_{CE} < V_{CC}$, → Transistor is in active.

If $V_{CE} = V_{CC}$ & $I_C = 0$, the transistor is operating in cut-off region as

else the transistor is in saturation region.

$V_{CE(Sat)} = 0.1V \longrightarrow Ge$

$= 0.2V \longrightarrow Si$

(ii) Junction J_E is forward biased,

If $V_C < V_B$ (NPN) $\Rightarrow$ $J_C \rightarrow F.B \Rightarrow$ Saturation region

$V_C > V_B$ (NPN) $\Rightarrow$ $J_C \rightarrow R.B \Rightarrow$ Active region

(iii) If the transistor in saturation region it satisfies the condition the base current $\boxed{I_B \geq \frac{I_C}{\beta_{min}}}$

else it is in active region.

(P1) In the transistor amplifier shown in Fig. 1(a), $R_c = 8K\Omega$, $R_L = 24K\Omega$, and $V_{cc} = 24V$. Draw the dc load line and determine the optimum operating point. Also draw the ac load line.

Solu: **DC load line;**

From Fig. (P1), we have

$$V_{cc} - I_c R_c - V_{CE} = 0$$

$$\Rightarrow V_{cc} = V_{CE} + I_c R_c \quad [\because \text{'no current through } R_L]$$

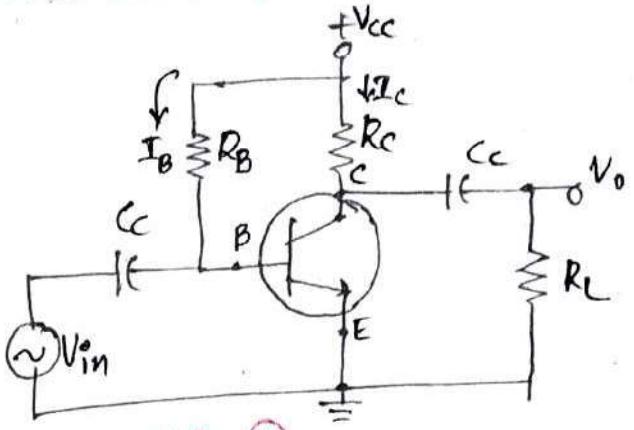


Fig. (P1a)

→ For drawing dc load line, the two end points, namely, maximum V_{CE} point (at $I_c = 0$) and maximum I_c point (at $V_{CE} = 0$) are required.

$$\text{Max. } V_{CE} = V_{cc} = 24V.$$

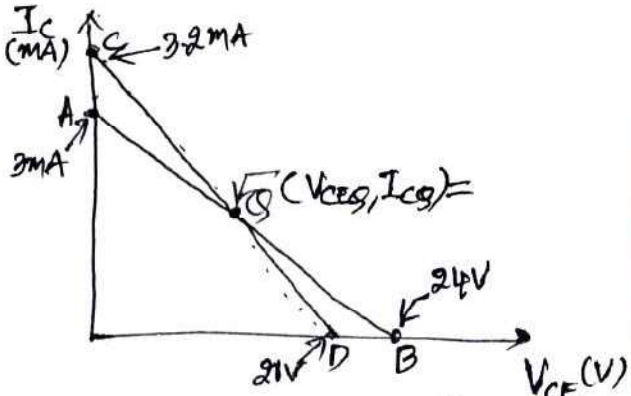
$$\text{Max. } I_c = \frac{V_{cc}}{R_c} = \frac{24V}{8K\Omega} = 3mA.$$

Therefore, the dc load line AB is drawn with the point B ($OB = 24V$) on the V_{CE} axis and the point A ($OA = 3mA$) on the I_c axis, as shown in Fig. (P1b)

(ii) For fixing optimum operating point Q, mark the middle of the AB load line with (V_{CEQ}, I_{CQ}).

i.e $$V_{CEQ} = \frac{V_{cc}}{2} = \frac{24V}{2} = 12V.$$

$$I_{CQ} = \frac{I_{c\,max}}{2} = \frac{3mA}{2} = 1.5mA$$



(iii) **AC load line;**

To draw an ac load line, two end points namely, Max. V_{CE} and maximum I_c when the signal is applied are required.

The ac load, $R_{ac} = R_c \| R_L = 8K\Omega \| 24K\Omega = \frac{8 \times 24}{8+24}$

$$\boxed{R_{ac} = 6K\Omega}$$

$$\text{Max. } V_{CE} = V_{CEQ} + I_{CQ} \cdot R_{ac} = 12 + (1.5m \times 6K) = 12 + 9 = 21V \quad \text{(point D value)}$$

$$\text{Max. } I_c = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 1.5mA + \left(\frac{12V}{6K\Omega}\right) = 1.5mA + 2mA = 3.2mA \quad \text{(point C value)}$$

(P2) In the fixed bias method (refer Fig. P2), a Silicon transistor with $\beta = 100$ is used. $V_{CC} = 6V$, $R_C = 3k\Omega$, $R_B = 530k\Omega$. Draw the dc load line and determine the operating point. What is the stability factor?

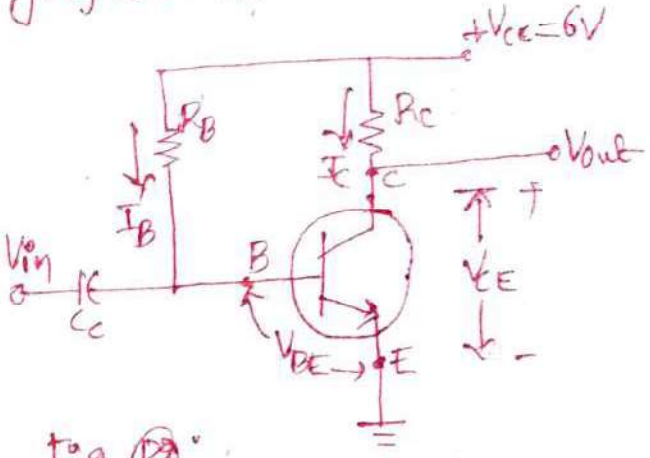


Fig. (P2):

Solu: (i) DC load line:

$V_{CE} = V_{CC} - I_C R_C$

when $I_C = 0$, $V_{CE} = V_{CC} = 6V$

when $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C} = \frac{6V}{3k\Omega} = 2mA$

(ii) Operating point Q:

For Silicon transistor, $V_{BE} = 0.7V$,

$V_{CC} = I_B R_B + V_{BE} \Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{(6-0.7)V}{530k\Omega} = 10\mu A$

Therefore, $I_C = \beta I_B = 100 \times 10\mu A = 1mA$.

$V_{CE} = V_{CC} - I_C R_C = 6V - (1mA \times 3k\Omega) = 6V - 3V = 3V$.

Therefore operating point is $V_{CEQ} = 3V$ and $I_{CQ} = 1mA$

(iii) Stability factor, S:

$S = 1 + \beta = 1 + 100 = 101$.

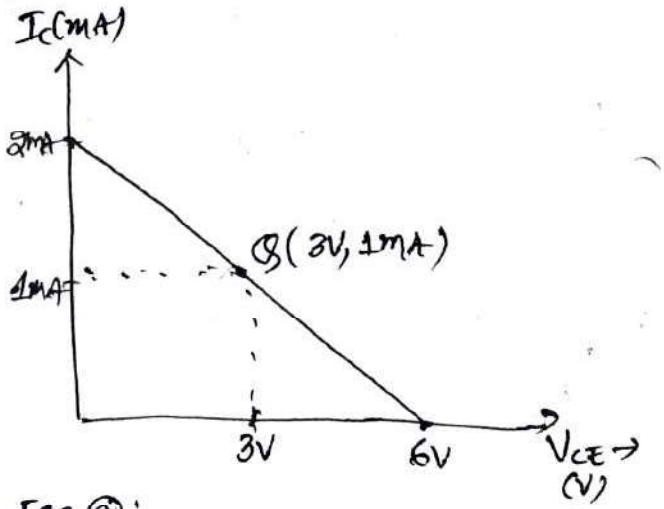


Fig. (2):

STABILIZATION AGAINST VARIATIONS IN V_{BE} and β

The variation of V_{BE} with temparature has a very important effect on bias stability. For a silicon transistor V_{BE} is about 0.6V at room temparature, and for a germanium transistor, it is about 0.2V.

— As the temparature increases, $|V_{BE}|$ decreases at the rate of 2.5mV/°c for both germanium and silicon transistors.

— The stability factor S':

The variation of I_C with V_{BE} is given by the stability factor S', denoted by

$$S' \equiv \frac{\partial I_C}{\partial V_{BE}} = \frac{dI_C}{dV_{BE}} \quad -(1)$$

where both I_{CO} and β are considered constant.

→ The variation of β with temparature:

As temparature increases then β increases, for 50°c rise in temparature, β value of Germanium transistor doubles and for 100°c rise in temparature, β value of silicon transistor doubles.

— The variation of I_C with respect to β is given by the stability factor, S'', defined by

$$S'' \equiv \frac{\partial I_C}{\partial \beta} = \frac{dI_C}{d\beta} \quad -(2)$$

where both I_{CO} and V_{BE} are considered as constant.

These stability factor are written for convenience:

$$S = \frac{\Delta I_C}{\Delta I_{CO}}, \quad S' = \frac{\Delta I_C}{\Delta V_{BE}}, \quad S'' = \frac{\Delta I_C}{\Delta \beta}$$

Each differential quotient (partial derivative) is calculated with all other parameters mentioned constant.

BIAS COMPENSATION

The collector to base circuit and the self-bias circuit are used to limit the variation in the operating collector current I_c caused by variation in I_{CO}, V_{BE}, and β.

— These circuits are examples of feedback amplifiers which is used to reduce drastically the amplification of the signal.

— If this loss in signal gain is intolerable in a particular application, it is often possible to use compensating techniques to reduce the drift of the operating point.

— Very often both stabilization and compensation techniques are used to provide maximum bias and the thermal stabilization.

→ Diode, thermistors and Sensistors can be used to compensate for variations in current.

(i) Diode compensation:

Figure 1 shows a transistor amplifier with a diode 'D' connected across the base emitter junction for compensation of change in collector saturation current I_{CO}.

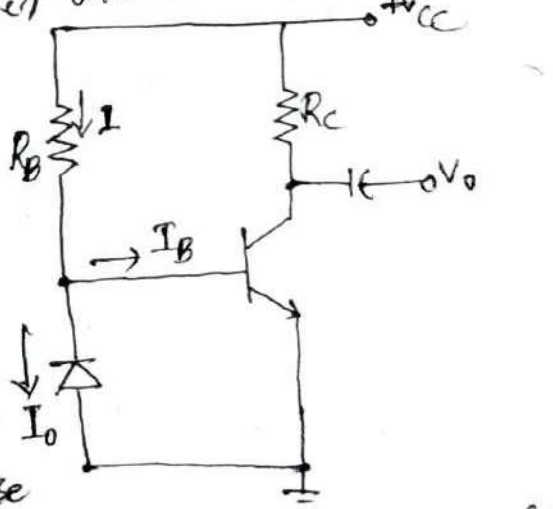


Fig.1: Diasbias Compensation

The diode is of the same material as the transistor and it is reverse biased by the base-emitter junction voltage V_{BE}, allowing the diode reverse saturation current I_o to flow through the diode D.

The base current $I_B = I - I_o$.

and we have $I_c = \beta I_B + (1+\beta) I_{CO} = \beta (I - I_o) + (1+\beta) I_{CO} \simeq \beta I - \beta I_o + \beta I_{CO}$

$\boxed{I_c \simeq \beta I}$ $\quad [\because 1+\beta \simeq \beta]$

As long as temparature is constant, diode D operates as a resistor. As the temparature increases, I_{CO} of the transistor increases. Hence, to compensate for this, the base current I_B should be decreased. This is the required action to keep I_C constant.

This method of bias compensation does not need a change in I_C to effect the change in I_B, as both I_D and I_{CO} can track almost equally according to the change in temparature.

(ii) Thermistor Compensation:

In Fig.②, a thermistor, R_T, having a negative temparature coefficient is connected in parallel with R_2.

The resistance of thermistor decreases exponentially with increase of temparature.

As increase in temparature will decrease the base voltage V_{BE}, reducing I_B and I_C.

Bias stabilization is provided by R_E and R_{CC}.

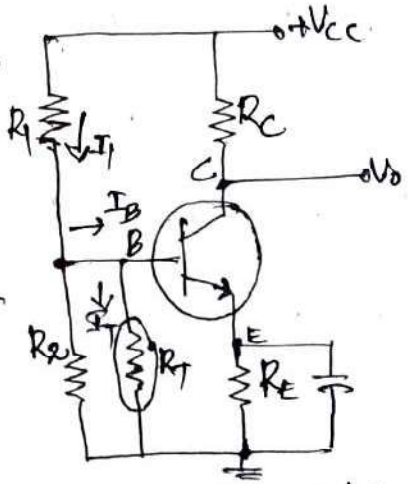


Fig.2: Thermister bias compensation

As T↑, R_T↓, I_T↑, I_B↓ → I_C↓

(iii) Sensistor Compensation;

Sensistor is a positive temparature coefficient element/resistance.

As temparature increases, R_S increases then, equivalent resistance of R_1 & R_S increases and V_{BE} decreases & reducing I_B & I_C.

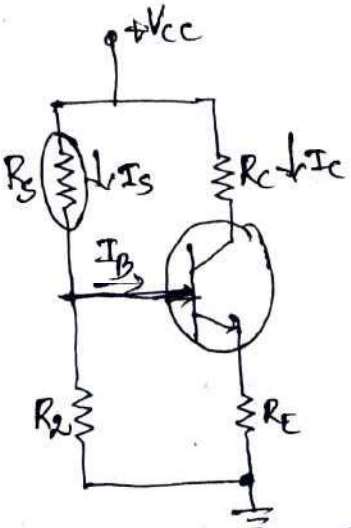
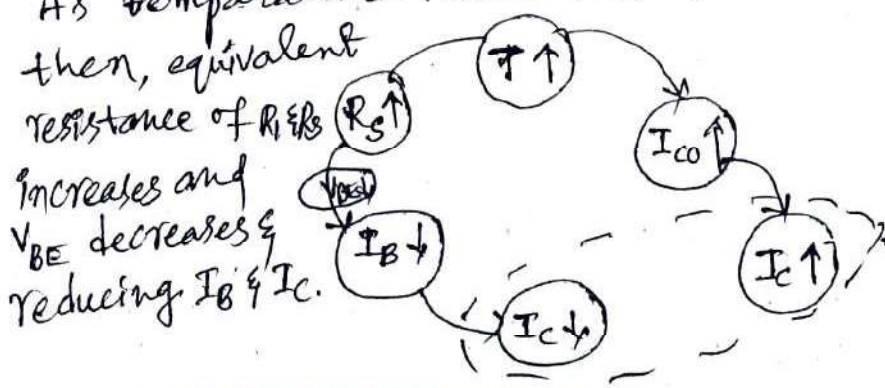
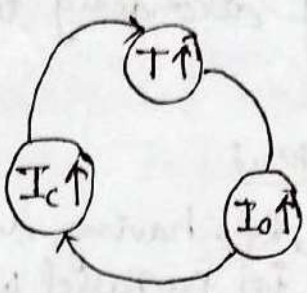


Fig.3: Sensistor circuit.



THERMAL RUNAWAY

Due to collection of charged particles by the collector, temperature across the collector-to-base junction (J_c) increases. As temperature increases, I_o increases intern I_c increases, and then again still temperature increases then I_o and I_c increases further as $I_c = \beta I_B + (1+\beta) I_o$.



This process becomes cumulative and at some particular stage, the temperature across the junction (J_c) becomes large and collector junction permanently damages. This process is called Thermal Runaway.

The self destruction of unstabilised transistor is called Thermal runaway.

→ The collector is normally made larger in size than the emitter inorder to help dissipate the heat developed at the collector junction.

- However, if the circuit is designed such that the base current I_B is made to decrease automatically with rise in temperature, then the decrease in βI_B will compensate for the increase in $(1+\beta) I_{CO}$, keeping I_c almost constant.

→ In power transistors, the heat developed at the collector junction may be removed by the use of heat sink, which is a metal sheet, fitted to the collector and whose surface radiates quickly.

Thermal Resistance:

The steady state rise in temperature at the collector junction is proportional to the power dissipated at the junction,

or $\Delta T = T_J - T_A \propto P_D$ — (1) where T_j – junction temperature
T_A – Ambient temperature
P_D – Power dissipation at the J_c junction

Equation is written as $T_j - T_A = \theta P_D$ — (2)

where θ is the constant of proportionality and is called thermal resistance in °c/w.

CONDITION FOR THERMAL STABILITY

For preventing thermal runaway, the required condition is that the rate at which the heat is released at the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition.

Hence, the condition to be satisfied to avoid thermal runaway is given by $\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j}$ — (1)

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta} \quad — (2)$$

$\left[\because \frac{d}{dT_j}\left[T_j - T_A\right] = \frac{d}{dT_j}\left[\theta P_D\right] \right.$

$\frac{dT_j}{dT_j} - \frac{d(T_A)}{dT_j} = \theta \frac{dP_D}{dT_j}$

$1 = \theta \frac{dP_D}{dT_j}$

$\left. \frac{dP_D}{dT_j} = \frac{1}{\theta} \right]$

→ If the circuit is properly designed, then the transistor cannot runaway below a specified ambient temperature or even any conditions.

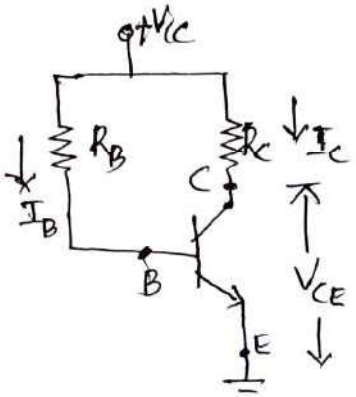
Consider the fixed bias circuit,

$$P_C = V_{CE} \cdot I_C \quad — (3)$$

Apply KVL to the output loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C \quad — (4)$$



Then $P_C = V_{CE} \cdot I_C = (V_{CC} - I_C R_C) I_C$

$$P_C = V_{CC} \cdot I_C - I_C^2 R_C \quad — (5)$$

Apply differentiation w.r.t I_C, $\frac{dP_C}{dI_C} = V_{CC} \cdot \frac{dI_C}{dI_C} - \frac{d}{dI_C}(I_C^2 R_C)$

$$= V_{CC} - 2I_C \cdot R_C \quad — (6)$$

As $\frac{dP_c}{dT_j} < \frac{1}{\theta}$,

$$\frac{dP_c}{dI_c} \times \frac{dI_c}{dI_o} \times \frac{dI_o}{dT_j} < \frac{1}{\theta}$$

$$(V_{cc} - 2I_cR_c) \cdot S \cdot (7\% I_o) < \frac{1}{\theta}$$

$$(V_{cc} - 2I_cR_c) \cdot S \cdot (0.07 I_o) < \frac{1}{\theta}$$

To avoid thermal runaway, the condition is

$V_{cc} - 2I_cR_c < 0$ [$\because$ S, I_o & θ are positive]

$V_{cc} < 2I_cR_c$

$\frac{V_{cc}}{2R_c} < I_c$ or $\boxed{I_c > \frac{V_{cc}}{2R_c}}$ — (7)

Then $V_{CE} = V_{cc} - I_cR_c = V_{cc} - \left(\frac{V_{cc}}{2R_c}\right)R_c < \frac{V_{cc}}{2}$

$\therefore \boxed{V_{CE} < \frac{V_{cc}}{2}}$ — (8).

APPLICATIONS

1. As a Switch:

When a transistor is used as a switch, it is usually made to operate alternatively in the cutoff condition and in saturation. This can be used for computer and control applications.

2. An Amplifier:

The basic amplifying action was produced by transferring a current I from a low to a high resistance circuit. The combination of the two terms results in the label transistor, that is

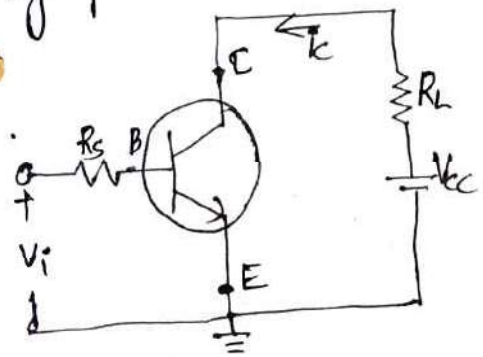
transfer + resistor → transistor

3. An Inverter:

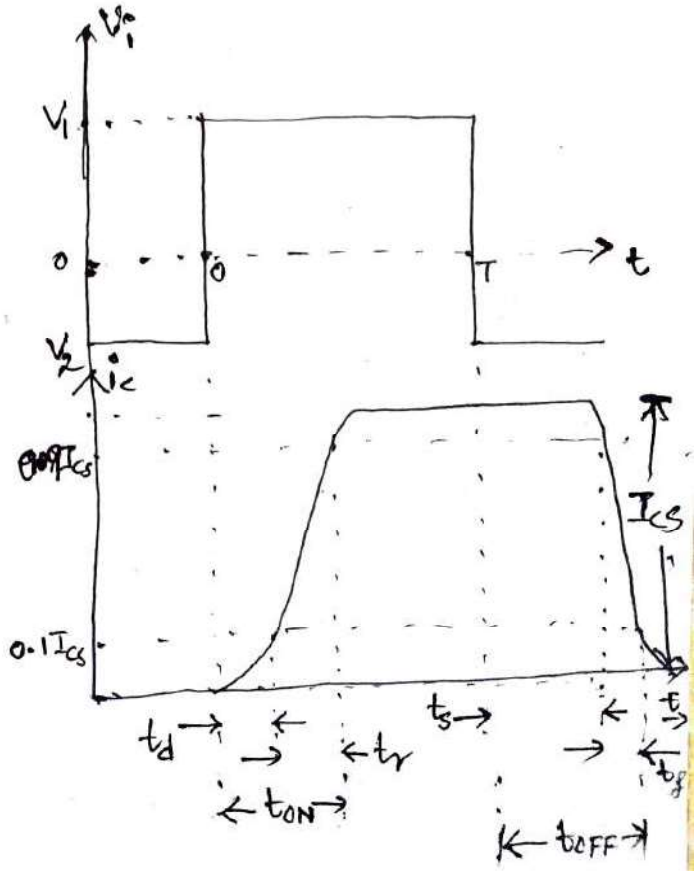
Common Emitter configuration can be employed as an inter in computer logic circuitry.

TRANSISTOR SWITCHING TIMES

Consider the transistor circuit shown in fig. (1a) driven by pulse wave-forms:



(a)



(b)

Fig. 1: (a) CE configuration
(b) input pulse & o/p wave-form.

The input waveforms applied between base and emitter through a resistor R_s, and the response of the collector current i_c to the waveform, together with its time relationship to that waveform as shown in Fig. 1b.

The current does not immediately respond to the input signal, instead there is a delay, and the time that elapses during this delay.

Consider the following timing definitions;

Delay time, t_d:

The time required for the current to rise to 10 percentage of its maximum (saturation) value is called the delay time, t_d.

Rise time, t_r:

The time required for the current to rise from 10 to 90 percent of I_{cs}.

Turn-ON time, t_{ON}:

The total turn-ON time t_{ON} is the sum of the delay and rise time, $t_{ON} = t_d + t_r$.

Storage time, t_s:

The interval which elapses between the transition of the input waveform and the time when i_c has dropped to 90% of I_{cs} is called the storage time, t_s.

Fall time, t_f:

The time required for i_c to fall from 90 to 10% of I_{cs} is called as Fall time, t_f.

Turn-OFF time, t_{off}:

It is defined as the sum of the storage time and fall time, $t_{OFF} \equiv t_s + t_f$.

(P1) Design the circuit shown in Fig. (P1), given Q-point values are to be $I_{CQ} = 1mA$ and $V_{CEQ} = 6V$. Assume that $V_{CC} = 10V$, $\beta = 100$ and $V_{BE(on)} = 0.7V$.

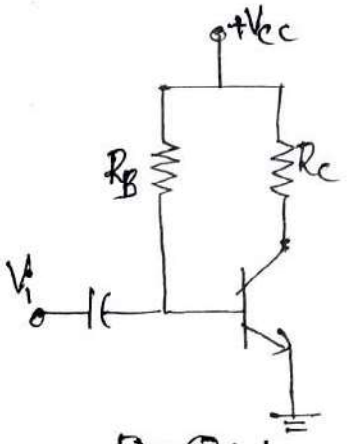


Fig. (P1):

Solu: The collector resistance is

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{10-6}{1mA} = 4K\Omega$$

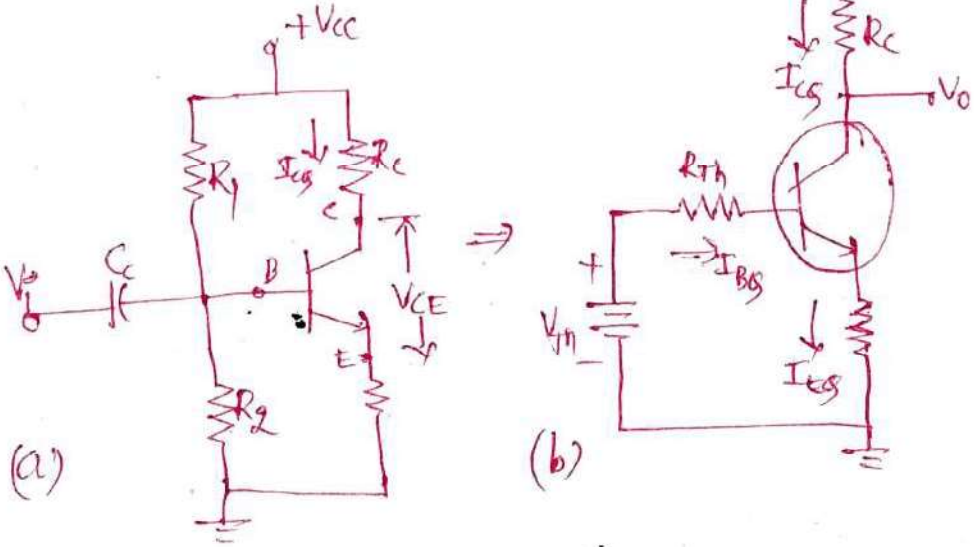
The base current is

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1\times10^{-3}}{100} = 10\mu A$$

The base resistance is

$$R_B = \frac{V_{CC} - V_{BE(on)}}{I_{BQ}} = \frac{10-0.7}{10\times10^{-6}} = 0.93M\Omega \simeq 1M\Omega.$$

(P2) Given a voltage divider bias circuit shown in Fig. (P2), determine the Q-point. Let $R_1 = 56K\Omega$, $R_2 = 12.2K\Omega$, $R_C = 2K\Omega$, $R_E = 400\Omega$, $V_{CC} = 10V$, $V_{BE(on)} = 0.7V$ and $\beta = 150$.



Solu: From Fig. (b),

$$R_{TH} = R_1 \| R_2 = 56K\Omega \| 12.2K\Omega = 10K\Omega$$

$$V_{TH} = \left(\frac{R_2}{R_1+R_2}\right)V_{CC} = \frac{12.2K}{56K+12.2K}\times10 = 1.79V$$

With the help of Kirchhoff's Voltage Law equation, we get

$$I_{BQ} = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E} = \frac{1.79 - 0.7}{10 + (151)(0.4)} = 15.5\mu A$$

Therefore, $I_{CQ} = \beta I_{BQ} = 150 \times 15.5 \times 10^{-6} = 2.32mA$.

$$I_{EQ} = I_{BQ} + I_{CQ} = 15.5\mu A + 2.32mA = 2.336mA.$$

$$V_{CEQ} = V_{CC} - I_{CQ}R_C - I_{EQ}R_E$$
$$= 10 - 2.32 \times 10^{-3} \times 2 \times 10^3 - 2.336 \times 10^{-3} \times 400 = 4.426V$$

(P3) A transistor has $I_B = 100\mu A$ and $I_C = 2mA$. Find (a) β of the transistor; (b) α of the transistor; (c) emitter current, I_E; (d) if I_B changes by $25\mu A$ and I_C changes by $+0.6mA$, find the new value of β.

Solu: Given $I_B = 100\mu A = 100 \times 10^{-6} A$ and $I_C = 2mA = 2 \times 10^{-3} A$.

a) To find β:

$$\beta = \frac{I_C}{I_B} = \frac{2 \times 10^{-3} A}{100 \times 10^{-6} A} = \frac{2}{100} \times 1000 = 20.$$

b) To find α:

$$\alpha = \frac{\beta}{\beta+1} = \frac{20}{20+1} = \frac{20}{21} = 0.952$$

c) To find Emitter current, I_E:

$$I_E = I_B + I_C = 100 \times 10^{-6} + 2 \times 10^{-3} A = (0.01 \times 10^{-3} + 2 \times 10^{-3})A$$
$$= 2.01mA.$$

(d) To find new value of β when $\Delta I_B = 25\mu A$ and $\Delta I_C = 0.6mA$

Therefore, $I_B = I_B + \Delta I_B = (100 + 25)\mu A = 125\mu A$

$I_C = I_C + \Delta I_C = (2 + 0.6)mA = 2.6mA$.

New value of β of the transistor, $\beta = \frac{I_C}{I_B} = \frac{2.6mA}{125\mu A} = 20.8$.

(P4) A Germanium transistor used in a complementary symmetry amplifier has $I_{CBO} = 10\mu A$ at 27°C and $h_{fe} = 50$. Find I_C when $I_B = 0.25mA$.

Solu: Given $I_{CBO} = I_{CO} = 10\mu A$ and $h_{FE} = \beta = 50$.

We have $I_C = \beta I_B + (1+\beta) I_{CBO} = 50 \times (0.25 \times 10^{-3}) + (1+50)(10 \times 10^{-6} A)$

$$\boxed{I_C = 13.01mA.}$$

Transistor Biasing

Transistor having three Configuration: Common Base, Common Emitter, and Common Collector Configurations. Comparision of CB, CE and CC Configurations are Shown in below.

	Common Base Configuration	Common Emitter Configuration	Common Collector Configuration
Input impedence R_i	Very Small	Moderate	Very high
O/p impedence R_o	Very Large	Moderate	Very Small
Current Gain A_I	$\alpha = \frac{I_C}{I_E} \simeq 1$ almost unity	$\beta = \frac{I_C}{I_B} \simeq 50$ to 500 Moderate	$\gamma = \frac{I_E}{I_B} \simeq 51$ to 501 Very High.
Voltage Gain A_V	Very High	Moderate	less than one
Applications	It is used as Voltage amplifies only because current gain is unity	It is used as Voltage and Current amplifier. Power Amplifies	It is used as Current Amplifies.

From above table, Common Emitter Configuration is preferred as Compare to Common Base and Common Collector Conf.

If we want device used in perticulas application, according to that application device is properly biased by external Source.

Transistor also having 3 applications i) ON Switch
ii) OFF Switch
iii) Amplifies
iv) Attenuator.

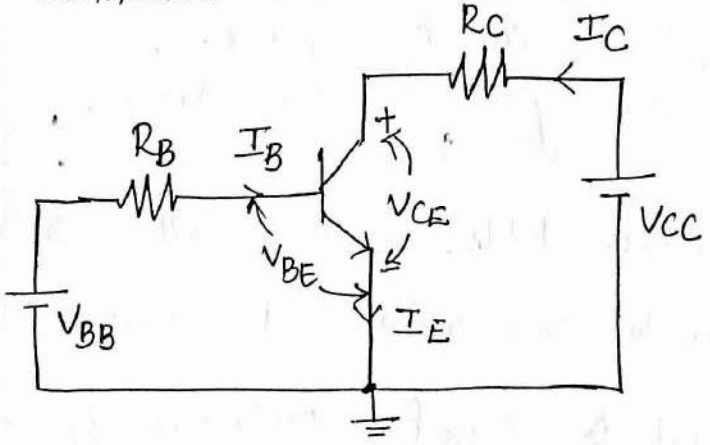
Any device having some limitations, Similarly transistor having 3 limitations : i) Max power dissipation
ii) Max forward Current
iii) Max reverse voltage or PIV

So transistor must be operated with in this limits only, when the duice exceding this limits, duice may damages due to excess heat.

DC load line and Quiesent (or) Q-point :-

The output Characteristics Can't give the direct relation between output voltage and output Current. Therefore, we need a DC loadline which is the Stright line on the output Characteri with a DC Slope Such that there would be direct relation b/n output voltage and output Current.

Now letus consider the amplifier Circuit for output Characteristics of BJT in CE configuration without any Signal Connected to it. This Condition is known as " Quiesent Conditi



Applying KVL in the output loop.

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

$$I_C R_C = V_{CC} - V_{CE}$$

$$\therefore I_C = \frac{V_{CC} - V_{CE}}{R_C} \longrightarrow (1)$$

eqn(1) is called as "load line equation".

When $V_{CE} = 0$ in eqn(1)

$I_C = \frac{V_{CC}}{R_C}$ ⟶ This is the point on y-axis.

When $I_C = 0$ in eqn (1)

$$I_C R_C = V_{CC} - V_{CE}$$

$$0 = V_{CC} - V_{CE}$$

$V_{CC} = V_{CE} \longrightarrow$ This is the point on X-axis.

Load line can be plotted on the Static o/p V-I Characteristics shown in below Fig.

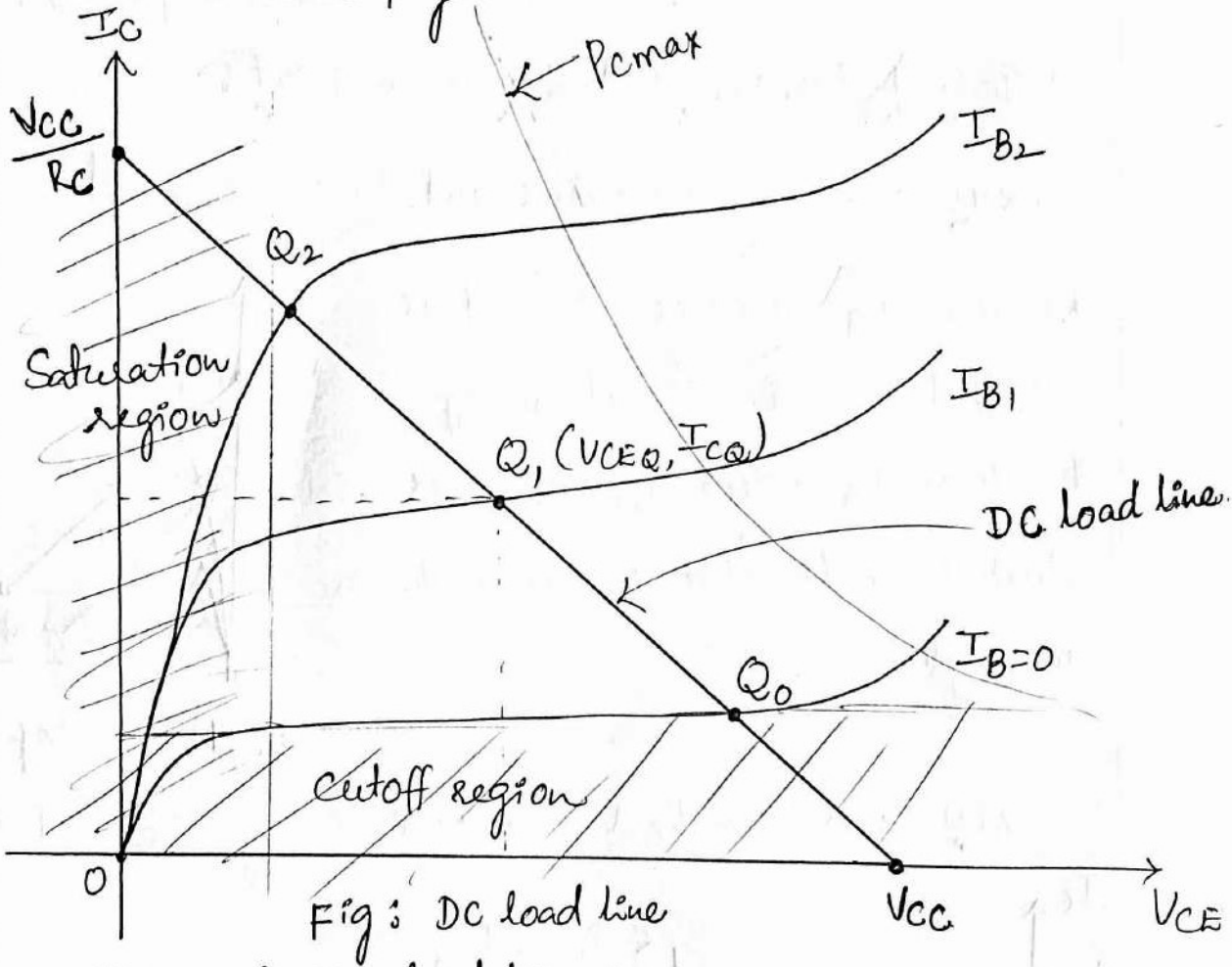


Fig: DC load line

Slope of DC load line:

$$\left(0, \frac{V_{CC}}{R_C}\right), (V_{CC}, 0)$$

(x_1, y_1) (x_2, y_2)

* Slope $m = \frac{y_2 - y_1}{x_2 - x_1} = \frac{0 - \frac{V_{CC}}{R_C}}{V_{CC} - 0} = \frac{-\frac{V_{CC}}{R_C}}{V_{CC}} = \frac{-1}{R_C}$

Q-point lies on DC load line, where DC load line gives the relation between o/p current I_C and o/p voltage V_{CE}.

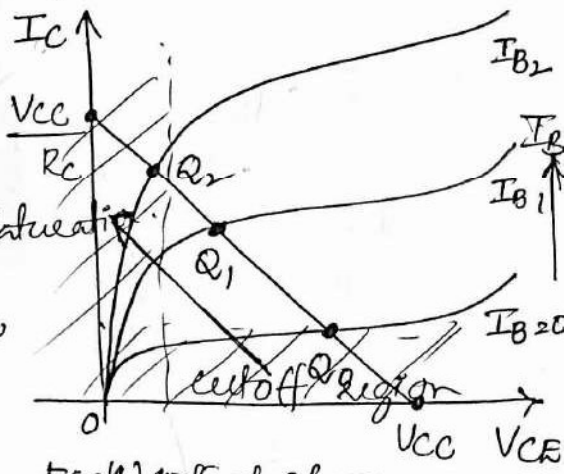
From above Fig, Q-point is depends on I_B and V_{CC} and R_C. Never choose Q point in the Saturation region, cutoff region and P_{cmax} region and above I_{cmax} and V_{cmax}. Because in Saturation region and cutoff region transistor not act as amplifier.

Hence Q-point has to fixed at active region (unshaded region in above Fig) to get the faithfull amplication.

Effects of I_B, V_{CC} and R_C on Q-point :-

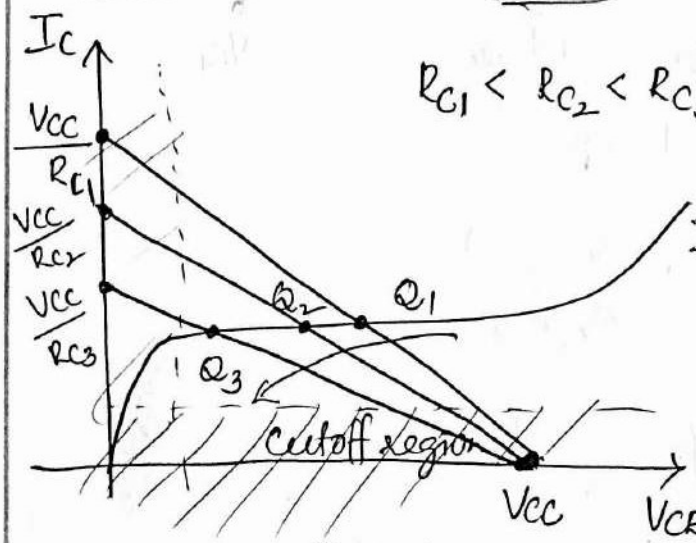
Case(1) :- When I_B Varies and keeping V_{CC} and R_C is constant.

* When I_B increases, Q point is shifted towards Saturation region.
* When I_B decreases, Q point is shift towards cutoff region as shown in Fig(1).



Fig(1): Effect of I_B on Q point

Case(2) :- When R_C Varies and keeping V_{CC} and I_B is constant



$R_{C1} < R_{C2} < R_{C3}$

* When R_C increases Q is shifted towards Saturation region.
* When R_C increases, $I_C \left(= \frac{V_{CC}}{R_C}\right)$ decreases.

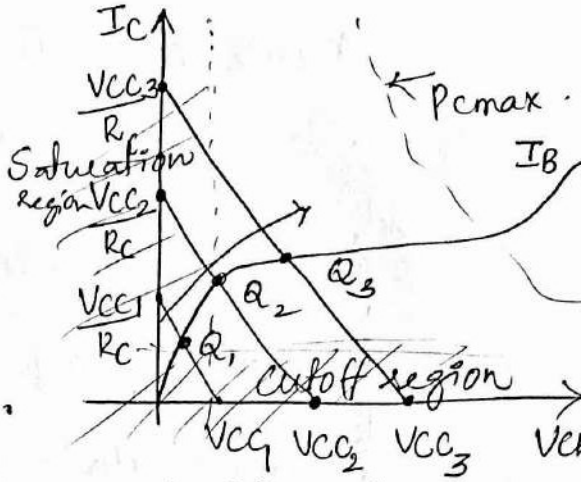
Fig(2): Effect of R_C on Q point.

Case(3) :- When V_{CC} ~~decreases~~ Varies, I_B and R_C kept constant.

$$V_{CC1} < V_{CC2} < V_{CC3}$$

When V_{CC} is varying and I_B and R_C are constant.

From Fig (3) when V_{CC} increases Q point shift towards Pcmax region. When V_{CC} decreases Q point is shift towards Saturation region.



Fig(3): Effect of V_{CC} on Q point.

From Fig(1), (2) and (3), when V_{CC}, R_C and I_B are Varies Q-point also varies i.e Q-point is not Stable.

Even V_{CC}, R_C and I_B are kept constant, Q-point is not Stable, why because Q-point gives the relation between O/p current (I_C) and O/p voltage (V_{CE}).

$$\text{But } I_C = \beta I_B + I_{CO}(1+\beta) \longrightarrow (1)$$

Here I_C is depends on 3 parameters those are V_{BE}, β, I_{CO} from equ(1) I_C is depends on I_B, β and I_{CO}.

$$I_C = fun(I_{CO}, I_B, \beta)$$

where I_B is depends on V_{BE}

$$I_C = fun(I_{CO}, V_{BE}, \beta)$$

But these 3 parameters are depends on Temperature.

* i) I_{CO} is double for every 10°C rise in temperature.

$$I_{CO2} = I_{CO1} \cdot 2^{(T_2 - T_1)/10}$$

* ii) $\frac{dV_{BE}}{dT} = -2.5\,mV/^\circ C$ i.e for every 1°C rise in temp

causes V_{BE} is decreases to 2.5mV.

* (iii) β is double for every 100°C rise in temperature → for Si
  β is double for every 50°C rise in temperature → for Ge.

So I_C depends on temperature, ∴ even fixing the V_{CC}, R_C and I_B, Q point is not fixed i.e not stable because I_C is varies with respect to temperature. So Q point (I_C, V_{CE}) varies with respect to I_C.

$$\therefore I_C = fun(I_{CO}, V_{BE}, \beta)$$

Total change of I_C with respect to I_{CO}, V_{BE} and β is given by the taylor's series.

$$\Delta I_C = \frac{\partial I_C}{\partial I_{CO}} \Delta I_{CO} + \frac{\partial I_C}{\partial V_{BE}} \Delta V_{BE} + \frac{\partial I_C}{\partial \beta} \Delta \beta$$

$$\Delta I_C = S \Delta I_{CO} + S' \Delta V_{BE} + S'' \Delta \beta$$

where S, S' and S'' are called "Stability factors".

$$S = \frac{\partial I_C}{\partial I_{CO}} \quad \text{i.e Change in } I_C \text{ w.r.t } I_{CO}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} \quad \text{i.e Change in } I_C \text{ w.r.t } V_{BE}$$

$$S'' = \frac{\partial I_C}{\partial \beta} \quad \text{i.e Change in } I_C \text{ w.r.t } \beta$$

But in 3 stability factors, I_{CO} is more effected by the temperature. So I_C is more depends on I_{CO}.

The effect due to V_{BE} and β almost get cancelled on I_C. So no need to consider S' and S''. So we are

mostly concentrate on S i.e change in I_C w.r.t I_{CO}

Consider the current equation I_C

$$I_C = \beta I_B + (1+\beta) I_{CO} \longrightarrow (1)$$

Partially differentiate eqn(1) w.r.t I_C.

$$\frac{\partial I_C}{\partial I_C} = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$(1+\beta) \frac{\partial I_{CO}}{\partial I_C} = 1 - \beta \frac{\partial I_B}{\partial I_C}$$

$$\frac{\partial I_{CO}}{\partial I_C} = \frac{1 - \beta \frac{\partial I_B}{\partial I_C}}{1+\beta}$$

***

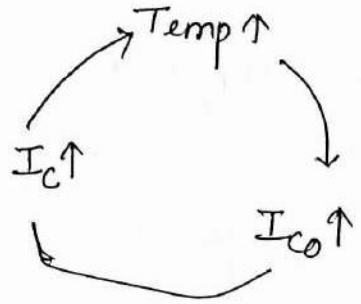
$\therefore$ Stability factor $S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$.

Small Value of Stability factor gives the more Stability to the device. That means, when $\frac{\partial I_C}{\partial I_{CO}}$ is Small i.e change in I_C Small with respect to I_{CO}, So device is said to be more Stable that means device gives constant o/p current I_C irrespective of Change in Temperature.

So for increasing the Stability of the device, we are using the different "biasing methods (or Stabilization methods".

Thermal runaway :-

When Temperature increases, I_{CO} increases, So I_C increases. When I_C increases, junction temperature increases, due to that temperature, again I_{CO} increases hence I_C increases, again temperature increases. This process is Cumulative in nature. So at particular large temperature device can spoil due to the excess heat. This phenominon is called "Thermal runaway".



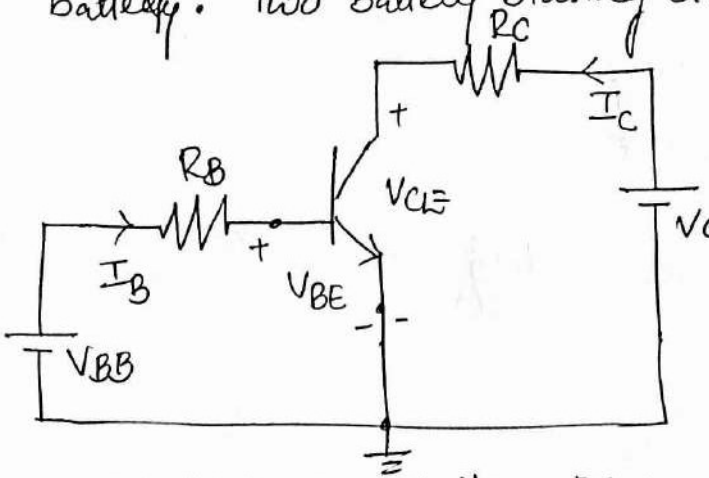
Biasing Techniques (or) Stabilization Techniques :-

For improving the Stability of device, we are using biasing techniques.

i) Two battery Biasing Circuit
ii) Fixed Biasing Circuit
iii) Fixed Bias with emitter resistance (R_E)
iv) Collector to Base Bias
v) Collector to Base Bias with emitter resistance (R_E)
vi) Self Bias (or) Voltage divider Bias (or) Emitter Bias.

9> Two Battery Biasing Circuit :-

In two battery biasing circuit, for making the input junction forward bias we are using one battery and for making the o/p junction reverse bias we are using one more battery. Two Battery biasing circuit is shown in Fig(1)



Fig(1): Two Battery Bias

input KVL

$$-V_{BB} + I_B R_B + V_{BE} = 0$$

$$I_B R_B = V_{BB} - V_{BE}$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} \rightarrow (1)$$

Partial diff of eqn(1) w.r.t I_C

$$\frac{\partial I_B}{\partial I_C} = 0 \rightarrow (2)$$

$$\therefore \text{Stability factor} = S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$$

$$\therefore S = \frac{1+\beta}{1-\beta(0)} \quad \left[\because \frac{\partial I_B}{\partial I_C} = 0\right]$$

*

$$\therefore \text{Stability factor } S = 1+\beta$$

β range is varies from 50 to 500, so Stability factor is very high that means, Change in I_C w.r.t I_{CO} is very high, so device having less Stability.

Advantages :-

i) Simple circuit

ii) No loss of gain because there is no feedback.

Disadvantages :-

i) Two batteries, so cost is very high

ii) Stability is very poor

iii) Q-point is not stable.

General procedure for Finding the Q-point for all biasing techniques :-

1) Write input KVL

2) In i/p KVL, Substitute $V_{BE active}$ i.e 0.7 for Si and 0.2 for Ge and find the I_B. Calculate I_C i.e $I_{CQ} = \beta I_B$

3) Write o/p KVL

in o/p KVL Sub I_{CQ} Value, find V_{CEQ}

$\therefore$ Q point = (V_{CEQ}, I_{CQ})

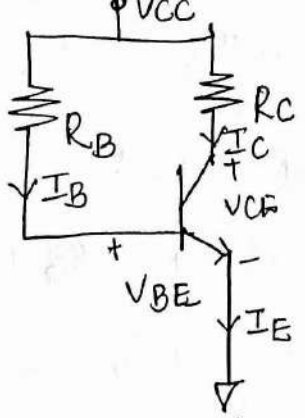
2) Fixed Biasing Technique :-

In Fixed Biasing Technique only one battery is used, so cost is reduced compare to Two battery biasing technique.

Fixed Biasing Technique is shown in below Fig(2)

In this tech Condition to get the Biasing is

$R_B >> R_C$.



Fig(2): Fixed Bias Technique

input KVL is

$$-V_{CC} + I_B R_B + V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow (1)$$

Partialy Diff eqn(1) w.r.t I_C

$$\frac{\partial I_B}{\partial I_C} = 0 \rightarrow (2)$$

$$\text{Stability factor } S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$$

Sub eqn(2) in Stability factor S

$$\therefore S = \frac{1+\beta}{1-\beta(0)}$$

Stability factor = $S = 1+\beta$.

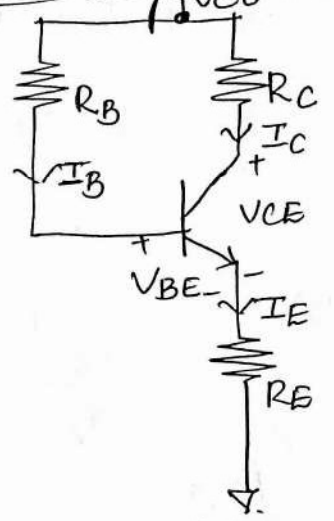
Advantages:-

i) Compare to two battery circuit, cost is reduced
ii) Simple circuit
iii) No loss of Gain.

Disadvantages:-

i) Stability of device is very poor
ii) Q-point is not stable.

3) Fixed biasing Circuit with emitter resistance:-



Fig(3): Fixed Bias with R_E

Input KVL :

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$$

Where $I_E = I_B + I_C$

$$-V_{CC} + I_B R_B + V_{BE} + (I_B + I_C) R_E = 0$$

$$-V_{CC} + I_B R_B + I_B R_E + V_{BE} + I_C R_E = 0$$

$$I_B(R_B + R_E) = V_{CC} - V_{BE} - I_C R_E$$

$$\therefore I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E} \longrightarrow (1)$$

Partially diff eqn (1) w.r.t I_C

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E} \longrightarrow (2)$$

Where Stability factor $S = \dfrac{1+\beta}{1 - \beta \dfrac{\partial I_B}{\partial I_C}}$.

Sub eqn (2) in Stability factor S

$$S = \frac{1+\beta}{1 - \beta\left(\dfrac{-R_E}{R_B + R_E}\right)}$$

$$S = \frac{1+\beta}{1 + \beta \dfrac{R_E}{R_B + R_E}} \longrightarrow (3)$$

in eqn(3) if $R_E >> R_B$

$$R_B + R_E \simeq R_E$$

So

$$S = \frac{1+\beta}{1+\beta \cdot \frac{R_E}{R_E}}$$

$$S = \frac{1+\beta}{1+\beta}$$

$$\boxed{S = 1}.$$

Advantages :-

Compare to fixed bias and two battery bias circuit, it gives more stability.

Disadvantages :-

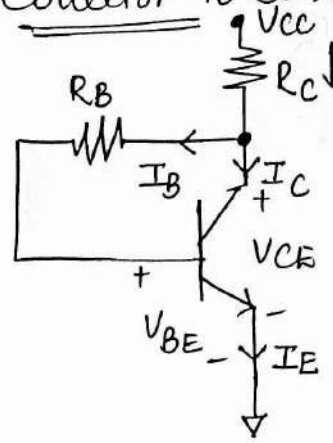
Loss of Gain because R_E provides -ve feed back to the circuit.

Role of R_E :-

1. By selecting High value of R_E we can get stability factor as 1 means stability will increases.

2. When R_E increases to get Good stability, but I_B decreases (from eqn(1)), when I_B decreases I_C also decrease ($\because I_C = \beta I_B$) hence Gain reduces.

4) Collector to Base Bias technique:-



In Collector to Base biasing method, resistance R_B is connected from collector terminal to Base terminal.

Write the input KVL

$$-V_{CC} + R_C(I_B + I_C) + I_B R_B + V_{BE} = 0$$

$$I_B(R_C + R_B) = V_{CC} - V_{BE} - I_C R_C$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \longrightarrow (1)$$

Equation (1), partialy diff w.r.t I_C

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B} \longrightarrow (2)$$

Stability factor $$S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

Sub equ(2) in Stability factor.

$$S = \frac{1+\beta}{1-\beta\left(\frac{-R_C}{R_C+R_B}\right)}$$

$$S = \frac{1+\beta}{1+\beta\frac{R_C}{R_C+R_B}}$$

When $R_C >> R_B$

$$R_B + R_C \simeq R_C$$

$\therefore$ Stability factor $S = \dfrac{1+\beta}{1+\beta\left(\dfrac{R_B}{R_C}\right)}$

$$= \frac{1+\beta}{1+\beta} = 1$$

$\therefore$ Stability factor $S = 1$.

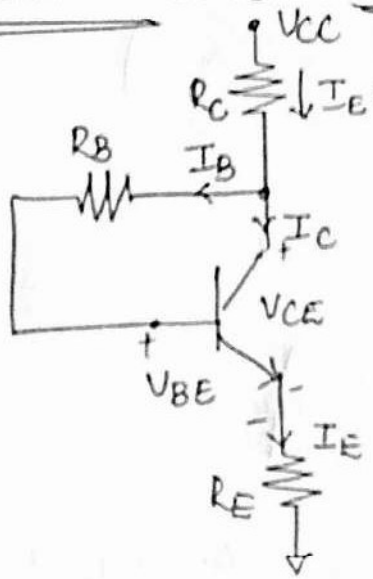
Advantages :-

Compare to fixed bias, fixed bias with R_E it gives more Stability.

Disadvantage :-

Loss of Gain due to feedback resistance R_C.

5) Collector to Base Bias with R_E :-



Write the Input KVL

$$-V_{CC} + (I_B + I_C)R_C + I_B R_B + V_{BE} + (I_B + I_C)R_E = 0.$$

$$I_B(R_C + R_B + R_E) = V_{CC} - V_{BE} - (R_C + R_E) I_C$$

$$\therefore I_B = \frac{V_{CC} - V_{BE} - (R_C + R_E) I_C}{R_C + R_B + R_E} \longrightarrow (1)$$

partially diff eqn(1) w.r.t I_C

$$\frac{\partial I_B}{\partial I_C} = \frac{-(R_C + R_E)}{R_C + R_B + R_E} \longrightarrow (2)$$

Sub eqn (2) in Stability factor S

$$\text{where } S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

$$S = \frac{1+\beta}{1-\beta\left(\frac{-(R_C+R_E)}{R_B+R_C+R_E}\right)}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C+R_E}{R_B+R_C+R_E}\right)}$$

Generally $(R_C+R_E) > R_B$

hence $R_C+R_E+R_B \simeq R_C+R_E$.

$$\therefore S \simeq \frac{1+\beta}{1+\beta\left(\frac{R_C+R_E}{R_C+R_E}\right)}$$

$$S \simeq \frac{1+\beta}{1+\beta} = 1.$$

∴ Stability factor S = 1

Advantages :-

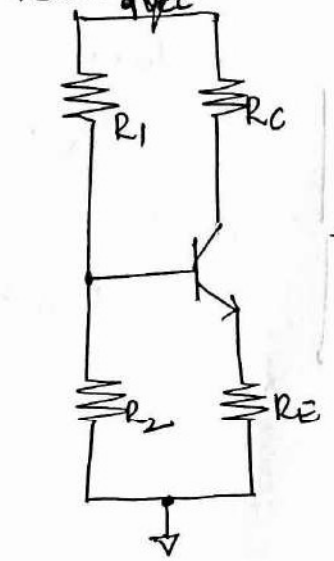
Compare previous Biasing techniques, it gives good stability

Disadvantages :-

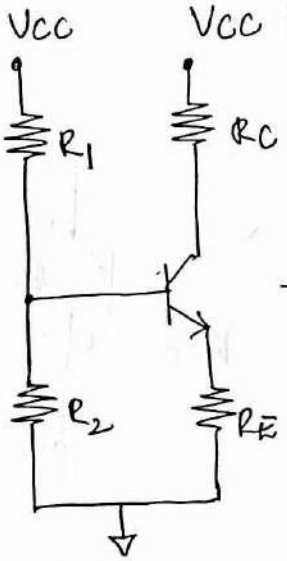
Loss gain due to prentence of R_C and R_E (more -ve Feedback

6) Self biasing Circuit (or) Voltage divider Circuit (or) Emitter Biasing Circuit :-

This biasing Circuit provides more stability to the device Compare to all biasing Circuit. In this biasing Circuit, Voltage division takes place between R_1 and R_2 hence this biasing technique also called as Voltage divider Biasing technique.



Fig(6): Self Bias Circuit



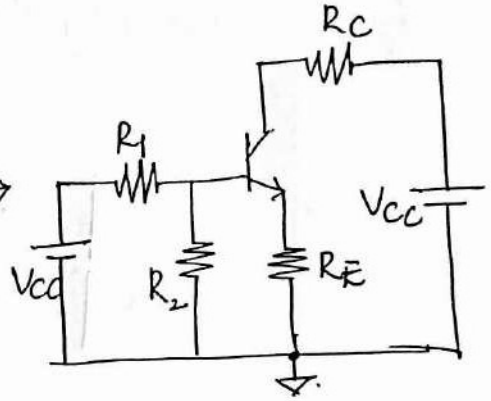
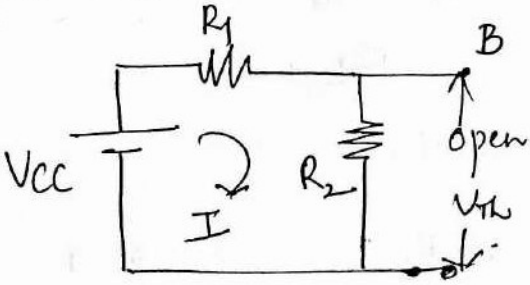


Fig 6(a,b): Equivalent Circuit diagrams for self bias.

To fininding Current flowing towards base (or) Voltage drop across the base and ground, we will apply Thevinian theorem.

To finding voltage drop across the base to ground open Circuit the device :-



KVL

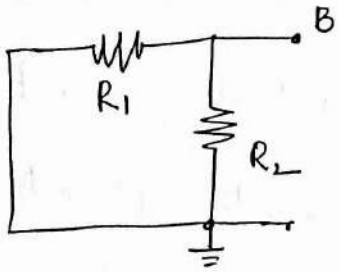
$$-V_{CC} + IR_1 + IR_2 = 0$$

$$I = \frac{V_{CC}}{R_1 + R_2}$$

$$\therefore V_{Th} = IR_2 = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

To finding equivalent Resistance (or) Thevinian Resistance,

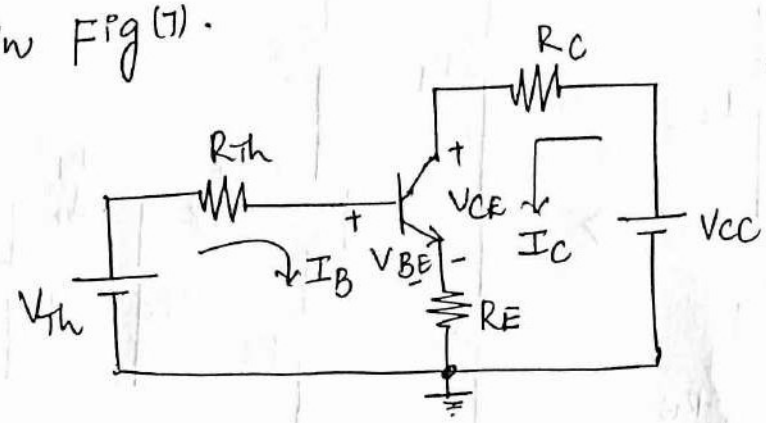
Short Circuit the Voltage Source



$$R_{Th} = R_1 // R_2$$

$$= \frac{R_1 R_2}{R_1 + R_2}$$

By using R_{Th} and V_{Th} Fig(6) again redraw as shown in Fig(7).



where

$$V_{Th} = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

Write the input KVL

$$-V_{Th} + I_B R_{Th} + V_{BE} + I_E R_E = 0$$

where $I_E = I_B + I_C$

$$-V_{Th} + I_B R_{Th} + V_{BE} + (I_B + I_C) R_E = 0$$

$$-V_{Th} + I_B R_{Th} + V_{BE} + I_B R_E + I_C R_E = 0$$

$$I_B (R_{Th} + R_E) = V_{Th} - V_{BE} - I_C R_E$$

$$\therefore I_B = \frac{V_{Th} - V_{BE} - I_C R_E}{R_{Th} + R_E} \longrightarrow (1)$$

differentiate eqn(1) w.r.t I_C.

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_{Th} + R_E} \longrightarrow (2)$$

Stability factor $S = \dfrac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}}$

$$= \frac{1+\beta}{1-\beta\left(\dfrac{-R_C}{R_{Th}+R_C}\right)}$$

$$= \frac{1+\beta}{1+\dfrac{\beta R_C}{R_{Th}+R_C}} \qquad R_C >> R_{Th}$$

$\therefore R_{Th}+R_C \simeq R_C$

$$\simeq \frac{1+\beta}{1+\beta\dfrac{R_C}{R_C}}$$

$$S \simeq \frac{1+\beta}{1+\beta} = 1 \qquad \boxed{\therefore S \simeq 1}$$

Stability factor S (i.e change in I_C w.r.t I_{CO}) is very small, so Stability of the device is very High.

O/p KVL :-

$$-V_{CC} + I_C R_C + V_{CE} + R_E(I_C + I_B) = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) - I_B R_E \longrightarrow (3)$$

From eqn(1), we can find I_{CQ} i.e βI_B

From eqn(3), we can find V_{CEQ}

$\therefore$ Q-point = (V_{CEQ}, I_{CQ}).

Advantages :-

i) cost is very less because one battery is used

ii) Stability is very high if $\frac{R_{Th}}{R_E} << 1$.

Disadvantages:-

Due to the presence of R_E in the Selfbiasing circuit, gain is losses because R_E is provides feedback from o/p to input.

Compensation Techniques:-

When biasing techniques fail to give more stability to the device, we are going for the compensation techniques.

Compensation Techniques:-

i) Diode Compensation Technique
(Compensation against I_{CO})

ii) Thermistor compensation Technique
(Compensation tech against V_{BE}).

i) Diode compensation Technique:-

In Selfbias circuit, R_2 is placed replaced by diode in Reverse bias as ashown in below Fig(7).

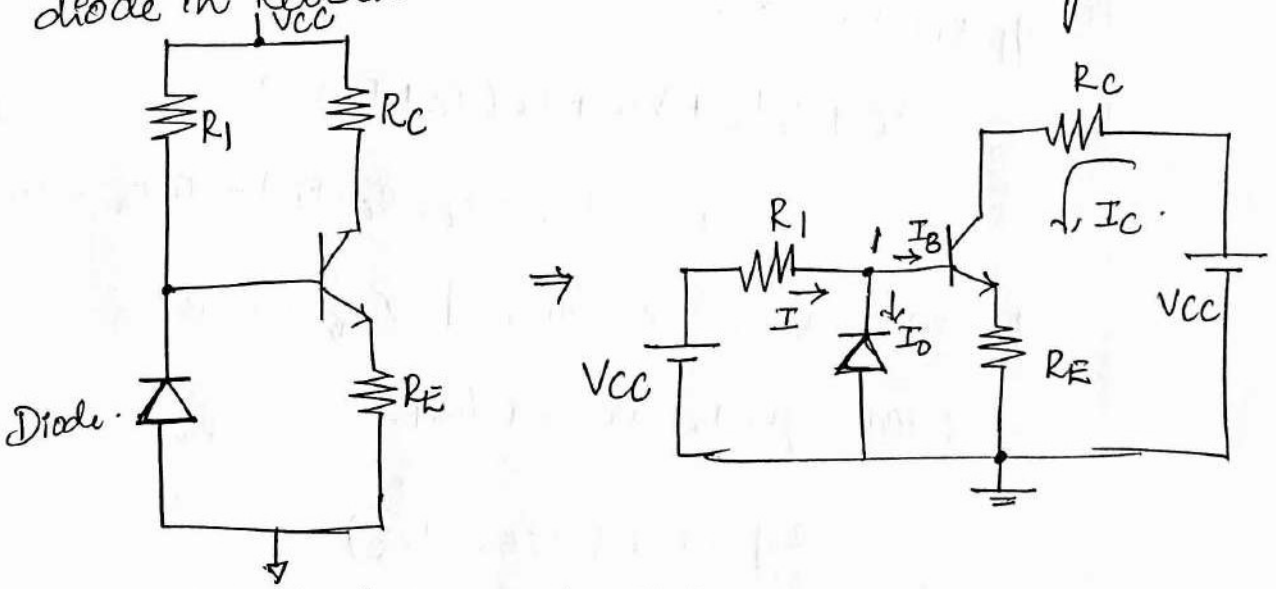


Fig (7): Diode Compensation Tech

In Fig (7), diode is operating in Reverse bias, hence it allows reverse Saturation current.

at node 'I', current division taken place, one current towards diode, another current toward base of BJT (I_B).

(I_0)

From the KCL at node I

Total current $I = I_0 + I_B$

$$I_B = (I - I_0) \longrightarrow (1)$$

From the current equation of CE Configuration i.e

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

where $\beta >> 1$ hence $1+\beta \simeq \beta$

$$\therefore I_C \simeq \beta I_B + \beta I_{CO} \longrightarrow (2)$$

Sub eqn(1) in eqn(2)

$$I_C = \beta(I - I_0) + \beta I_{CO}$$

$$= \beta I - \beta I_0 + \beta I_{CO}$$

$$= \beta I + \beta(I_{CO} - I_0) \rightarrow (3)$$

In eqn(3), I_{CO} reverse Saturation current of collector jun I_0 is the reverse Saturation current of diode. If the diode and BJT are constructed with same material with same dopping

I_{CO} and I_O are Same

$$\therefore \quad I_C = \beta I_B + \beta (I_{CO} - I_O)$$

$$I_C = \beta I_B \longrightarrow (4)$$

According to defination of Stability factor $S = \frac{\partial I_C}{\partial I_{CO}}$

hence $\frac{\partial I_C}{\partial I_{CO}} = 0$ beeause equation (4) not depends on I_{CO}.

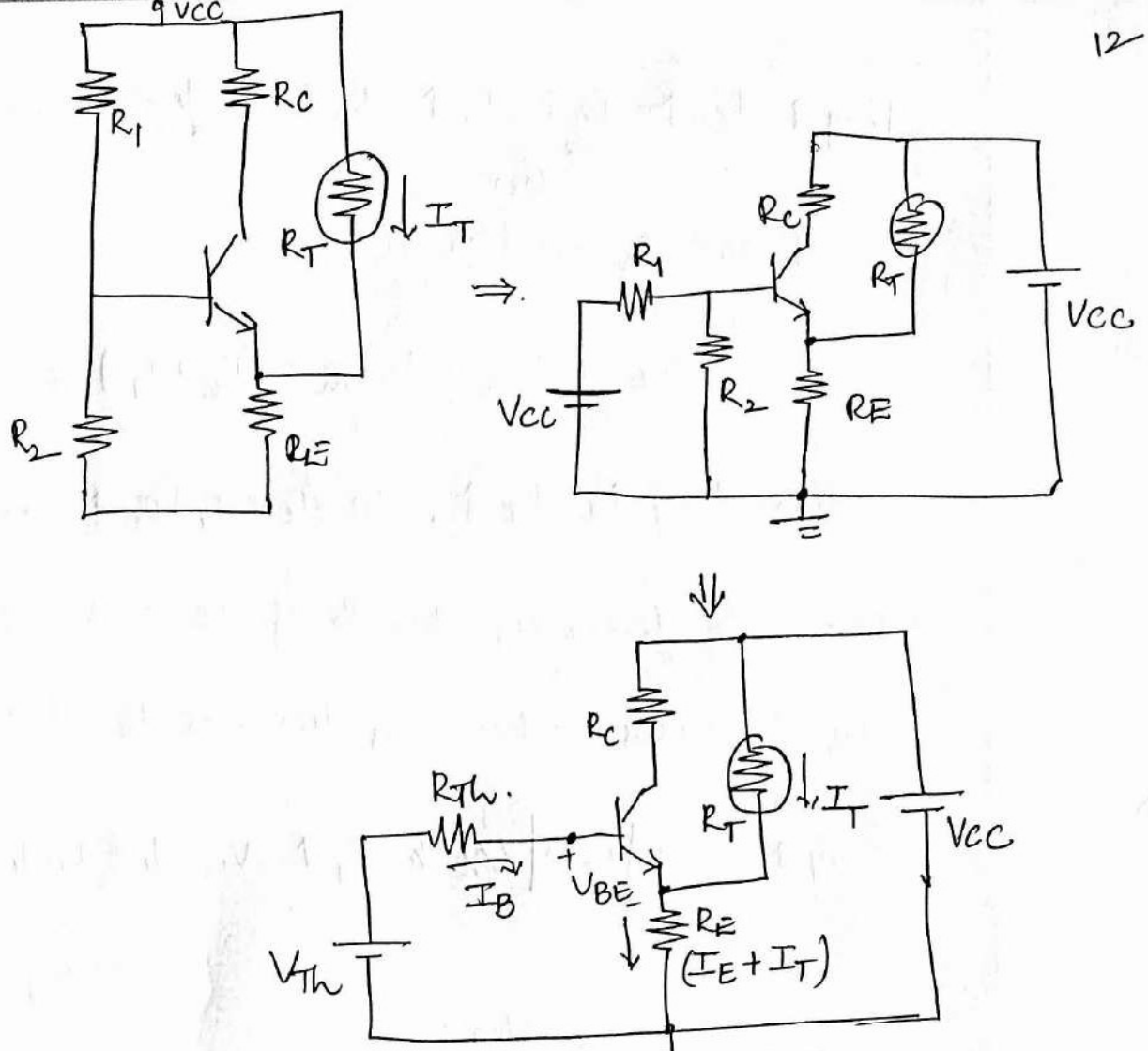
So we can make Change in I_C independ of Change in I_{CO} hence Stability of the device is Very high.

ii) Thermistor Compensation Techniques:-

Thermistor is a temperature Sensitive element having negative temperature co-effecient of resistance decreas exponentially with increase of temperature T.

The Circuit of Fig gives a Selfbiased CE amplifier with thermistor R_T Connected from V_{CC} supply to the emitter terminal. Thermistor R_T uses to minimize the increase in collector current due to Changes in I_{CO}.

In below Fig, I_T indicates Thermistor Current. R_T indicates Thermistor.



Fig(8): Thermistor compensation technique.

input KVL is

$$-V_{Th} + I_B R_{Th} + V_{BE} + (I_E + I_T) R_E = 0.$$

where $I_E = I_B + I_C$

$$-V_{Th} + I_B R_{Th} + V_{BE} + (I_B + I_C + I_T) R_E = 0$$

$$\therefore I_B = \frac{V_{Th} - V_{BE} - (I_C + I_T) R_E}{R_{Th} + R_E} \longrightarrow (1)$$

When Temp ↑, Resistance of thermistor R_T decreases (R_T↓), Thermistor Current (I_T ↑), Voltage drop across R_E i.e $(I_C + I_T) R_E$ ↑ hence I_B will decreases.

When I_B decreases I_C also decreases.

Temp ↑ I_{CO} ↑ I_C ↑ I_T ↑ I_B ↓ I_C ↓ $\therefore I_C = \beta I_B$

(or)

From V_B equation (1)

$$V_{BE} = V_{Th} - I_B R_{Th} - (I_E + I_T) R_E \longrightarrow (2)$$

When Temp ↑, I_T ↑, so $(I_E + I_T) R_E$ ↑ $\therefore V_{BE}$ ↓

When V_{BE} decreases, Strength of Forward bias decreases

So I_B decreases, when I_B decreases I_C also decreases.

Temp ↑ I_{CO} ↑ I_C ↑ V_{BE} ↓ I_T ↑ V_{BE} ↓ I_B ↓ I_C ↓

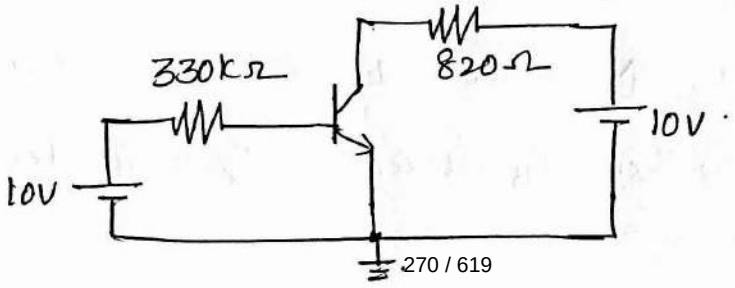
$\because I_C = \beta I_B$

Problems

1. In CE configuration $V_{CC} = 10V$, $R_C = 8k\Omega$. Draw the DC load line determine the operating point for zero Signal. If $I_B = 50\mu A$ and β is 40.

2. In transistor circuit $R_L = 5k\Omega$ and $I_{CQ} = 1.2mA$, determine the operating point when battery Voltage = 12V. How will Q-point Changes when the load resistance is changed from $5k\Omega$ to $7.5k\Omega$.

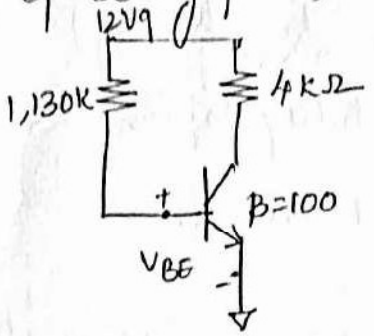
3. What is the Base current in given Fig



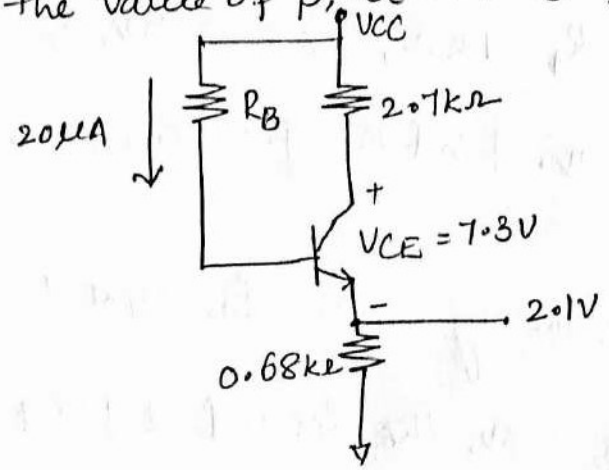
4. Temperature Changes from 30°C to 60°C producing Change in I_C from 2.2mA to 3.8mA. Assume reverse Saturation current Changes 1.7μA/°C. What is the Stability factor.

5. In fixed biasing Circuit $R_B = 1M\Omega$, $R_C = 5k\Omega$, $V_{CC} = 6V$ and $\beta = 100$ determine Q-point.

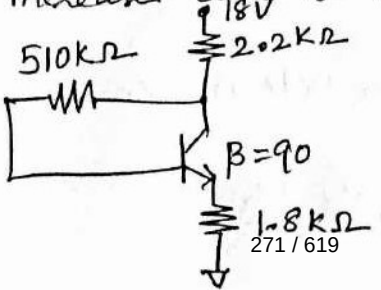
6. For given figure shows the circuit of fixed bias using Silicon transistor with $\beta = 100$. Determine I_B, I_C, V_C, V_B and V_{CB}, operating point, Stability factor.



7. Find the Value of β, V_{CC} and R_B of following Circuit.



8. Find I_C and V_{CE} for following Circuit. What will happen to V_{CE} if β increases due to temperature.



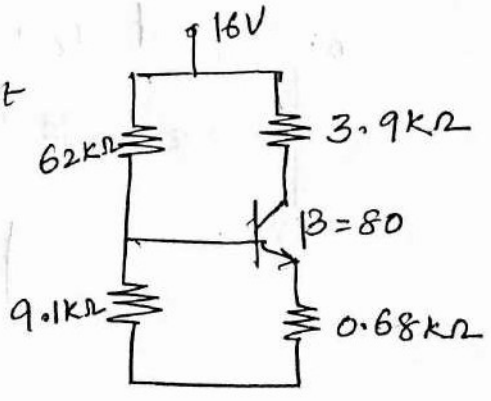
9. CE amplifier employing npn transistor as load resistence R_C connected between collector and V_{CC} supply of 16V for biasing a resistor R_1 is connected b/w collector and base and resistance $R_2 = 10k\Omega$ is connected b/w base and ground. Draw the circuit. Calculate the values of R_1, R_C and S. If $V_{BE} = 0.2V$, $I_E = 2mA$, $\alpha = 0.985$ and $V_{CE} = 6V$.

10. Assume that Silicon transistor with $\beta = 50$, $V_{BE} = 0.6V$, $V_{CC} = 20V$ and $R_C = 4.7K\Omega$ is used in Self biased circuit. It is designed to establish Q-point at $V_{CE} = 8V$ and $I_C = 2mA$ and Stability factor $S \leq 5$. Design the circuit with all component values.

11. In a Self biasing CE configuration amplifier circuit $R_2 = 90k\Omega$, $R_1 = 1K\Omega$, $V_{CC} = 22.5V$, $R_C = 5.6k\Omega$, $R_E = 1K\Omega$, $\beta = 55$, $V_{BE} = 0V$. Find the operating point and Stability factor

12. Design Self biasing Circuit for NPN transistor having $h_{fe} = 100$, $V_{BE} = 0.6V$, the desired Q point is $V_{CEQ} = 5V$, $I_{CQ} = 1mA$ and $S \leq 8$. Assume $V_{CC} = 10V$ and $R_E = 1K\Omega$.

13. For the voltage divider bias circuit in a given figure. Determine I_{CQ}, I_{BQ}, V_{CEQ}, V_C, V_E, V_B.



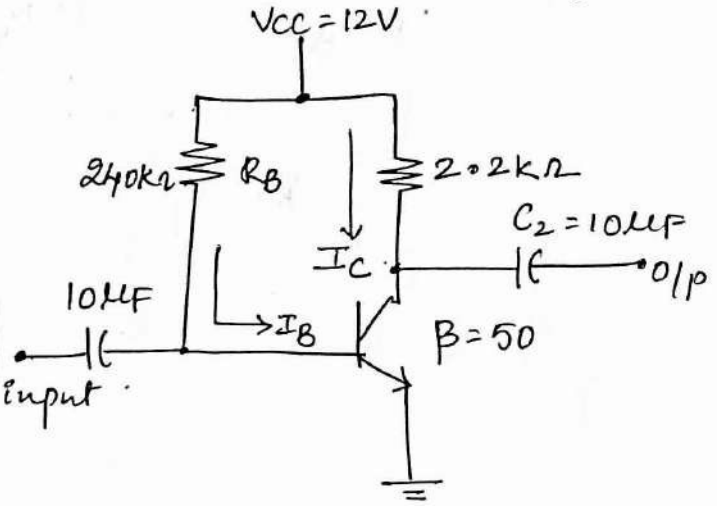
14. Determine the following for the fixed-bias configuration shown in below Fig

i) I_{BQ} and I_{CQ}

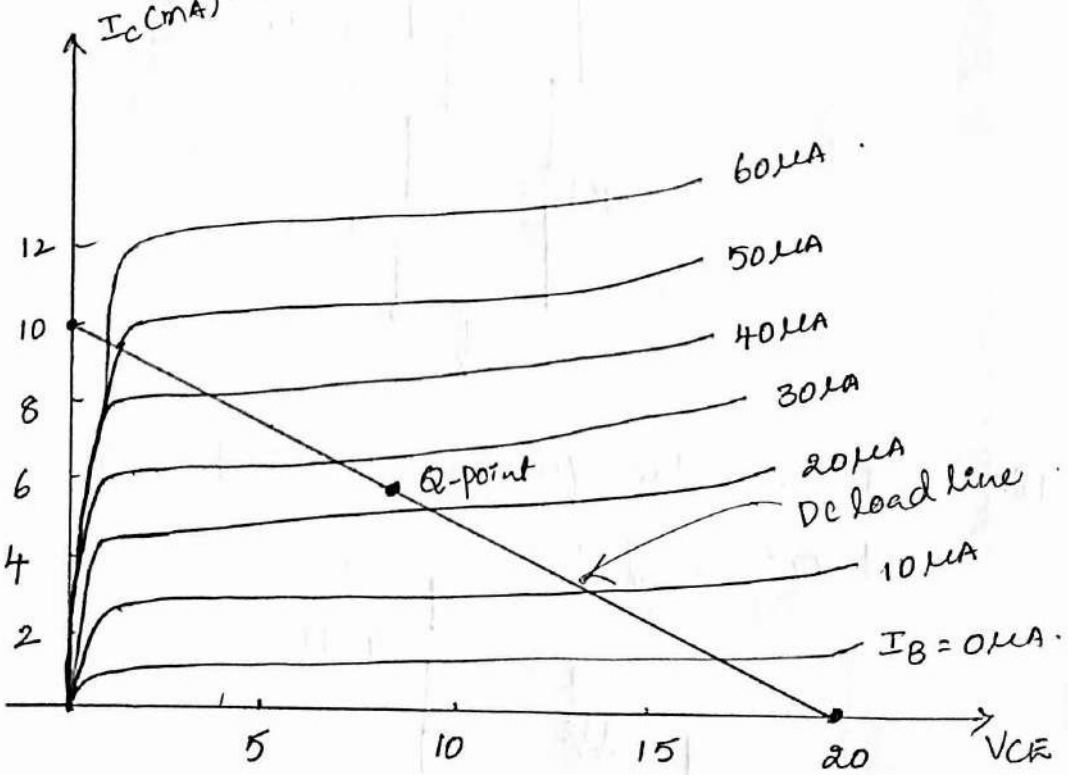
ii) V_{CEQ}

iii) V_B and V_C

iv) V_{BC}.

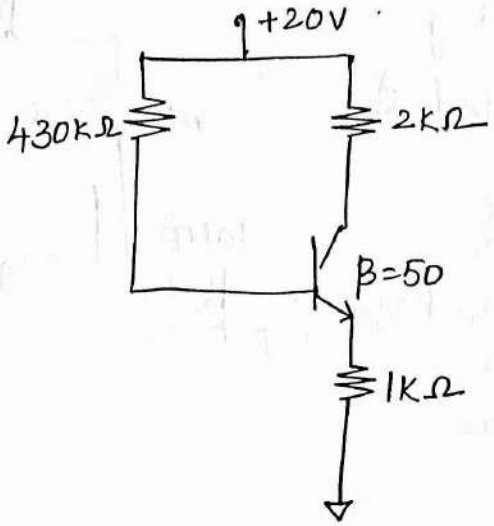


15. Given the load line of below Fig and the defined Q-point determine the required values of V_{CC}, R_C and R_B for a fixed bias configuration.



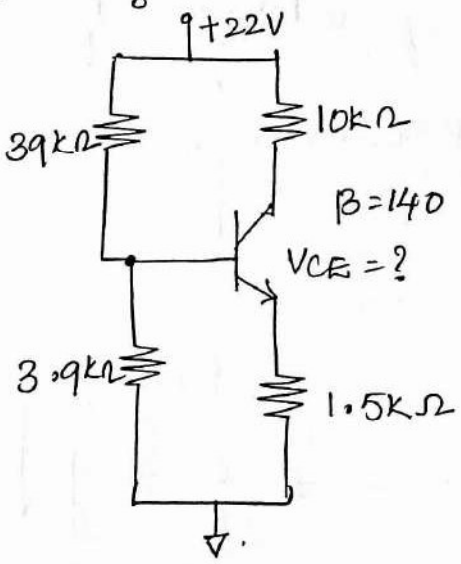
16. For the emitter bias Circuit as shown in below Fig. Determines

a) I_B b) I_C c) V_{CE} d) V_C e) V_E f) V_B g) V_{BC}.

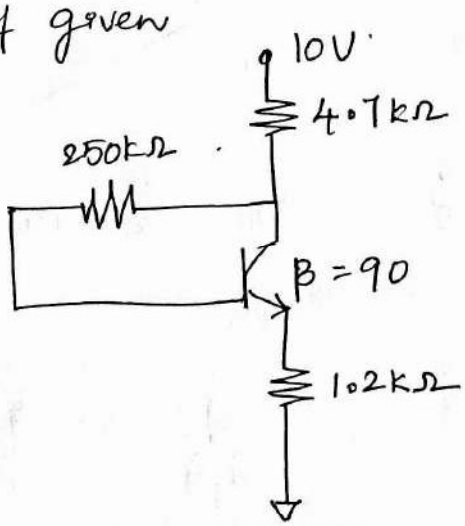


17. For the voltage divider configuration of Fig. Determine the

i) dc bias voltage V_{CE} and ii) the current I_C.



18. Determine the quiescent levels of I_{CQ} and V_{CEQ} for the network of given



Field Effect Transistor (FET)

The field effect transistor is a semiconductor device which operation is depends on electricfield i.e current flowing in the device is controlled by electric field.

There are two types of Field effect Transistor

1) Junction Field Effect Transistor (JFET)
   a) N-Channel JFET b) P-Channel JFET.

2) Metal Oxide Semiconductor field effect Transistor (MOSFET)
   (or)
   Insulated-Gate Field effect Transistor (IGFET)

a) n Channel MOSFET (nMos)
   - Enhancement Mode
   - Depletion Mode

b) p Channel MOSFET (pMos)
   - Enhancement Mode
   - Depletion Mode

The Junction field effect Transistor :-

The Structure of an n-Channel field effect transistor is shown in below Fig(1). Ohmic Contacts are made to the two ends of a Semiconductor bar of n-type material. Current is caused to flow along the length of the bar because of the voltage supply connected between the ends. Here current is due to majority carriers: In case of n-channel JFET, current due to electrons and in case of p-channel JFET current due to holes.

Source :-

The Source is the terminal through which the majority Carriers enter the Bar.

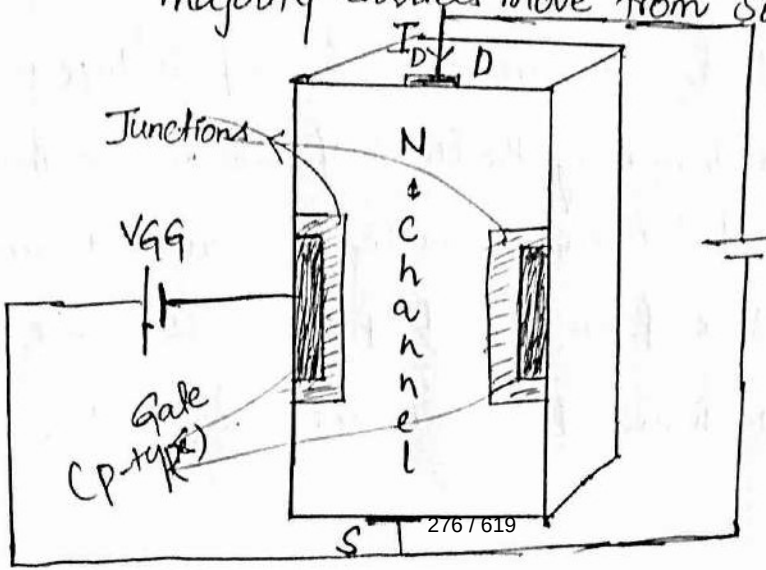
Drain :-

The Drain is the terminal through which the majority Carriers leave the Bar. Conventional Current entering the bar at D is designated by I_D. The drain to Source voltage is called V_{DS}, and is positive if D is more positive than Source. In Fig, V_{DD} is Drain Supply voltage.

Gate :-

on both Sides of the n-type bar, heavily doped p-type impurities have been inserted by alloying (or) by diffusion (or) by any other procedures available for Creating p-n junctions. These impurities regionsare called the Gate 'G'. Between the gates and Source voltage $V_{GS} = -V_{GG}$ is applied in the direction to reverse bias the p-n junction, Conventional current entering the bar at G is designated I_G. Two Gate terminals are internaly connected.

Channel :- The region in Fig of n-type material between the two gate regions is the Channel through which the majority Carriers move from Source to Drain.



Fig(1): Physical Structure of N-Channel JFET.

In above Fig, if $V_{GG}=5V$ and junction width is uniformly increases because zero potential is there through out the Channel ($\because V_{DS}=0$). Reverse bias is same from Source to Drain because at any position in the Channel region potential difference is same as shown in Fig(2). So junction width is uniform throughout the Channel.

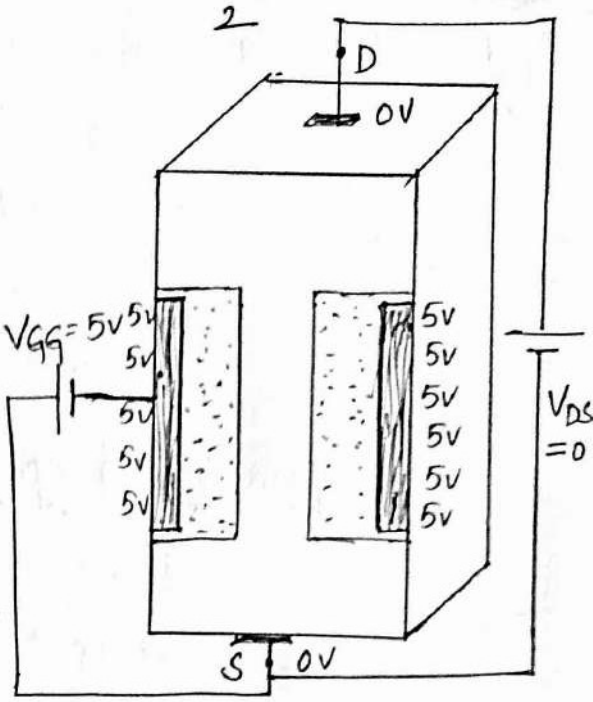


Fig 2: When $V_{GG}=-5V$ and $V_{DS}=0V$.

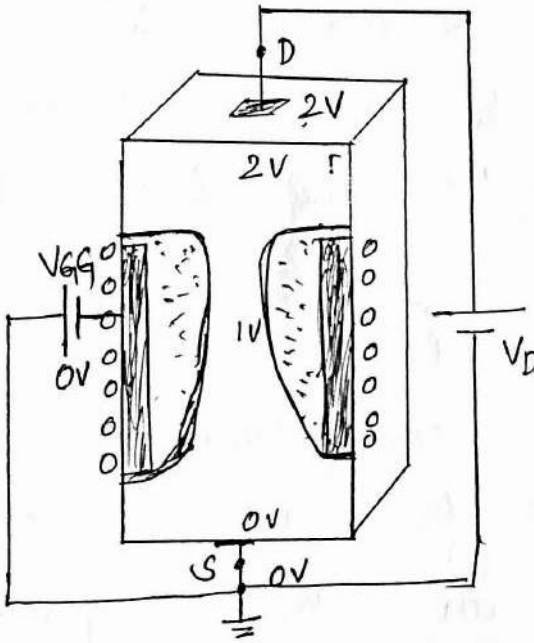


Fig 3: $V_{GG}=0$ and V_{DS} is Constant.

When V_{GG} is equal to zero (or) Constant and V_{DS} is applied (if $V_{DS}=5V$) junction width is formed as shown in Fig(3). When $V_{DS}=2V$ when $V_{DS}=2V$ at Drain end of the Channel is having "2V" and Source end of channel is having "0V". When $V_{GG}=0V$ potential difference near to drain end is 2V and potential difference near to Source end is 0V. So Reverse bias is max near to drain and reverse bias is min near to Source. So Junction width is maximum at Drain end and min at Source end as shown in Fig 3.

Note:-

* When $V_{DS}=0V$ & V_{GG} is Constant throughout the Channel depletion region (or) junction is uniformly formed as shown in Fig(2).

* When V_{DS} = Constant potential (i.e not zero) and V_{GG} either zero or Constant, depletion region (Junction) is "now uniformly" formed. Near to Drain region depletion region is maximum and near to Source region depletion region is min as shown in Fig 3.

Principle of Operation :-

For understanding the physical operation of n-Channel JFET, Let us Consider Fig (a) where a positive Voltage V_{DS} has been applied across the Channel and both the gate terminals are combined to directly Connect with Source to establish the Condition $V_{GS}=0$

The application of V_{DS} Causes electrons to move from Source to Drain terminal establishing the Conventional Current I_D to flow from the Drain to Source.

When $V_{GS}=0$ and V_{DS} is varied

First consider Smaller V_{DS} values, resistance of Channel is almost Constant because resistance $R = \frac{\rho l}{A} \rightarrow (1)$.

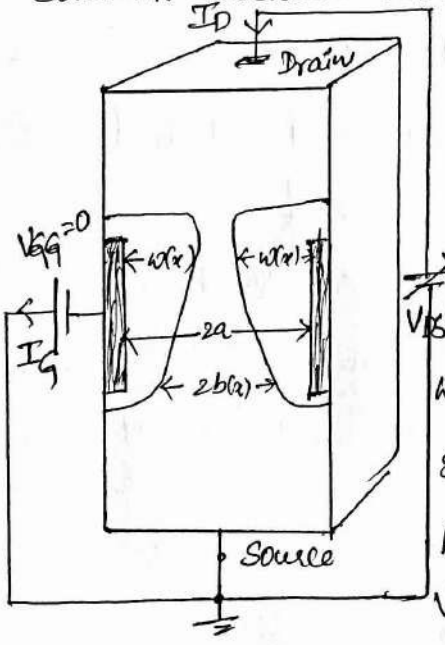


Fig (a).

In eqn(1) ρ is the resistivity and L is the length of the physical Substrate. Where A is Cross sectional area i.e $A = 2b(x) \cdot W$ Where "2b(x)" is Channel width and W is the width of Substrate. ~~Where "A" is the Cross sectional area is~~

For Smaller Voltages, Change in 2b(x) is Very small. So we treated as 2b(x) i.e Change in Channel width is almost Constant. So 'A' is Constant.

In eqn(1) ρ and L are constants and for smaller potential of V_{DS}, 'A' is also almost constant so resistance 'R' is constant.

$$So \quad V_{DS} = I_{DS} \cdot R$$

Here resistance is almost constant for smaller potential V_{DS}. So current I_D is almost linearly varies with respect to voltage V_{DS}.

For largest V_{DS}, resistance of Channel increases.

$$R = \frac{\rho l}{A}$$

In above equation ρ, l are constants

$$A = 2b(x) \cdot W$$

In above eqn W is also constant, $2b(x)$ is Channel width that is varies with respect to V_{DS}. When V_{DS} increases, Channel width $2b(x)$ is decreases, so area A is decreases. When area A decreases, Resistance R will increases $\because R \propto \frac{1}{A}$

$$\therefore \quad V_{DS} = I_{DS} \cdot R$$

$$I_{DS} = \frac{V_{DS}}{R}$$

In above equation, when V_{DS} increases, Resistance is also increases hence I_{DS} is constant.

Pinchoff Voltage V_p :-

It is the minimum drain-to source voltage at which the drain current essentialy becomes constant. At that voltage Channel width is nearly zero.

When V_{GG} increases, $2b(x)$ is further decreases because

V_{GG} effect also taken place on junction width. So at Smaller Values of V_{DS} we will getting $2b(x)$ is almost zero from that Voltage onwards current is Constant.

Output (or) Static (or) Drain Characteristics of JFET :-

The curve between drain current I_D and drain - Source voltage V_{DS} of a JFET at Constant gate - Source voltage V_{GS} is known as output Characteristics (or) Drain Characteristics of JFET.

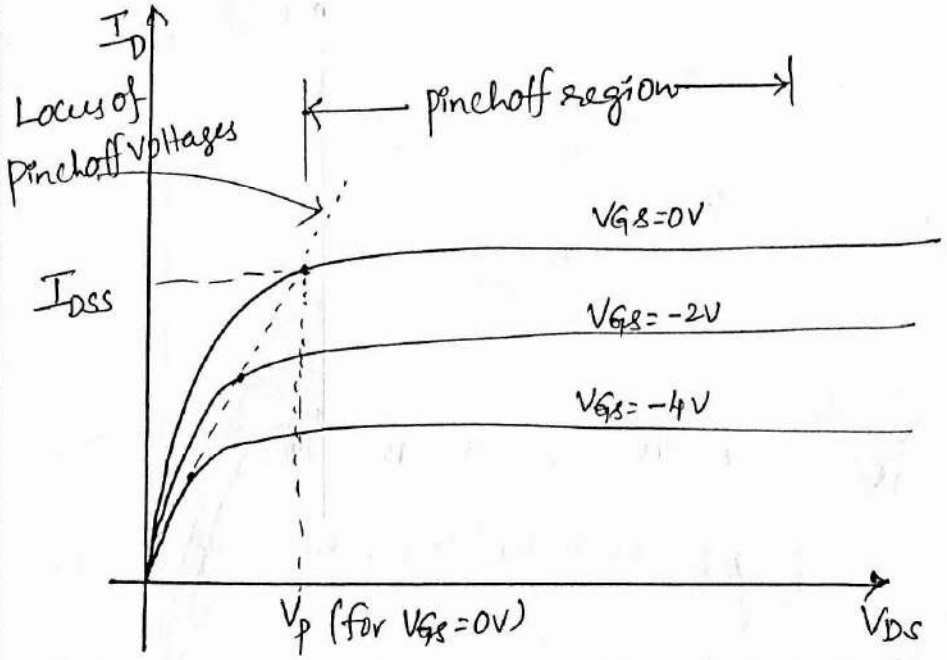
When $V_{GS} = 0$

i) at Smaller Voltages of V_{DS}, the Drain Current I_D is linearly rises with drain Source Voltage V_{DS}, because resistance offered by the Channel is Constant. ($\because V_{DS} = I_D \cdot R$; $I_D = \frac{V_{DS}}{R}$ there resistance is Constant So V_{DS} increases, I_D also increases)

ii) After Smaller Voltages of V_{DS}, the drain Current I_D is Constant with increase in drain - Source Voltage V_{DS}, because resistance offered by the Channel is increases [$\because V_{DS} = I_D \cdot R$; $I_D = \frac{V_{DS}\uparrow}{R\uparrow}$ here V_{DS} increases resistance is also increases So I_D is Constant].

Drain to Source Voltage V_{DS} above which drain Current becomes Constant is known as "pinch off Voltage".

After pinch off voltage the Channel width becomes So narrow, i.e depletion layers almost touch eachother, hence the drain current passes through the Small passage between these layers. Therefore increase in drain Current is very Small with V_{DS} above pinchoff Voltage



Where I_{DSS} is Drain to Source Saturation Current
V_p is the pinchoff Voltage.

Fig: output (or) Static Characteristics of JFET.

Transfer Characteristics:-

The transfer characteristics of JFET is a plot of output current i.e Drain current Vs input Controlling quantity i.e gate Source Voltage and Keeping V_{DS} equal to pinchoff voltage.

When V_{GS} increases, Channel width $2b(x)$ decreases, so resistance increases, when resistance increase current I_D in the Channel is decreases.

From Shockley equation

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

From above equation, when V_{GS} increases I_D is decreases. When $V_{GS}=V_p$, $I_D=0$ but exactly not equal to zero i.e in orders of nA so we treated as approximately equal to zero.

When $V_{GS}=0$, we are getting maximum current i.e I_{DSS} (Drain to Source Saturation current) as shown in below Fig.

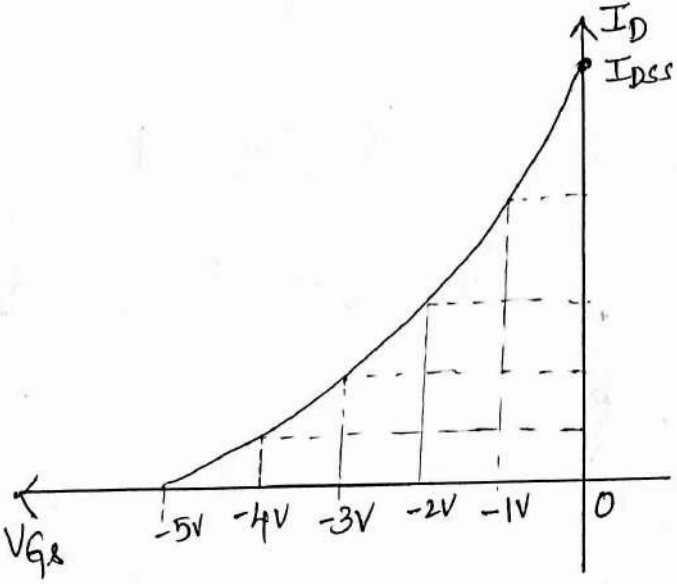
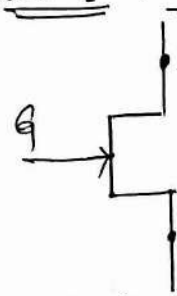


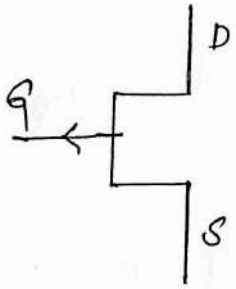
Fig: Transfer Characteristics of JFET.

Symbol of N Channel JFET



Arrow indicates current direction when Gate is forward bias

Symbol of P Channel JFET



Arrow indicates current direction when Gate is forward bias.

Pinchoff Voltage V_p :-

Junction width $W(x) = a - b(x)$

We know the relation between Junction width and reverse voltage as shown in below

$$W(x) = \left[\frac{2\epsilon}{qN_D} V(x)\right]^{1/2}$$

Where $V(x)$ is the reverse voltage

N_D Diffusion Constant

ϵ permitivity

q Charge of the particle.

at $V(x)$ = pinchoff voltage $b(x) \simeq 0$

$$W(x) = a - b(x) = \left[\frac{2\epsilon}{qN_D} V(x)\right]^{1/2}$$

at $V(x) = V_p$, $b(x) = 0$

$$a - 0 = \left[\frac{2\epsilon}{qN_D} V_p\right]^{1/2}$$

$$a = \left[\frac{2\epsilon}{qN_D} V_p\right]^{1/2}$$

Square on both sides

$$a^2 = \frac{2\epsilon}{qN_D} V_p$$

$\therefore$ pinchoff voltage $\boxed{V_p = \frac{qN_D}{2\epsilon} \cdot a^2}$

at particular $V(x) = V_{GS}$ $b(x) = b$

$$a - b = \left[\frac{2\epsilon}{qN_D} V_{GS}\right]^{1/2}$$

$$(a-b)^2 = \frac{2\epsilon}{qN_D} V_{GS}$$

$$V_{GS} = \frac{qN_D}{2\epsilon} (a-b)^2$$

$$V_{GS} = \frac{qN_D}{2\epsilon} a^2 \left(1 - \frac{b}{a}\right)^2$$

where $V_p = \frac{qN_D}{2\epsilon} a^2$

$\therefore$ $V_{GS} = V_p \left(1 - \frac{b}{a}\right)^2 \longrightarrow$ eqn(1)

$$\frac{V_{GS}}{V_p} = \left(1 - \frac{b}{a}\right)^2$$

apply root on both sides

$$\left(\frac{V_{GS}}{V_p}\right)^{1/2} = 1 - \frac{b}{a}$$

$$\frac{b}{a} = 1 - \left(\frac{V_{GS}}{V_p}\right)^{1/2}$$

∴ Half Channel width $= \boxed{b = a\left[1 - \left(\frac{V_{GS}}{V_p}\right)^{1/2}\right]}$

where a is Half distance between the two depletion regions.

Relation between I_{DS} and V_{GS} is given by Shockely equation

$$\boxed{I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$

JFET parameters:-

Drain resistance:-

Current density $J = nq\vartheta \longrightarrow (1)$

Where n is Concentration of Charge carriers

q is Charge of the particle

ϑ is drift velocity.

Drift Velocity $\vartheta \propto$ Electric field E

$$\vartheta = \mu E \longrightarrow (2)$$

Where μ is the mobility of Charged particle

Sub eqn(2) in eqn(1)

$$\therefore J = nq\mu E \longrightarrow (3)$$

By the definition current density $J = \frac{\text{Current (I)}}{\text{Area (A)}}$

Hence eqn(3) becomes

$$\frac{I}{A} = nq\mu E$$

$$\frac{I}{A} = nq\mu \cdot \frac{V_{DS}}{L}$$

$$I_{DS} = \frac{nq\mu A V_{DS}}{L} \longrightarrow (4)$$

where L is the length of the channel

V_{DS} is the Drain to Source voltage

A is crosssectional area i.e $2b(x) \cdot W$

$\therefore$ eqn(4) becomes

$$I_{DS} = \frac{nq\mu 2b(x) W V_{DS}}{L} \longrightarrow (5)$$

By the definition $\frac{V_{DS}}{I_{DS}}$ is resistance of the Channel

(or Drain resistance

$$r_d = \frac{V_{DS}}{I_{DS}} = \frac{L}{nq\mu 2b(x) \cdot W} \longrightarrow (6)$$

n is the Concentration of Charge carriers

in n-Channel JFET 'n' is replaced by N_D.

$\therefore$ Drain resistance $r_d = \dfrac{L}{N_D q \mu 2b(x) \cdot W}$

at particular constant V_{GS} $b(x) = b$

$$r_d = \frac{V_{DS}}{I_{DS}} = \frac{L}{N_D q \mu 2b \cdot W}$$

where $b = a\left[1 - \left\{\frac{V_{GS}}{V_P}\right\}^{1/2}\right]$

$$\therefore r_d = \frac{L}{2N_D q \mu a \left[1 - \left\{\frac{V_{GS}}{V_P}\right\}^{1/2}\right] W} \longrightarrow (1)$$

when $V_{GS} = 0$

$r_{d(ON)} = \dfrac{L}{2N_D q \mu a W}$ is called as Drain ON resistance and denoted as $r_{d(ON)}$.

$\therefore$ Drain resistance $\boxed{r_d = \dfrac{r_{d(ON)}}{\left[1 - \left\{\frac{V_{GS}}{V_P}\right\}^{1/2}\right]}}$

when $V_{GS} = V_P$ in equ (1).

$\underline{\underline{r_d = \infty}}$

Trance Conductance g_m :-

Shockly equation is given by $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ ⟶ (1)

equation (1) is differentiate w.r.t V_{GS}

$$\frac{\partial I_{DS}}{\partial V_{GS}} = 2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)\left(\frac{-1}{V_P}\right)$$

Trance conductance $g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$ ⟶ (2)

When $V_{GS} = 0$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2I_{DSS}}{V_P}$$

Let $\frac{-2I_{DSS}}{V_P}$ as g_{mo}, so $g_{mo} = \frac{-2I_{DSS}}{V_P}$

∴ Trance conductance $\boxed{g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)}$

When $V_{GS} = V_P$

Trance conductance $g_m = g_{mo}\left(1 - \frac{V_P}{V_P}\right)$

$$g_m = g_{mo}(1-1)$$

$$g_m = 0$$

Amplification factor μ :-

Amplification factor μ = $\frac{\text{Change in } V_{DS}}{\text{Change in } V_{GS}}$

i.e $\mu = \frac{\partial V_{DS}}{\partial V_{GS}}$

$= \frac{\partial V_{DS}}{\partial I_{DS}} \times \frac{\partial I_{DS}}{\partial V_{GS}}$

Amplification factor = $\mu = r_d \times g_m$

Where r_d is Drain resistance

g_m is Transconductance.

Important factor of JFET :-

1) JFET is "unipolar device" because current is due to majority charge carries (due to electrons in n-Channel JFET and due to holes in p- Channel JFET)

2) JFET is Bilateral

3) JFET is Voltage Control device i.e output current I_D depends on V_{GS} and V_{DS}. So I_{DS} is function of V_{GS} and V_{DS}. $I_{DS} = f(V_{GS}, V_{DS})$.

4) In pinchoff region it act as "Voltage Controlled Current Source".

5) Input resistance of JFET is maximum because i/p is reverse bias.

Metal oxide Semiconductor Field Effect Transistor (MOSFET):-

MOSFETs are divided into two types

1) Enhancement mode MOSFET

2) Depletion mode MOSFET

Enhancement MOSFET:-

Enhancement MOSFET also divided into two types. 1) N-Channel enhancement MOSFET

2) p-Channel enhancement MOSFET.

Enhancement MOSFET is operated in enhancement mode only i.e current is increases w.r.t Voltage.

physical Structure of Enhancement MOSFET:-

(N-Channel Enhancement MOSFET)

The Transistor is fabricated on p-type substrate, which is single crystal Silicon wafer that provides physical support for the device. Two heavily dopped n-type regions are created in the substrate to serve as the Source(S) and Drain(D). A thin layer of Silicon dioxide (SiO_2), which is an excellent electrical insulator, is grown on the surface of the Silicon, covering the area between Source and Drain regions. Metal is deposited on top of the oxide layer to form the "gate" Contact of MOSFET. Metal Contacts are also made for Source and Drain.

Substrate is known as Body. The name metal oxide Semi conductor FET is derived from its physical structure. Another name of MOSFET is the Insulated Gate FET (IGFET) The Gate metal is electrically insulated (or seperated) from the device body by the oxide layers. The current in the gate terminal is extremely small ($\simeq 10^{-15}$A). The region b/n Source and drain below the Gate region is known as "Channel".

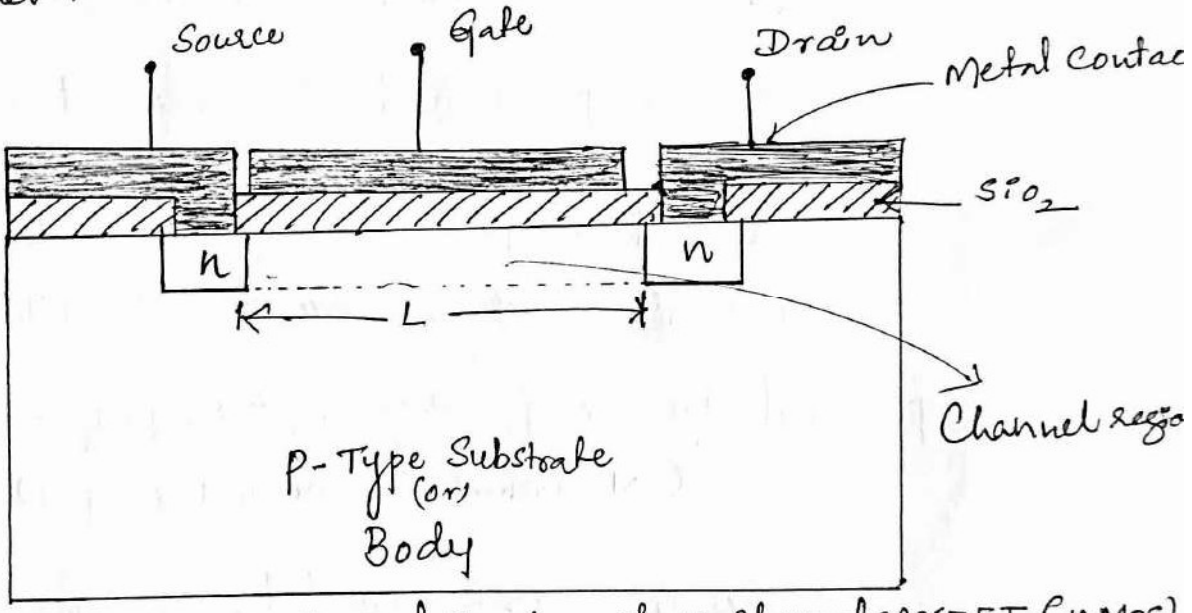


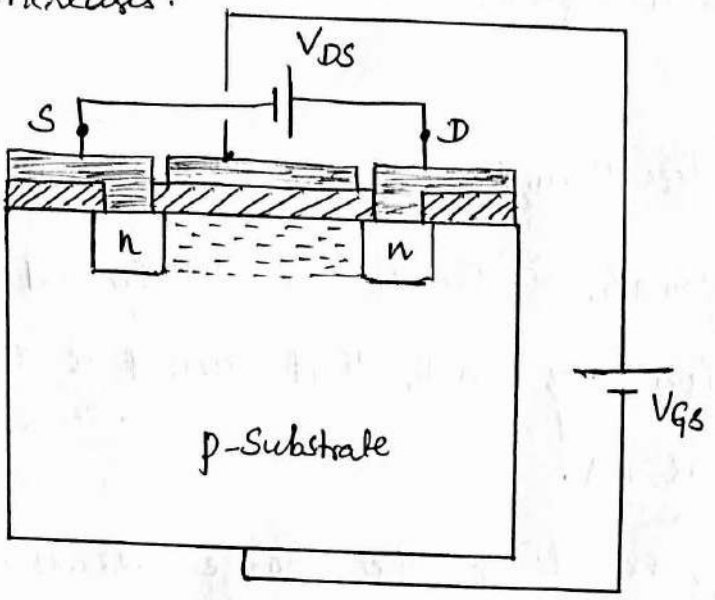
Fig: physical structure of n-Channel MOSFET (nMOS) Enhancement mode

Operation of Enhancement-n-Channel MOSFET:-

Operation of enhancement type MOSFET is given by the below Fig. When Gate is more +ve than p type Substrate:

In p-type Substrate majority carriers are holes and minority carriers are electrons. So holes are repelled by the +ve potential, hence holes are move downwards. Electrons are attracted towards Gate terminals, So negative Charge carriers are fill the region b/n Source and Drain-regions (i.e Channel region)

The negative carriers provides a conduction channel between the source and the Drain. When magnitude of V_{GS} increases carriers in the channel region increases so depth of channel is increases.

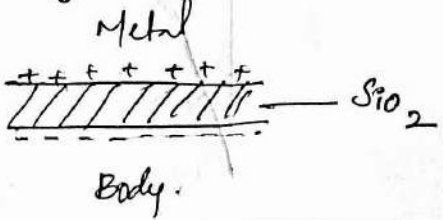


Now if a +ve potential is applied to Drain w.r.t source. Then electrons in the channel region are attracted towards +ve potential (i.e towards drain). Current direction is opposite to electron flow so that current direction is drain to source.

For the MOSFET as shown in above Fig, the induced charge in the channel is n-type carriers, so the device is designated as "n channel MOSFET (nMOS)".

The value of V_{GS} at which a sufficient number of mobile electrons tends to accumulated or (gathering) in the channel region to form a conducting channel is called the "Threshold voltage" and denoted as V_T.

The Gate and the Body of MOSFET form a parallel plate capacitor with oxide layer acting as the capacitor dielectric.



The induced negative charge on the channel region is controlled by V_{GS} (i.e when $V_{GS}\uparrow$ more carriers are gathered in channel region, when V_{GS} is small, less no.of carriers are there in the channel region). So the channel conductivity is controlled by V_{GS}.

As V_{GS} is less than the V_T, the charge carriers in the channel region is very small, so conduction (or) current flow in the channel is also very small, that current is in order of nA so we treated as 0A.

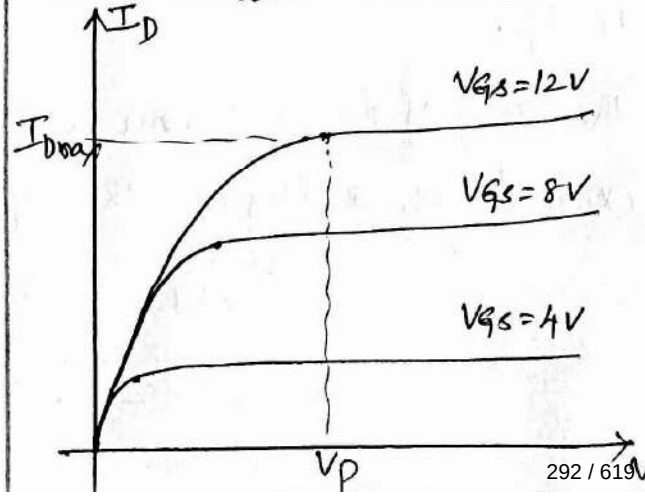
When V_{GS} exceeds V_T, the charge carriers in the channel increases, which in turn increases the channel conduction.

∴ Conduction of channel is proportional to excess gate voltage i.e $(V_{GS}-V_T)$ it is also known as "Effective voltage".

Drain Characteristics :-

Drain characteristics gives the relation between Drain current I_D and Drain to source voltage V_{DS} where keeping V_{GS} is constant.

When $V_{GS} < V_T$, current is very small in order of nA so that current considered as approximately zero.



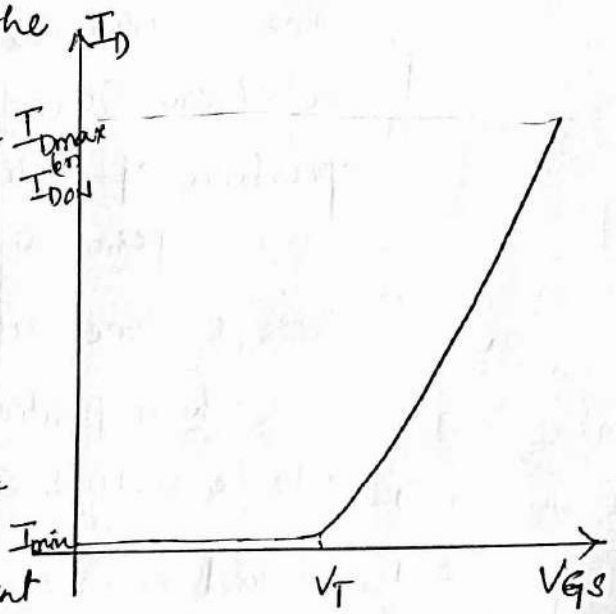
After V_{GS} exceeds V_T, then current in the channel is increases, for smaller values of V_{DS}, current in the channel is directly proportional to V_{DS}. After max current is reached there is no further increase in the current in the channel. So change in the current is almost constant.

Transfer Characteristics :-

This characteristics give the relation between Drain current (I_D) and V_{GS} where V_{DS} is keeping constant.

When $V_{GS} < V_T$, current I_D in the Channel is very small i.e in order of nA so we treated as that current is almost equal to zero.

After $V_{GS} > V_T$, current I_D is propotional to $(V_{GS} - V_T)$ i.e current is linearly increases with increment in V_{GS}.



Normaly V_T is inorder of 1V to 3V depends on the material. Where I_{min} is approximatly zero. Where I_{Dmax} (or) I_{DON} is the max current flowing in the Channel.

Depletion MOSFET :-

The Basic construction of n-Channel depletion-type MOSFET is shown in below Fig.

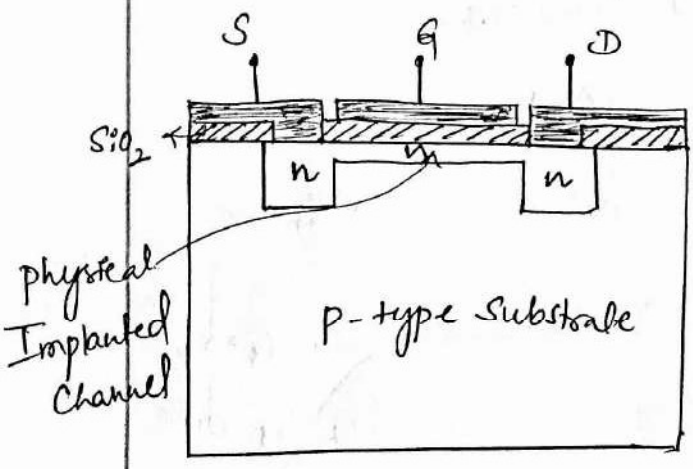


Fig: Depletion N Channel MOSFET.

Its Structure is Similar to that of enhancement type MOSFET with one important difference, the depletion MOSFET has a physical implanted channel in between Source and Drain.

Thus an n channel depletion MOSFET has an n-type Silicon layer connecting the n-source and n-drain regions at the top of the p-type Substrate.

There is no need to induce a Channel, unlike the case of the enhancement MOSFET. Even for $V_{GS}=0$, a current I_D flows if a voltage V_{DS} is applied between drain and source because some carriers are available in physical layer that is connecting in between source and Drain as shown above Fig.

Operation of Depletion MOSFET :-

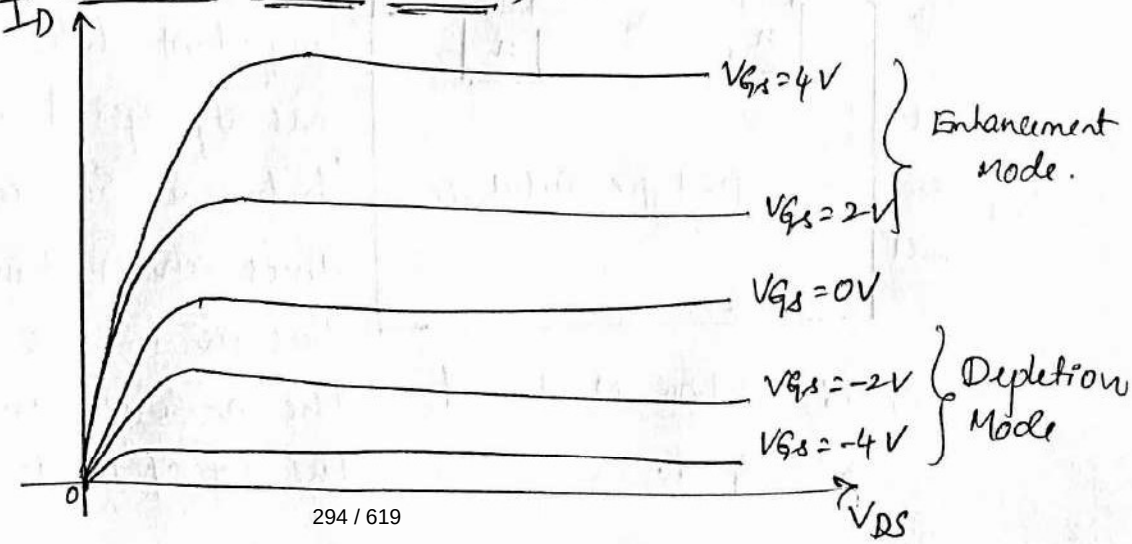
Operation is similar to Enhancement MOSFET. Even $V_{GS}=0V$, there is some current I_D exists in between source and Drain.

When positive Gate voltage is applied, negative charges are induced into the n-type Channel. In this Channel the conductivity of Channel increases and current is rises.

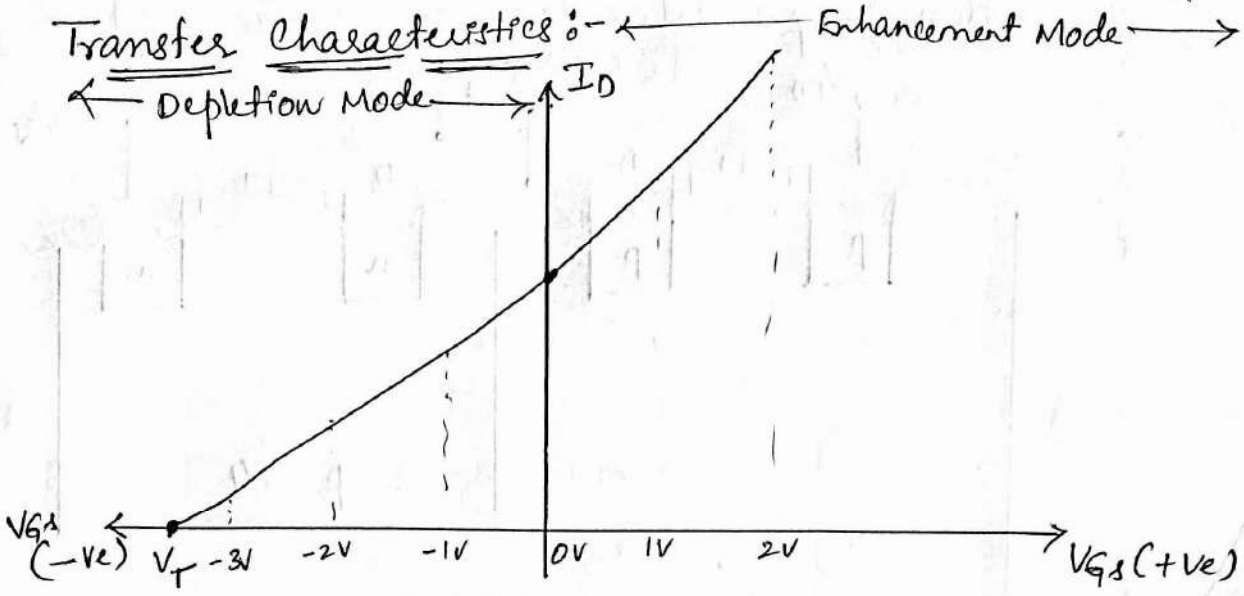
When V_{GS} increases more no. of negative charge particles in Channel region increases, so conductivity of the Channel increases, so current also increases.

When -ve Gate voltage is applied, current I_D is decreased because, when -ve potential is applied to gate, electrons in the implanted n- channel is repelled from -ve potentials, so electrons are move downwards. So carriers in the n- Channel is decreases so current from Drain to source is also decreases.

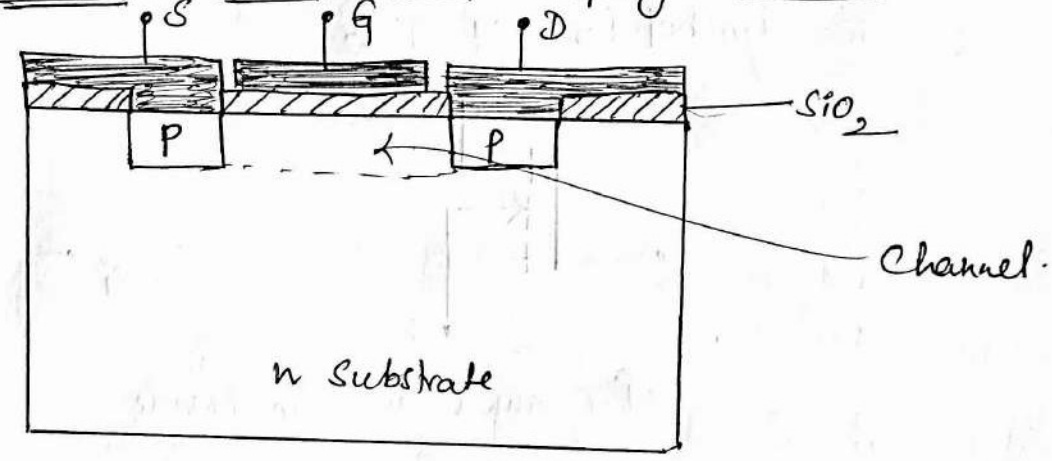
Drain Characteristics (I_D Vs V_{DS}) :-



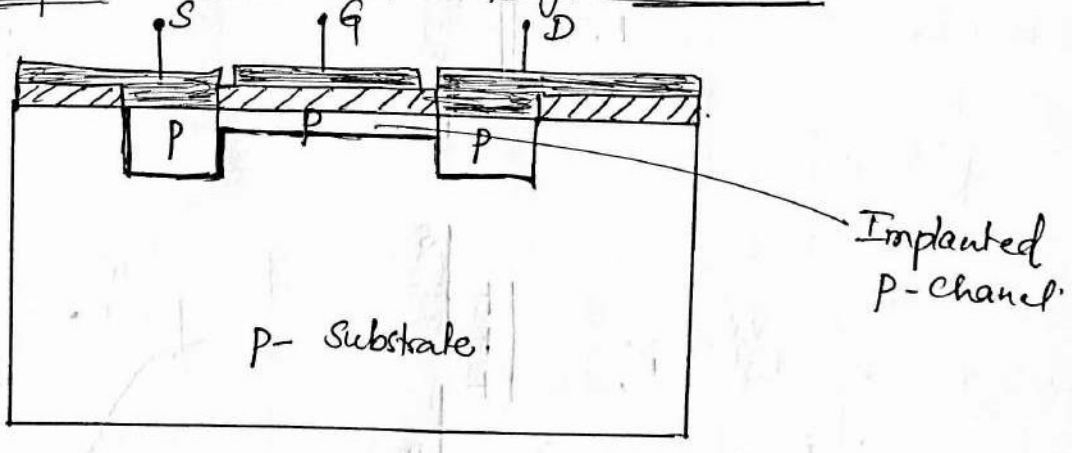
Transfer Characteristics :-



p Channel Enhancement Mode MOSFET physical Structure :-

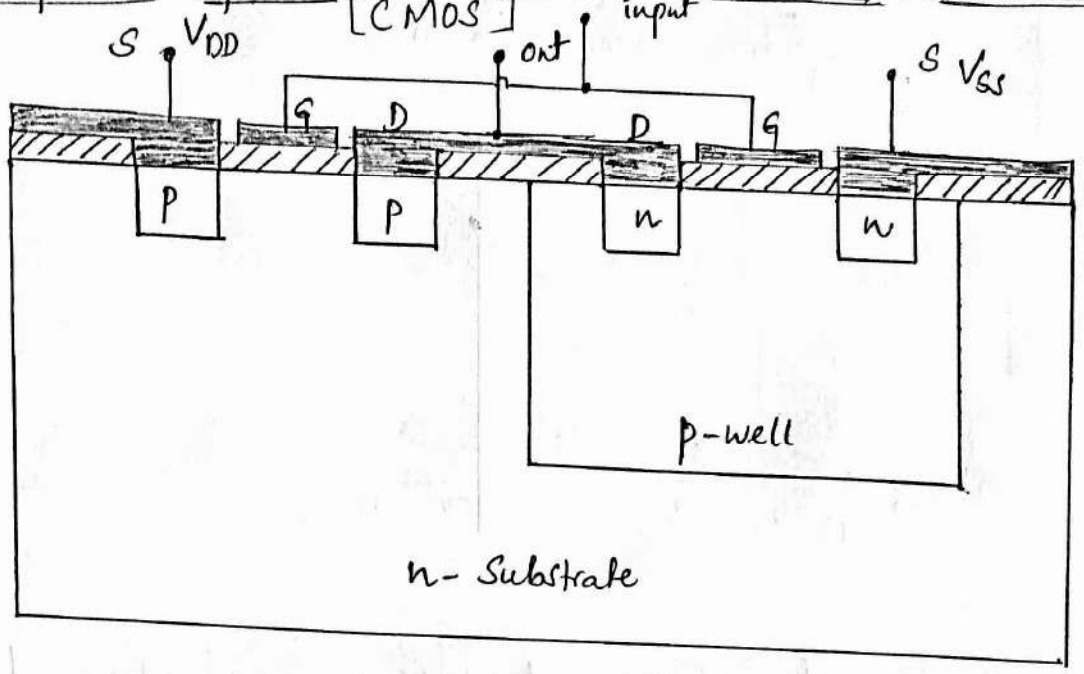


p Channel Depletion Mode MOSFET physical Structure :-

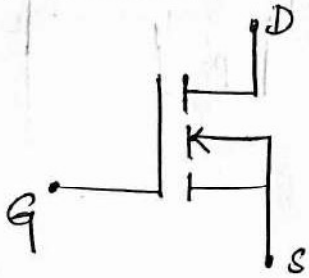


Working principle and operation of p Channel MOSFET (Both Depletion Mode & Enhancement) is Similar to n Channel MOSFET except require Voltage (V_{GS}) is -Ve to form the Channel b/w Source and Drain.

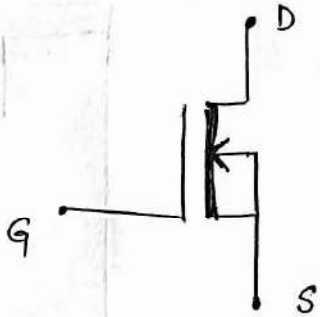
Complementary Metal oxide Semiconductor Field Effect Transistor :- [CMOS]



Symbol for MOSFET :-

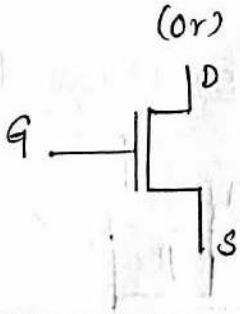


N Channel Enhancement Mode



N Channel Depletion Mode.

(or)



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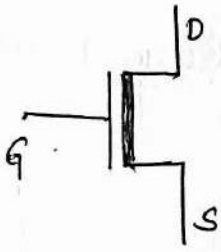

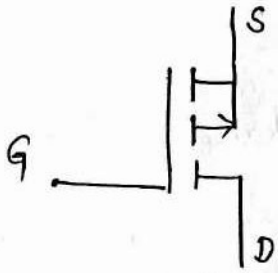

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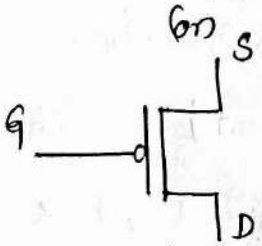
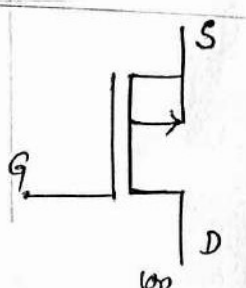
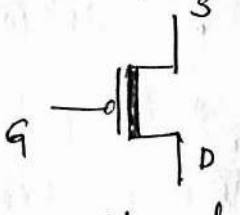


p Channel Enhancement Mode

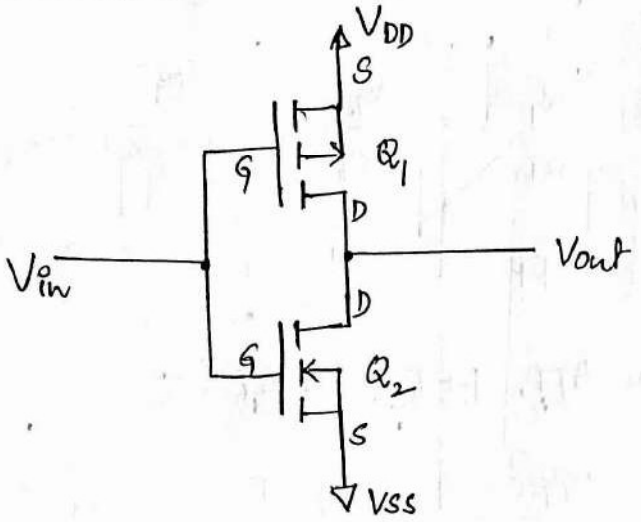


(or)



p Channel Depletion Mode.

CMOS Symbol :-



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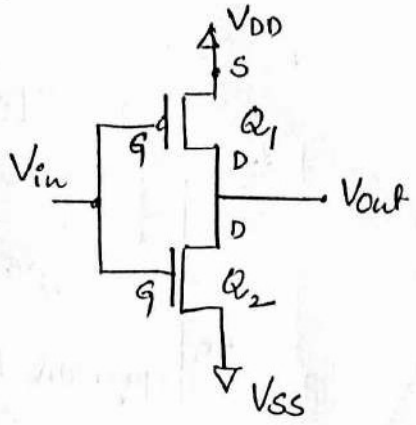
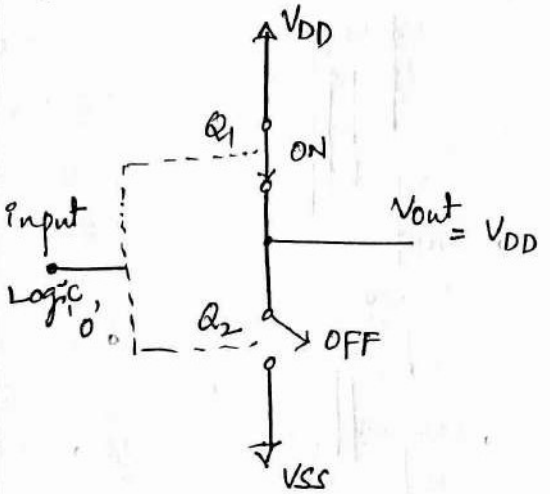


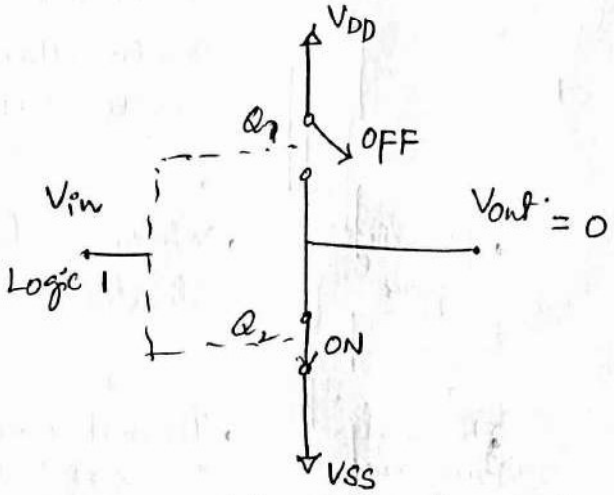
Operation of CMOS :-

When the Low input voltage is given to the CMOS Inverter, then the PMOS transistor is switched ON whereas the NMOS transistor will switch OFF by allowing the flow of electrons through out the gate terminal & generating high Logic output voltage.

When the High input voltage is given to the CMOS Inverter, then the PMOS transistor is switched OFF, whereas the NMOS transistor will switch ON, hence Vout is isolated from supply V_{DD} and Vout discharge through ~~CMOS, CMOS~~ NMOS to ground.



a) operation of CMOS when input is Logic '0'

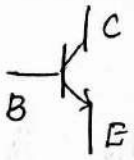
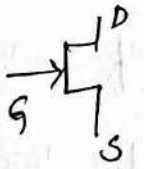
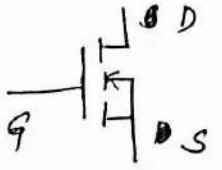


b) When Input is Logic "1"

Summarizes the operation of CMOS inverter :-

Input	Q_1	Q_2	Output
Logic 0	ON	OFF	Logic 1 (V_{DD})
Logic 1	OFF	ON	Logic 0 (0V)

**Comparison between BJT, JFET, MOSFET :-

Parameters	BJT	JFET	MOSFET
• Symbol			
• Definition	• BJT is known as Bipolar Junction device because it uses both electrons and holes for conduction	• JFET is known as unipolar device because current due to one charge carrier i.e electrons or holes	• MOSFET is known as unipolar device because current is due to one charge carriers depending on type of MOS
• Input Resistance	• BJT offers Low input resistance	• JFET offers large input resistance order of 1MΩ to 5MΩ	• MOSFET offers very large input resistance.
• Biasing used	• Fixed Bias, Collector-to Base Bias, Self Bias or Voltage divider Bias	• Self Bias (or) Voltage divider Bias	• In Depletion Mode MOSFET : Voltage divider Biasing In Enhancement Mode MOSFET : Feedback Bias and Voltage divider Bias
• operating regions	• Active, Cutoff, Saturation	• Ohmic, pinchoff region.	• Linear or Saturation region.
• Thermal runaway	• Thermal runaway occurs at High Voltages	• No thermal runaway	• No thermal runaway.

• Type of device	• Current Controlled Device	• Voltage Controlled Device	• Voltage Controlled Device.
• Terminals	• Base, Emitter, Collector	• Gate, Drain, Source	• Gate, Drain, Source.
• Input current	• Input current is order of mA	• Gate current is order of nA	• Gate current is order of pA.
• Applications	• Low current application	• Low voltage application	• Since power consumption is less used in CMOS Circuits

Current equation for MOSFET :-

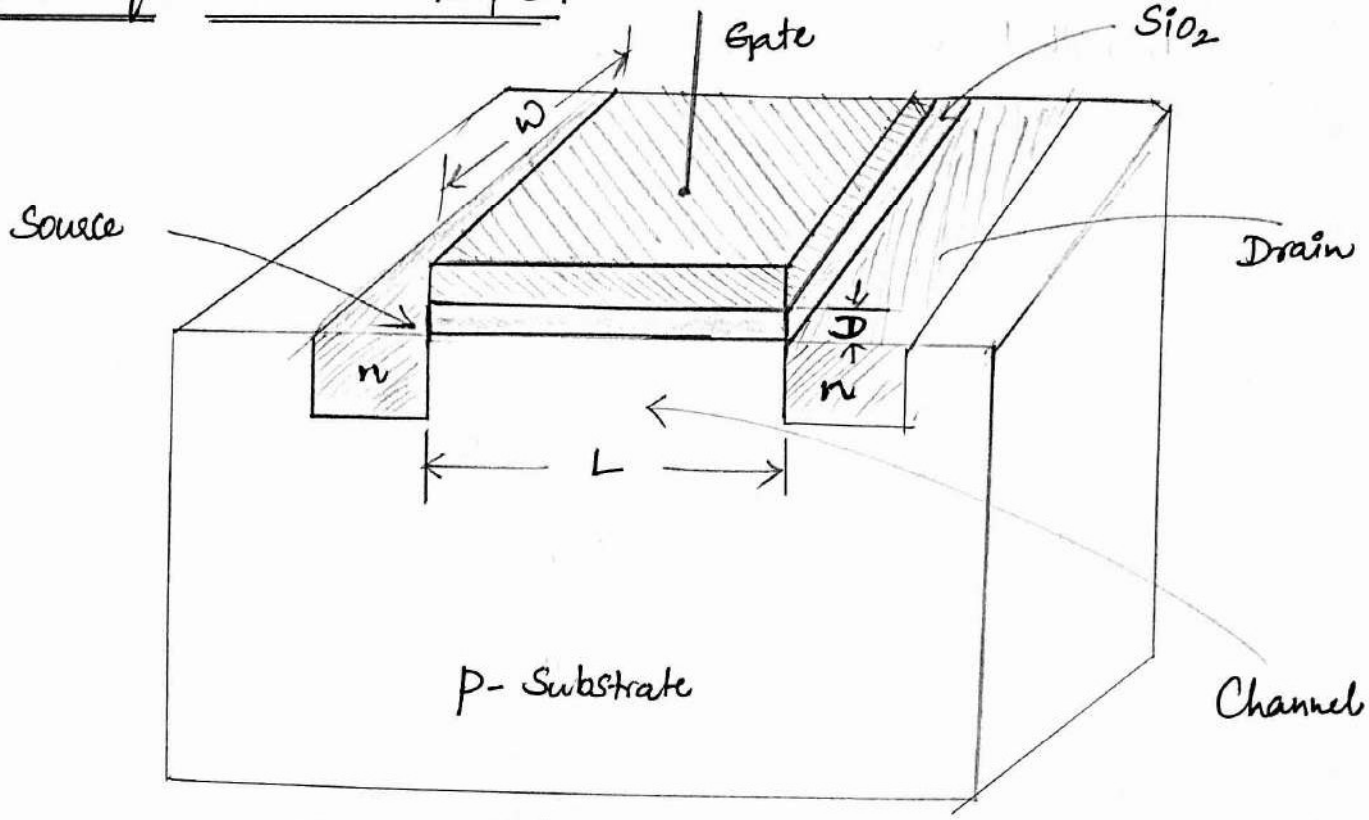


Fig: nMOS transistor structure

In above Fig,

Where L : Length of Channel

W : width of Channel

D : thickness of oxide layer

The whole concept of the MOS transistor evolves from the use of a voltage on the gate to induce a charge in the channel between source and Drain, which may then be caused to move from source to Drain under the influence of an electric field created by voltage V_{ds} applied between drain and source. Since the charged induced is dependent on the gate to source voltage V_{gs} then I_{ds} depends on both V_{gs} and V_{ds}.

$\therefore$ Current from Drain to source

$$I_{ds} = \frac{\text{Charge induced in channel } (Q_c)}{\text{Electron transit time } (T)} \quad \text{---(1)}$$

transit time τ defined as

$$\tau = \frac{\text{Length of Channel}(L)}{\text{Velocity}(v)} \quad \text{——— (2)}$$

Velocity of the electron depends on Electric field produced by Drain to Source voltage V_{ds}.

$$\text{Velocity}(v) \propto E_{ds}$$

$$v = \mu_n E_{ds} \quad \text{——— (3)}$$

Where E_{ds} is the Electric field formed between Source and Drain and E_{ds} is defined as

$$E_{ds} = \frac{V_{ds}}{L} \quad \text{—(4)}$$

Sub eqn(4) in eqn(3)

$$v = \mu_n \cdot \frac{V_{ds}}{L} \quad \text{——— (5)}$$

Sub eqn(5) in eqn(2)

$$\tau = \frac{L}{\mu_n \frac{V_{ds}}{L}}$$

$$\therefore \text{Transit Time} = \boxed{\tau = \frac{L^2}{\mu_n V_{ds}}} \quad \text{——— (6)}.$$

Typical values of

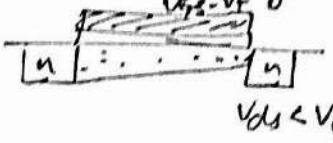
$\mu_n = 650 \text{ cm}^2/\text{V-sec}$

$\mu_p = 240 \text{ cm}^2/\text{V-sec}.$

Charge induced in Channel due to gate voltage is due to the voltage difference between the gate and the channel.

Note that the voltage along the channel varies linearly with distance from the Source to Drain.

assuming that the device is "not Saturated" then the average value is $\frac{V_{ds}}{2}$.



Furthermore, the effective gate voltage $V_g = V_{gs} - V_t$ where V_t is the threshold voltage needed to invert the charge under the gate and establish the channel.

Charge induced in the channel is defined as

$$Q_C = C_g \cdot V \quad \left[\because C = \frac{Q}{V}\right] \text{ ——(7)}$$

W.K.T

Capacitance $C_g = \frac{\epsilon A}{d}$

where $\epsilon = \epsilon_0 \epsilon_{ins}$, A is Area of the Channel i.e "W·L"

d is the distance between Gate and Channel i.e "D"

-thickness of oxide.

$$\therefore C_g = \frac{\epsilon_0 \epsilon_{ins} \cdot W \cdot L}{D} \text{ ——(8)}$$

Sub (8) in (7).

$$Q_C = \frac{\epsilon_0 \epsilon_{ins} \cdot W \cdot L}{D} \cdot V$$

$$Q_C = \epsilon_0 \epsilon_{ins} \cdot W \cdot L \cdot \frac{V}{D}$$

where V is the voltage difference between Gate and Channel and D is the distance between Gate and Channel.

$$Q_C = \epsilon_0 \epsilon_{ins} \cdot W \cdot L \cdot \frac{\left((V_{GS} - V_t) - \frac{V_{ds}}{2}\right)}{D}$$

hence $\frac{V}{D}$ is denoted as Electric field formed.

$$\therefore \quad Q_C = \epsilon_0 \epsilon_{ins} \cdot W \cdot L \cdot E_g \qquad \left\{ \because E_g = \frac{\left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right]}{D} \right\}$$

$$\longrightarrow (9)$$

where E_g : Average Electric field gate-to Channel

ϵ_{ins} : relative permittivity of insulation between Gate & Channel.

ϵ_0 : permittivity of free space

$\epsilon_0 = 8.85 \times 10^{-14}$ F cm^{-1}

$\epsilon_{ins} = 4.0$ for Si.

Sub eqn (6) and (9) in eqn (1)

$$I_{ds} = \frac{\epsilon_0 \epsilon_{ins} \cdot W \cdot L \, E_g}{\frac{L^2}{\mu_n V_{ds}}}$$

$$I_{ds} = \frac{\epsilon_0 \epsilon_{ins} \cdot W \cdot K \cdot \left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right]}{\frac{L^2 D}{\mu_n V_{ds}}}$$

$$\boxed{I_{ds} = \frac{\epsilon_0 \epsilon_{ins} \cdot \mu_n}{D} \cdot \frac{W}{L} \cdot \left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right] \cdot V_{ds}} \qquad \text{---------- (10)}$$

let $\quad K = \dfrac{\epsilon_0 \epsilon_{ins} \cdot \mu_n}{D}$

The factor $\frac{W}{L}$ is, of course, contributed by the geometry and it is common practice to write

$$\beta = K \frac{W}{L}$$

So that

$$\boxed{I_{ds} = K \cdot \frac{W}{L} \left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right] V_{ds}} \qquad \text{---------- (11)}$$

$$\boxed{I_{ds} = \beta \left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right] V_{ds}} \qquad \text{---------- (12)}$$

We also have

$$K = \frac{C_g \mu_n}{WL} \qquad \text{where } K = \frac{\epsilon_0 \epsilon_{ins} \mu_n}{D}$$

$$C_g = \frac{\epsilon_0 \epsilon_{ins} \cdot W \cdot L}{D}$$

So that eqn (11) becomes

$$I_{ds} = \frac{C_g \mu_n}{WL} \cdot \frac{W}{L}\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds} \qquad \frac{K}{C_g} = \frac{\frac{\epsilon_0 \epsilon_{ins} \cdot \mu_n}{D}}{\frac{\epsilon_0 \epsilon_{ins} \cdot W \cdot L}{D}}$$

$$\boxed{I_{ds} = \frac{C_g \mu_n}{L^2}\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds}} \longrightarrow (13)$$

$$\frac{K}{C_g} = \frac{\mu_n}{W \cdot L}$$

$$\therefore K = \frac{\mu_n C_g}{WL}.$$

Sometimes it is convenient to use gate capacitance per unit area C_{ox} rather than C_g in this and other expressions. Noting that

$$C_g = C_{ox} \cdot W \cdot L \qquad \text{where } C_{ox} = \frac{\epsilon_0 \epsilon_{ins}}{D}$$

So that eqn (13) can be written as

$$I_{ds} = \frac{C_{ox} \cdot W \cdot L \, \mu_n}{L^2}\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds}$$

$$\boxed{\therefore I_{ds} = C_{ox} \cdot \mu_n \cdot \frac{W}{L}\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)V_{ds}} \longrightarrow (14)$$

$\because K = C_{ox} \cdot \mu_n$

~~$\therefore I_{ds} = \beta$~~

where $\beta = C_{ox} \cdot \mu_n \frac{W}{L}$

and $K = C_{ox} \cdot \mu_n$.

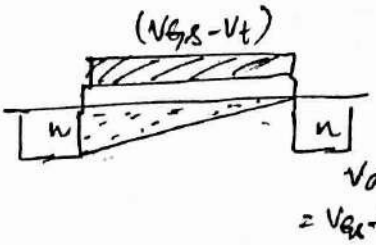
because

$K = \frac{\mu_n C_g}{WL}$

where $C_g = C_{ox} \cdot WL$

$K = \frac{\mu_n C_{ox} WL}{WL} = \mu_n C_{ox}$

* In pinchoff region :-



$V_{ds} = V_{gs} - V_t$

Sub above condition in eqn (11)

$$I_{ds} = K \cdot \frac{W}{L} \left[(V_{gs} - V_t) - \frac{(V_{gs} - V_t)}{2} \right] (V_{gs} - V_t)$$

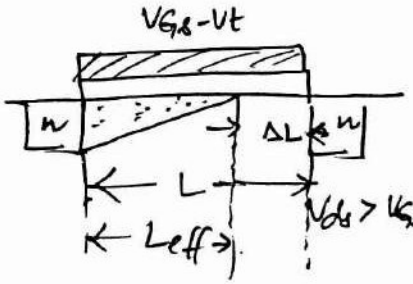
$$I_{ds} = \frac{K \cdot W}{2L} \left[V_{gs} - V_t \right]^2$$

$$\boxed{I_{ds} = \frac{K W}{2L} (V_{gs} - V_t)^2} \quad \text{---------- (15)}$$

$$\boxed{I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2} \quad \text{---------- (16)}$$

$$\boxed{I_{ds} = \frac{1}{2} \epsilon_{ox} \mu_n \frac{W}{L} (V_{gs} - V_t)^2} \quad (17) \text{ where } \beta = C_{ox} \mu_n \frac{W}{L}$$

* In Saturation region :-



$V_{ds} > V_{GS} - V_t$

in this condition

effective Channel length $L_{eff} = L - \Delta L$

Sub in eqn (15)

$$I_{ds} = \frac{KW}{2(L_{eff})} (V_{gs} - V_t)^2$$

$$= \frac{KW}{2(L - \Delta L)} (V_{gs} - V_t)^2 = \frac{KW}{2L\left(1 - \frac{\Delta L}{L}\right)} (V_{gs} - V_t)^2$$

$$= \frac{KW}{2L}(V_{gs}-V_t)^2\left(1-\frac{\Delta L}{L}\right)^{-1}$$

$\because (1-x)^{-1}$

$= 1+x+\frac{x^2}{2!}+\cdots$

Higher order terms are neglected

$= 1+x$

$$= \frac{KW}{2L}(V_{gs}-V_t)^2\left(1+\frac{\Delta L}{L}\right)$$

Where $\frac{\Delta L}{L} \propto V_{ds}$

$\therefore \frac{\Delta L}{L} = \lambda V_{ds}$

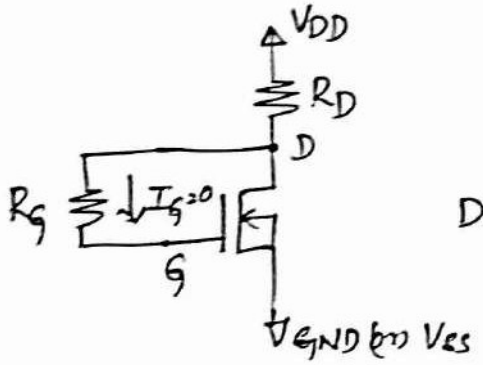
Where λ is the proportional constant and it is called as Channel length modulation parameters.

$$\therefore I_{ds} = \frac{KW}{2L}(V_{gs}-V_t)^2(1+\lambda V_{ds})$$

$$I_{ds} = \frac{1}{2}\beta(V_{gs}-V_t)^2(1+\lambda V_{ds}) \quad \text{—— (18)}$$

Feedback biasing Arrangement :-

A popular biasing arrangement for enhancement type MOSFET is provided in Fig 1. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on". Since $I_G = 0\,mA$ and $V_{R_G} = 0V$, the dc equivalent network appears as shown in Fig 1(a).



Fig(1)

DC equivalent

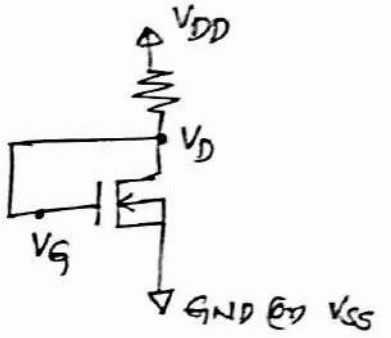


Fig 1a : DC equivalent of Feedback Bias

A direct connection now exists between drain and Gate, resulting in

$$V_D = V_G$$

and $V_S = 0$

hence

$$V_{DS} = V_{GS}$$

Output KVL is

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

where $V_{DS} = V_{GS}$

$$-V_{DD} + I_D R_D + V_{GS} = 0$$

$$\boxed{\therefore V_{GS} = V_{DD} - I_D R_D} \quad \text{——— (1)}$$

In eqn (1)

when $I_D = 0$	when $V_{GS} = 0$
$\therefore V_{GS} = V_{DD}$	$0 = V_{DD} - I_D R_D$.
	$V_{DD} = I_D R_D$
	$\therefore I_D = \frac{V_{DD}}{R_D}$

Two points are located on plot (V_{GS}, I_{DS}) as shown in below Fig.

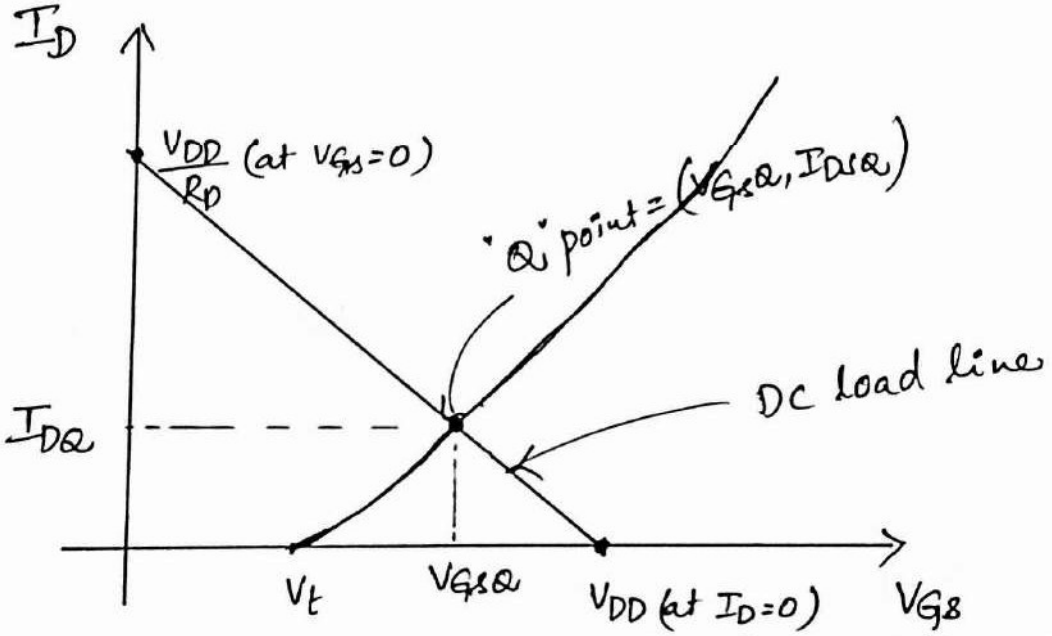


Fig: Determine the Q point for ~~the~~ Feedback bias.

Voltage-Divider Biasing Arrangement:-

A second popular biasing arrangement for the enhancement-type MOSFET appears in below Fig. The fact that $I_G = 0mA$ results in the following equation for V_{GG} as derived from the application of the voltage-divider rule:

$$\therefore V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD} \quad \text{——— (2)}$$

Applying KVL around the indicated loop of Fig will result in

$$-V_G + V_{GS} + I_D R_S = 0$$

$$\boxed{V_{GS} = V_G - I_D R_S} \quad \longleftarrow (3)$$

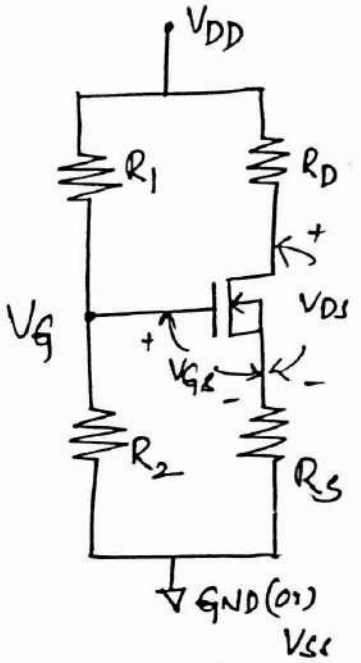


Fig: Voltage-divider Bias.

in eqn(3)

when $I_D = 0$

$V_{GS} = V_G$

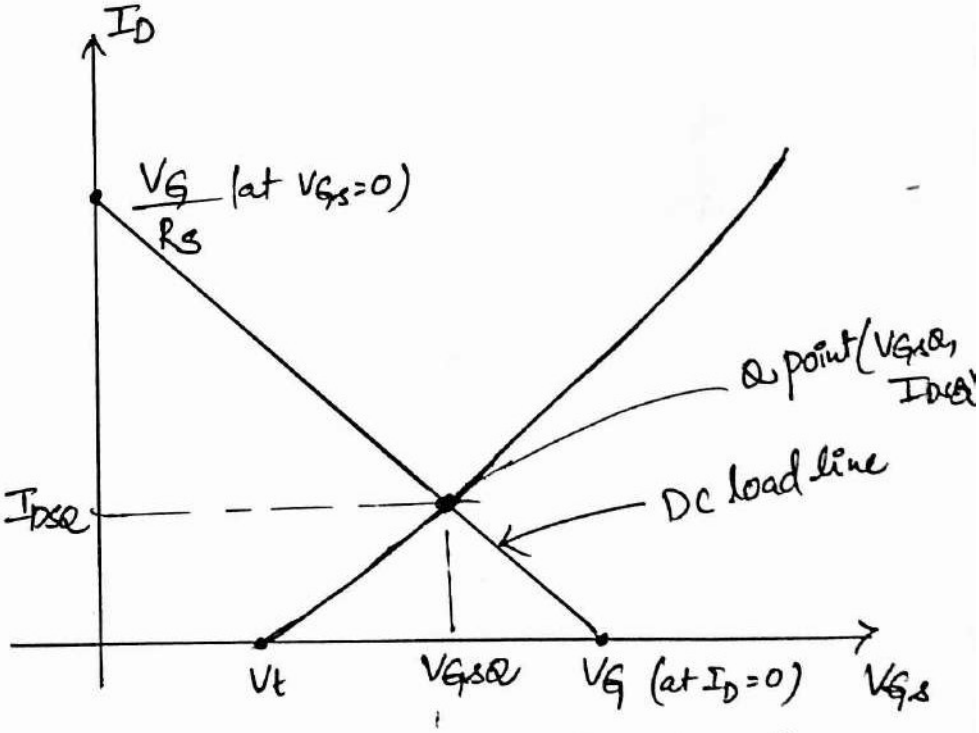
when $V_{GS} = 0$

$0 = V_G - I_D R_S$

$V_G = I_D R_S$

$\therefore I_D = \dfrac{V_G}{R_S}$

locate above two points on plot (V_{GS} Vs I_{DS}) as shown in below Fig:



where $V_G = \dfrac{R_2}{R_1+R_2} \cdot V_{DD}$

From the output

$$-V_{DD} + I_D R_D + V_{DS} + I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

at $I_D = I_{DSQ}$ $\boxed{V_{DSQ} = V_{DD} - I_{DSQ}(R_D + R_S).}$

✳ Problems and Solutions on MOSFET ✳

1. An NMOS transistor with $V_{TN}=1V$ has a drain current $i_D=0.8mA$ when $V_{GS}=3V$ and $V_{DS}=4.5V$. Calculate the drain current when a) $V_{GS}=2V$, $V_{DS}=4.5V$ and b) $V_{GS}=3V$; $V_{DS}=1V$.

Sol :- Given data

$$i_D = 0.8mA$$

$$V_{GS} = 3V$$

$$V_{DS} = 4.5V$$

$$V_{TN} = 1V$$

For given data, NMOS operating in "Saturation region" because $\boxed{V_{DS} > V_{GS} - V_{TN}}$ i.e $4.5V > 3V - 1V$

$$4.5V > 2V$$

∴ Current equation in NMOS for Saturation region is

$$i_D = \frac{\beta}{2}(V_{GS} - V_{TN})^2 \quad \text{where } \beta = \frac{K_n W}{L}$$

Let $\frac{\beta}{2}$ as K

$$i_D = K(V_{GS} - V_{TN})^2$$

$$0.8\times10^{-3} = K(3-1)^2$$

$$K = \frac{0.8\times10^{-3}}{2^2} = \frac{0.8\times10^{-3}}{4} = 0.2\,mA/V^2$$

$$\boxed{\therefore K = 0.2\,mA/V^2}$$

we have to find i_D for a) $V_{GS} = 2V$, $V_{DS} = 4.5V$ and

b) $V_{GS} = 3V$, $V_{DS} = 1V$.

a) Given $V_{GS} = 2V$, $V_{DS} = 4.5V$

$$V_{DS} > V_{GS} - V_{tN}$$

$$4.5 > 2 - 1$$

$$4.5 > 1$$

hence NMOS operating in Saturation region.

Current equation in Saturation region is $i_D = K(V_{GS} - V_{TN})^2$

$$i_D = 0.2 \times 10^{-3} (2-1)^2$$

$$i_D = 0.2 \times 10^{-3}$$

$$i_D = 0.2mA$$

b) Given $V_{GS} = 3V$, $V_{DS} = 1V$

$$V_{DS} \quad V_{GS} - V_{TN}$$

$$1 < 3 - 1$$

$$1 < 2$$

hence NMOS operating in Linear region.

Current equation in Linear region is $i_D = \frac{KW}{L}\left[(V_{GS} - V_{TN}) - \frac{V_{ds}}{2}\right]V_{ds}$

$$K = \frac{\frac{KW}{L}}{2}$$

$$\therefore \frac{KW}{L} = 2K$$

Where K obtained as $0.2mA/V^2$.

$$\frac{KW}{L} = 2 \times 0.2 mA/V^2$$

$$= 0.4 mA/V^2$$

$$\therefore i_D = \frac{KW}{L}\left[(V_{gs} - V_{TN}) - \frac{V_{ds}}{2}\right] V_{ds}$$

$$= 0.4 \times 10^{-3}\left[(3-1) - \frac{1}{2}\right] \cdot 1 \quad \because V_{gs} = 3V ; V_{DS} = 1$$

$$= 0.4 \times 10^{-3}\left[2 - \frac{1}{2}\right]$$

$$= 0.4 \times 10^{-3}\left[\frac{3}{2}\right]$$

$$= 0.6 \times 10^{-3}$$

$$i_D = \underline{0.6 mA}$$

2. Determine the Source to Drain voltage required to bias a p-channel enhancement-mode MOSFET in the Saturation region. Consider an enhancement mode p-channel MOSFET for which $K_p = 0.2 mA/V^2$, $V_{TP} = -0.50V$ and $i_D = 0.5 mA$

Sol:-

Given:

Type of MOSFET : p-channel MOSFET

Operating region : Saturation region

$K_p = 0.2 mA/V^2$

$V_{TP} = -0.5V$

$i_D = 0.5 mA$

We have to find V_{SD}.

For Saturation region, condition is

$$V_{SD} = V_{SG} + V_{TP} \quad \text{— (1)}$$

V_{TP} given in the data, we have to find V_{SG}

in Saturation region current equation for p MOS

$$i_D = K_p (V_{SG} + V_{TP})^2$$

$$0.5\times10^{-3} = 0.2\times10^{-3} (V_{SG} - 0.5)^2$$

$$\frac{0.5\times10^{-3}}{0.2\times10^{-3}} = (V_{SG} - 0.5)^2$$

$$(V_{SG} - 0.5)^2 = \frac{0.5}{0.2}$$

$$(V_{SG} - 0.5)^2 = 2.5$$

$$V_{SG} - 0.5 = \sqrt{2.5}$$

$$V_{SG} - 0.5 = 1.58$$

$$V_{SG} = 1.58 + 0.5$$

$$V_{SG} = 2.08V$$

from eqn (1)

$$\therefore V_{SD} = 2.08 - 0.5$$

$$\therefore V_{SD} = 1.58V$$

3. Calculate the current in an n-Channel MOSFET. Consider an n-Channel enhancement mode MOSFET with the following parameters $V_{TN} = 0.4V$, $W = 20\mu m$, $L = 0.8\mu m$, $\mu_n = 650\ cm^2/V\text{-}S$, $t_{ox} = 200\ \text{Å}$ and $\epsilon_{ox} = 3.9(8.85\times10^{-14})\ F/cm$. Determine the current when the transistor is biased in the Saturation region for a) $V_{GS} = 0.8V$ and b) $V_{GS} = 1.6V$.

Sol:- Given data:

$$V_{TN} = 0.4V$$
$$W = 20\mu m = 20\times10^{-4}cm$$
$$L = 0.8\mu m = 0.8\times10^{-4}cm$$
$$\mu_n = 650\ cm^2/V\text{-}S$$

$$\beta_n = \frac{\epsilon_{ox}\cdot\mu_n}{t_{ox}}\cdot\frac{W}{L}$$

$$= \frac{3.9(8.85\times10^{-14})\times650}{200\times10^{-8}}\times\frac{20\times10^{-4}}{0.8\times10^{-4}}$$

$$\boxed{\beta_n = 2.80mA/V^2}$$

a) for $V_{GS} = 0.8V$

$$I_D = \frac{\beta}{2}(V_{GS}-V_{TN})^2 = \frac{1.40\times10^{-3}}{2}(0.8-0.4)^2$$

$$I_D = 0.224mA$$

b) for $V_{GS} = 1.6V$

$$I_D = \frac{\beta}{2}(V_{GS}-V_{TN})^2 = \frac{1.40\times10^{-3}}{2}(1.6-0.4)^2$$

$$I_D = 2.02mA$$

4. The data sheet for a certain enhancement MOSFET states that drain current is $I_D = 3mA$ at $V_{GS} = 10V$ and $V_{GS(TN)} = 5V$. Determine the drain current I_D for $V_{GS} = 8V$.

Sol:- Given data : $I_D = 3mA$

$V_{GS} = 10V$

$V_{GS(TN)} = 5V$

$I_D = ?$ for $V_{GS} = 8V$

$$I_D = K(V_{GS} - V_{GS(TN)})^2$$

Where $K = \frac{\beta}{2}$ Where $\beta = \frac{K_n W}{L}$ Where $K = \frac{\epsilon_{ox} \cdot \mu_n}{t_{ox}}$

$$K = \frac{I_D}{(V_{GS} - V_{GS(TN)})^2}$$

$$= \frac{3 \times 10^{-3}}{(10-5)^2} = \frac{3 \times 10^{-3}}{25}$$

$$\boxed{K = 0.12\ mA/V^2}$$

Thus, the drain current I_D at $V_{GS} = 8V$ is $I_D = K(V_{GS} - V_{GS(TN)})^2$

$$I_D = 0.12 \times 10^{-3}(8-5)^2$$

$$I_D = 1.08mA$$

5. The n-Channel MOSFET shown in the figure operates with drain current $I_D = 0.4\ mA$ and $V_D = 1.0V$. The transistor has $V_{GS(Th)} = 2.0V$, $\mu_n C_{ox} = 20\mu A/V^2$, $L = 10\mu m$ and $W = 400\mu m$. Determine its drain resistance R_D and source resistance R_S.

Sol:- Given $I_D = 0.4mA$

$V_D = 1.0V$

$V_{GS(Th)} = 2.0V$

$\mu_n C_{ox} = 20\mu A/V^2$

$L = 10\mu m$

$W = 400\mu m$

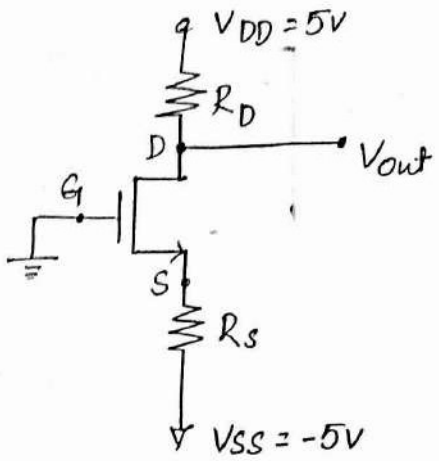


Fig - ①

Find V_{GS} from current equation.

$$I_D = \frac{1}{2} C_{ox} \mu_n \frac{W}{L} (V_{GS} - V_{th})^2$$

$$0.4\times10^{-3} = \frac{1}{2} \times 20\times10^{-6} \times \frac{400\times10^{-6}}{10\times10^{-6}} (V_{GS} - 2)^2$$

$$0.4\times10^{-3} = 400\times10^{-6} (V_{GS} - 2)^2$$

$$0.4\times10^{-3} = 0.4\times10^{-3} (V_{GS} - 2)^2$$

above equation satisfied for $V_{GS} = 1V$ or $V_{GS} = 3V$.

we have to chose $V_{GS} = 3V$, because V_{GS} should be greater than $V_{GS(Th)}$ i.e 2.0V.

$\therefore \quad V_{GS} = 3V$

where $V_{GS} = V_G - V_S$.

From the Fig ① $V_G = 0$

$$V_{GS} = -V_S$$

$$V_S = -V_{GS}$$

$$V_S = -3V$$

The Source resistance $R_S = \dfrac{V_S - V_{SS}}{I_D}$

$= \dfrac{-3-(-5)}{0.4\times10^{-3}}$

$= \dfrac{-3+5}{0.4\times10^{-3}} = \dfrac{2}{0.4\times10^{-3}}$

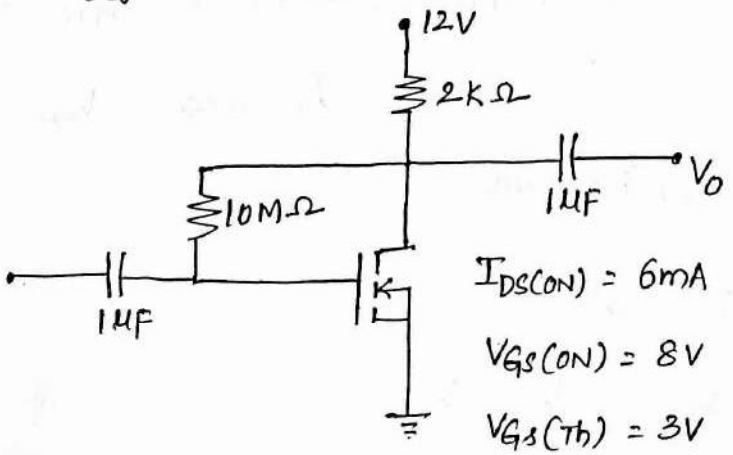
$\therefore R_S = 5K\Omega$

The Drain resistance $R_D = \dfrac{V_{DD} - V_D}{I_D}$

$= \dfrac{5-1}{0.4\times10^{-3}} = \dfrac{4}{0.4\times10^{-3}}$

$\therefore R_D = 10K\Omega$

6. Determine I_{DQ} and V_{DSQ} for the enhancement type MOSFET.



Sol:- For given values $K = \dfrac{I_{D(ON)}}{(V_{GS(ON)} - V_{GS(Th)})^2}$

$= \dfrac{6mA}{(8V-3V)^2} = 0.24\times10^{-3} A/V^2$

$K = 0.24 mA/V^2$

Consider current equation

$$I_D = K\left(V_{GS} - V_{GS(Th)}\right)^2$$

→ FOR $V_{GS} = 10V$

$I_D = 0.24\times10^{-3}(10-3)^2$

$I_D = 11.76mA$

→ FOR $V_{GS} = 3V$

$I_D = 0.24\times10^{-3}(3-3)$

$I_D = 0mA$

→ FOR $V_{GS} = 6V$

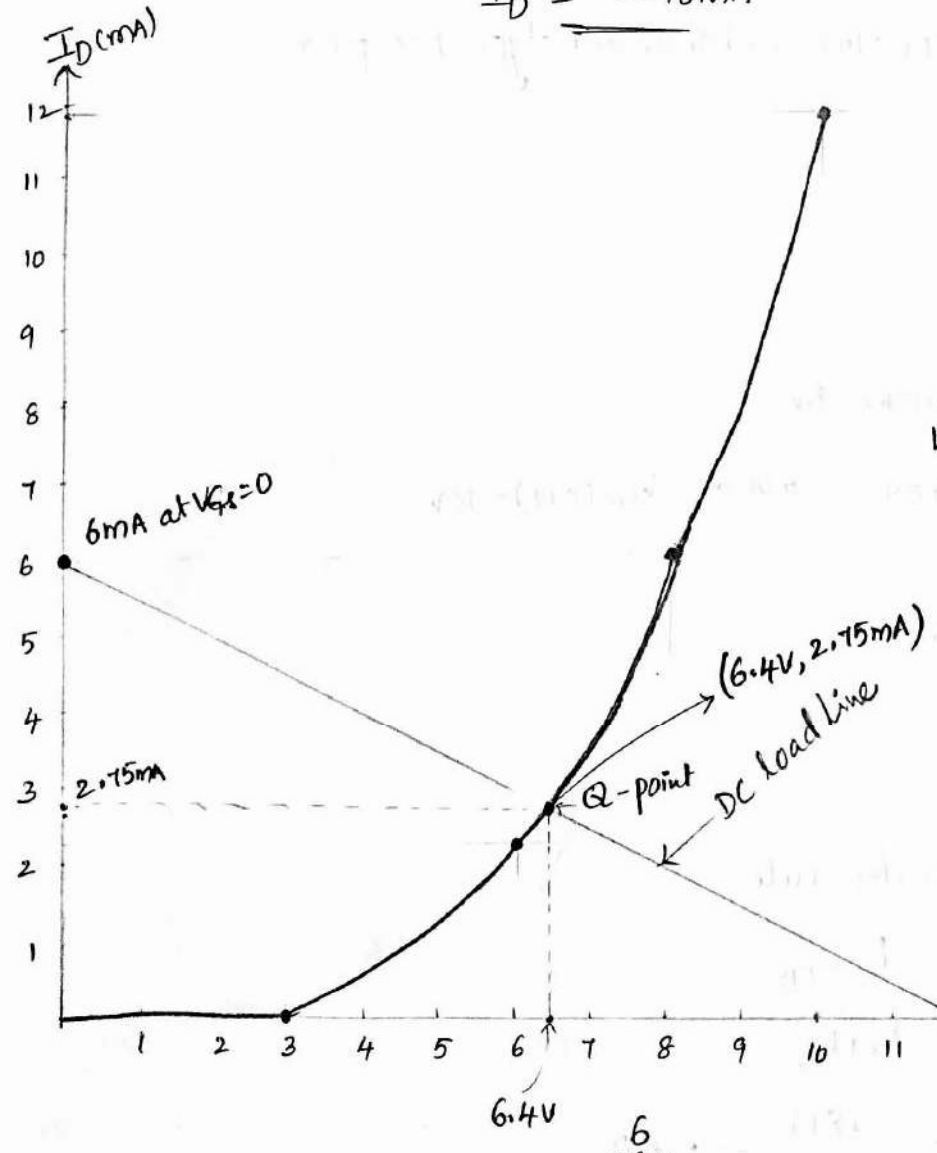
$I_D = 0.24\times10^{-3}(6-3)^2$

$I_D = 2.16mA$

→ FOR $V_{GS} = 8V$

$I_D = 0.24\times10^{-3}(8-3)^2$

$I_D = 6mA$



For given fig

$V_G = V_D$. $[\because I_G = 0]$

and $V_S = 0$

$\therefore V_{GS} = V_{DS}$

Write the output KVL

$-V_{DD} + I_D R_D + V_{DS} = 0$

where $V_{DS} = V_{GS}$

$-V_{DD} + I_D R_D + V_{GS} = 0$

$$V_{GS} = V_{DD} - I_D R_D$$

DC load line eqn

In above eqn consider

$V_{GS} = 0$

$0 = V_{DD} - I_D R_D$

$I_D R_D = V_{DD}$

$$I_D = \frac{V_{DD}}{R_D}$$

$$I_D = \frac{12V}{2K}$$

$I_D = 6mA$ for $V_{GS} = 0$

In Same equation

$$I_D = 0$$

$$V_{GS} = V_{DD} - 0 \times R_D$$

$$V_{GS} = V_{DD}$$

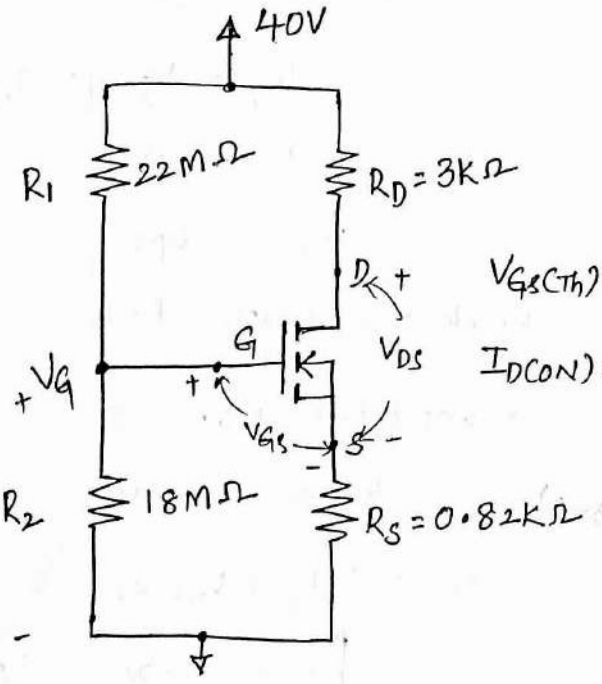
$$\therefore V_{GS} = 12V \quad \text{—— } I_D = 0$$

Locate above two points on the plots.

From the plot Q-point = (V_{GSQ}, I_{DQ})

$= (6.4V, 2.75mA)$

7. Determine I_{DQ} and V_{DSQ} for the enhancement type MOSFET



Sol:-

From voltage divides rule

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_G = \frac{18M}{22M + 18M} \cdot 40$$

$$V_G = \frac{18M}{40M} \cdot 40 = 18V \quad \therefore V_G = 18V$$

From given data

$$K = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_{GS(Th)})^2}$$

$$= \frac{3mA}{(10-5)^2} = \frac{3mA}{25}$$

$$K = 0.12 mA/V^2$$

$$I_D = 0.12 \times 10^{-3} (V_{GS} - 5)^2$$

→ at $V_{GS} = 5V$

$$I_D = 0$$

→ at $V_{GS} = 10V$

$$I_D = 0.12 \times 10^{-3} (10-5)^2$$

$$= 0.12 \times 10^{-3} \times 25$$

$$I_D = 3mA$$

→ at $V_{GS} = 15V$

$$I_D = 0.12 \times 10^{-3} (15-5)^2$$

$$= 0.12 \times 10^{-3} \times 100$$

$$= 12 mA$$

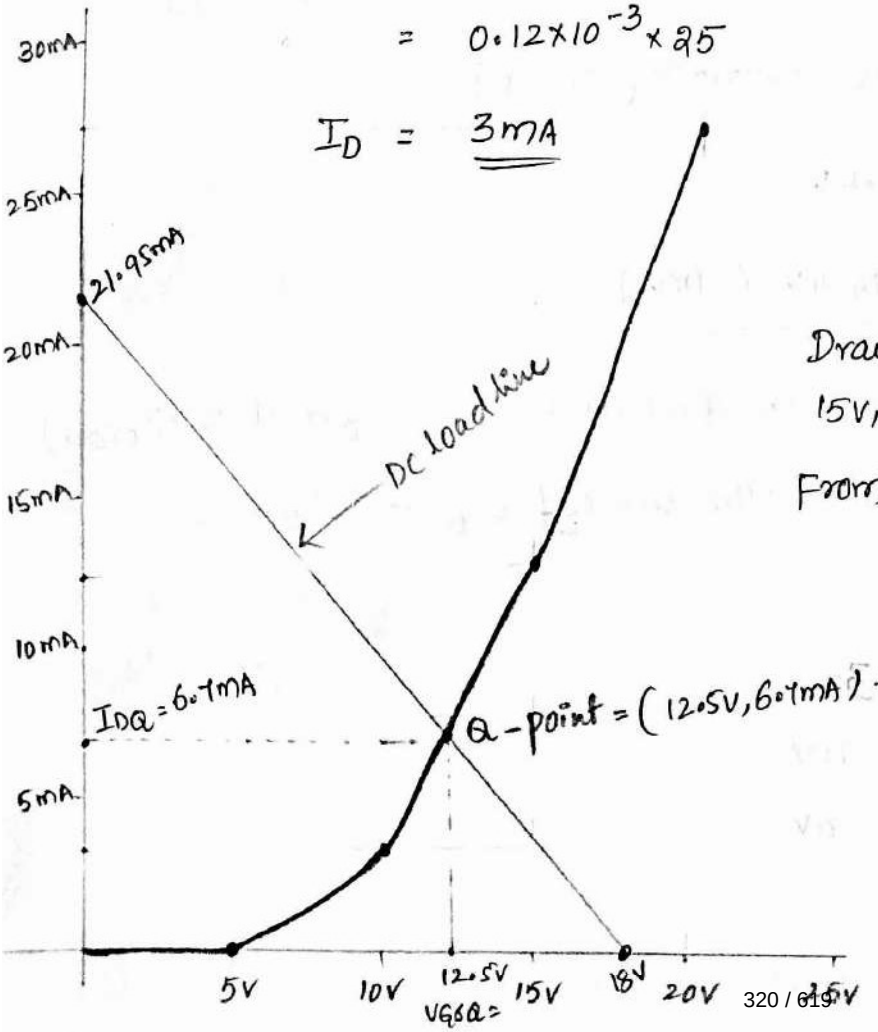
→ at $V_{GS} = 20V$

$$I_D = 0.12 \times 10^{-3} (20-5)^2$$

$$= 0.12 \times 10^{-3} \times 225$$

$$I_D = 27mA$$

Draw the plot by considering $V_{GS} = 5V, 10V, 15V, 20V$.



From the Fig, write the input KVL

$$-V_G + V_{GS} + I_D \cdot R_S = 0$$

$$\boxed{V_{GS} = V_G - I_D R_S}$$ DC load line eqn

When $I_D = 0$

$$V_{GS} = V_G$$

$$\therefore V_{GS} = 18V$$

When $V_{GS} = 0$

$$V_{GS} = V_G - I_D R_S$$

$$0 = V_G - I_D R_S$$

$$I_D = \frac{V_G}{R_S} = \frac{18}{0.82k}$$

$$I_D = 21.95mA$$

locate $V_{GS} = 18V$ (for $I_D = 0$) and $I_D = 21.95mA$ (for $V_{GS} = 0$).

From that, @ point $(V_{GSQ}, I_{DQ}) = (12.5V, 6.7mA)$.

→ Write the Output KVL

$$-V_{DD} + I_D R_D + V_{DS} + I_D R_S = 0$$

$$V_{DS_Q} = V_{DD} - I_{D_Q}(R_D + R_S)$$

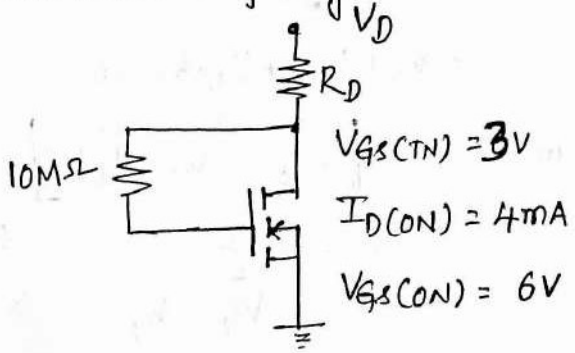
$$= 40V - 6.7 \times 10^{-3}(3K + 0.82K)$$

$$= 40V - 6.7 \times 10^{-3}(3.82K)$$

$$V_{DSQ} = 14.4V$$

$$\therefore (V_{DSQ}, I_{DQ}) = (14.4V, 6.7mA)$$

8. The levels of V_{DS} and I_D are specified as $V_{DS} = \frac{1}{2}V_{DD}$ and $I_D = I_{D(ON)}$ for the network of Fig. Determine the levels of V_{DD} and R_D.



Sol:- Given $I_D = I_{D(ON)} = 4mA$ and $V_{GS} = V_{GS(ON)} = 6V$ for this Configuration

$$V_{DS} = V_{GS} = \frac{1}{2} V_{DD}$$

$$6V = \frac{1}{2} V_{DD}$$

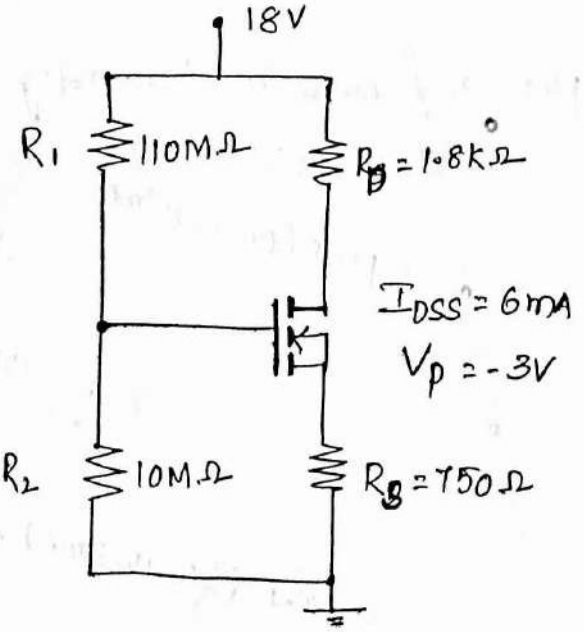
$$V_{DD} = 12V$$

$$R_D = \frac{V_{DD} - V_{DS}}{I_{D(ON)}} = \frac{V_{DD} - \frac{1}{2}V_{DD}}{I_{D(ON)}} = \frac{\frac{V_{DD}}{2}}{I_{D(ON)}}$$

$$= \frac{6V}{4mA}$$

$$R_D = 1.5K\Omega$$

9. Determine the operating point (V_{GSQ}, I_{DSQ}) for given circuit having depletion mode MOSFET. Repeat Same for $R_S = 150\Omega$



Sol:-

To Study the performance of depletion mode MOSFET, we have to use Shockly equation, because operation of depletion mode MOSFET Similar to JFET.

Shockly equation :-

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

→ at $V_{GS} = V_p$

$$I_D = 0$$

→ at $V_{GS} = \frac{V_p}{2} = \frac{-3}{2} = -1.5V$

$$I_D = 6\times10^{-3}\left(1-\left(\frac{+1.5}{+3}\right)\right)^2$$

$$= 6\times10^{-3}\left(1-\frac{1.5}{3}\right)^2$$

$$I_D = \underline{1.5mA}$$

$\rightarrow V_{GS} = 0$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$= 6\times10^{-3}\left(1-\frac{0}{V_P}\right)^2$$

$$I_D = 6\times10^{-3}$$

$$I_D = \underline{6mA}$$

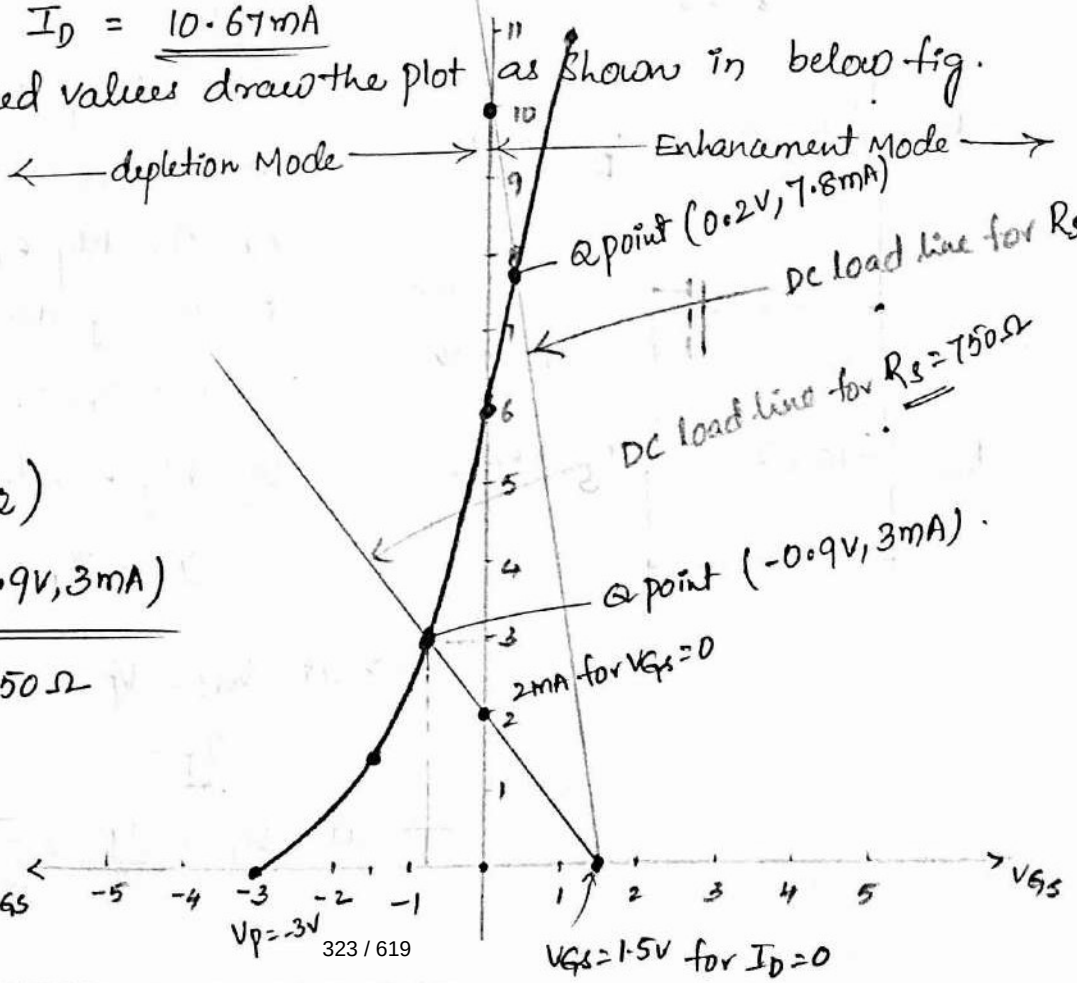
$\rightarrow V_{GS} = 1V$

$$I_D = 6\times10^{-3}\left(1-\frac{1}{-3}\right)^2$$

$$I_D = 6\times10^{-3}\left(1+\frac{1}{3}\right)^2$$

$$I_D = \underline{10.67mA}$$

For obtained values draw the plot as shown in below fig.



$\therefore$ Q point

(V_{GSQ}, I_{DQ})

$= \underline{(-0.9V, 3mA)}$

for $R_S = 750\Omega$

*** if $R_S = \underline{150\Omega}$

Qpoint $\underline{=}$ (V_{GSQ}, I_{DQ})

$= \underline{(0.2V, 7.8mA)}$

For given circuit, by applying voltage divider rule

$$V_G = \frac{R_2}{R_1+R_2} \cdot V_{DD}$$

$$= \frac{10M}{120M} \cdot 18$$

$$V_G = 1.5V$$

By writing input KVL

$$-V_G + V_{GS} + I_D R_S = 0$$

$$\boxed{V_{GS} = V_G - I_D R_S}$$ — load line eqn.

When $I_D = 0$

$V_{GS} = V_G$

$\therefore V_{GS} = 1.5V$

When $V_{GS} = 0$

$0 = V_G - I_D R_S$

$V_G = I_D R_S$

$$I_D = \frac{V_G}{R_S} = \frac{1.5V}{750}$$

$I_D = 2mA$

to get the DC load line, locate the above points on the plot.

from that Q-point

$(V_{GSQ}, I_{DQ}) = (-0.9V, 3mA)$ for $R_S = 750\Omega$

*** if $R_S = 150\Omega$

load line eqn

$$\boxed{V_{GS} = V_G - I_D R_S}$$ — load line eqn.

When $I_D = 0$

$V_{GS} = V_G$

$\therefore V_{GS} = 1.5V$

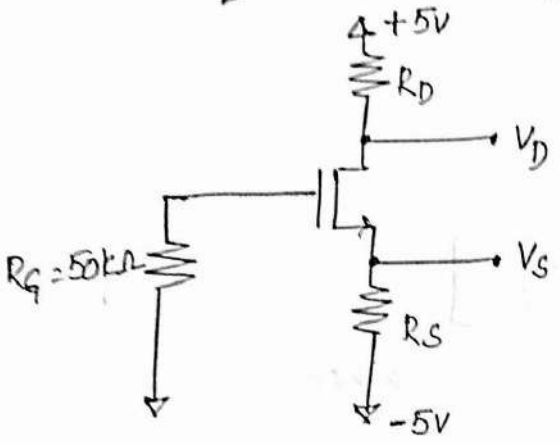
When $V_{GS} = 0$

$0 = V_G - I_D R_S$

$$I_D = \frac{V_G}{R_S} = \frac{1.5V}{150}; \quad I_D = 10mA$$

from the plot Q point is $(0.2V, 7.8mA)$

10. Design a MOSFET circuit biased with both positive and negative voltages to meet a set of specifications: The circuit configuration to be designed is shown in Fig. Design the circuit such that $I_{DQ} = 0.5mA$ and $V_{DSQ} = 4V$. Choices: Standard resistors are to be used in the final design. A transistor with nominal parameters of $K_n' = 80\mu A/V^2$, $\frac{W}{L} = 6.25$ and $V_{TN} = 1.2V$ is available.



Sol:- Given $I_{DQ} = 0.5mA$

$V_{DSQ} = 4V$

$K_n' = 80\mu A/V^2$

$\frac{W}{L} = 6.25$

$V_{TN} = 1.2V$

For above Fig $V_G = 0$

$$V_{GS} = V_G - V_S$$

$$= 0 - V_S$$

$$V_S = -V_{GS}$$

To find V_S, we require V_{GS} and V_{GS} is obtained from current equation i.e $i_D = K_n' \cdot \frac{W}{L} (V_{GS} - V_{TN})^2$

$$0.5\times10^{-3} = 80\times10^{-6} \times 6.25 (V_{GS} - 1.2)^2$$

$$(V_{GS} - 1.2)^2 = \frac{0.5}{80\times10^{-3}\times6.25} = \frac{0.5\times10^3}{80\times6.25}$$

$$(V_{gs} - 1.2)^2 = 1$$

$$V_{gs} - 1.2 = 1$$

$$V_{gs} = 2.2V$$

$\therefore V_S = -V_{GS}$

$$V_S = -2.2V$$

From this, we can calculate R_S

$$R_S = \frac{V_S - (-5)}{I_D}$$

$$= \frac{-2.2 + 5}{0.5mA}$$

$$R_S = \frac{2.8}{0.5mA}$$

$$**R_S = 5.6k\Omega$$

* Given $V_{DSQ} = 4V$

$$V_{DS} = V_D - V_S$$

$$4 = V_D - V_S$$

$$= V_D - (-2.2)$$

$$4 = V_D + 2.2$$

$$V_D = 4 - 2.2$$

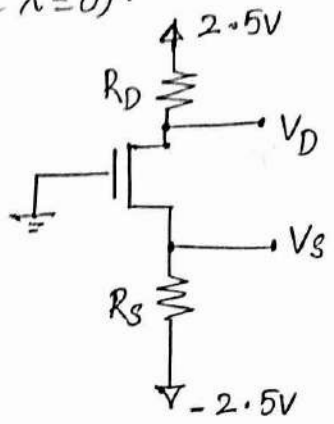
$$V_D = 1.8V$$

from this we can calculate R_D

$$R_D = \frac{5 - V_D}{I_D} = \frac{5 - 1.8}{0.5mA} = \frac{3.2}{0.5mA}$$

$$**R_D = 6.4k\Omega$$

11. Design the circuit shown below that is determine the values of R_D and R_S so that the transistor operates at $I_D = 0.4mA$ and $V_D = 0.5V$. The NMOS transistor has $V_t = 0.7V$, $\mu_n C_{ox} = 100\mu A/V^2$ $L = 1\mu m$ and $W = 32\mu m$. Neglect the channel length Modulation effect (i.e $\lambda = 0$).



Sol:- Given $I_D = 0.4mA$

$V_D = 0.5V$

$V_t = 0.7V$

$\mu_n C_{ox} = 100\mu A/V^2$

$L = 1\mu m$

$W = 32\mu m$

For given circuit

$V_G = 0$

$V_{GS} = V_G - V_S$

$V_{GS} = 0 - V_S$

$V_S = -V_{GS}$ — (1)

$\therefore V_S = -1.2V$

$$R_S = \frac{V_S - (-2.5)}{I_D}$$

$$= \frac{-1.2 + 2.5}{0.4 \times 10^{-3}}$$

$$* R_S = 3.25k\Omega$$

To find the V_{GS}

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{gs} - V_t)^2$$

$$0.4mA = \frac{100 \times 10^{-6}}{2} \times \frac{32}{1} (V_{gs} - V_t)^2$$

$$0.4 \times 10^{-3} = 100 \times 10^{-6} \times \frac{32}{2} (V_{gs} - 0.7)^2$$

$$\frac{0.4}{100 \times 32 \times 10^{-3}} = (V_{gs} - 0.7)^2$$

$$\frac{400 \times 2}{3200} = (V_{gs} - 0.7)^2$$

$$\sqrt{0.25} = V_{gs} - 0.7$$

$$0.5 = V_{gs} - 0.7$$

$$V_{gs} = 1.2V$$ — (2)

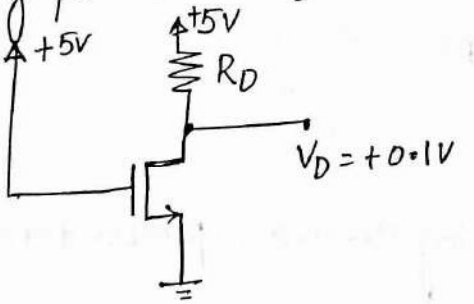
$$R_D = \frac{2.5 - V_D}{I_D}$$

$$= \frac{2.5 - 0.5}{0.4\,mA}$$

$$= \frac{2}{0.4}$$

$$* R_D = 5K\Omega$$

12. Design the circuit in below Fig to establish a drain voltage of 0.1V. What is the effective resistance between drain and source at this operating point? Let $V_t = 1V$ and $k_n'(W/L) = 1mA/V^2$.



Sol:- In above circuit $V_G = 5V$, $V_S = 0$, $V_{GS} = 5V$, $V_D = 0.1V$

$V_S = 0$ $V_{DS} = 0.1V$

From above conditions

$$\boxed{V_{DS} < V_{GS} - V_t}$$

$$0.1V < (5 - 1)V$$

$$0.1V < 4V$$

hence device is operating in "Linear region."

Current equation in Linear region $= k_n' \frac{W}{L}\left((V_{GS} - V_t) - \frac{V_{ds}}{2}\right)V_{ds}$

$$I_D = 1\times10^{-3}\left[(5-1) - \frac{0.1}{2}\right]\times 0.1$$

$$= 1\times10^{-3}\left[4 - \frac{0.1}{2}\right]\times0.1 = 1\times10^{-3}\left[\frac{7.9}{2}\right]\times0.1$$

$$** I_D = 0.395mA$$

$$R_D = \frac{5 - V_D}{I_D}$$

$$= \frac{5 - 0.1}{0.395m}$$

$$R_D = \frac{4.9}{0.395m}$$

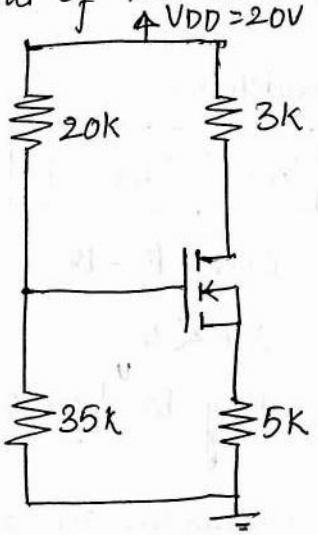
$$* R_D = 12.40K\Omega$$

Effective Drain to Source resistance: $R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.1}{0.395 \times 10^{-3}}$

$$= 0.253K\Omega$$

Effective Drain to Source resistance $= R_{DS} = 253\Omega$

13. Consider the following circuit. process transconductance parameter $K_n' = 0.5mA/V^2$, $\frac{W}{L} = 1$. Threshold voltage = 3V, $V_{DD} = 20V$, Find the operating point of the circuit.



Sol:- Given data $K_n' = 0.5mA/V^2$ $V_{DD} = 20V$.

$$\frac{W}{L} = 1$$

$$V_t = 3V$$

Current equation

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L} (V_{GS} - V_t)^2 \quad \because \frac{\beta}{2}.$$

Where $\beta = k_n' \cdot \frac{W}{L}$

$$I_D = \frac{0.5 \times 10^{-3} \times 1}{2} (V_{GS} - 3)^2$$

$$I_D = 0.25 \times 10^{-3} (V_{GS} - 3)^2$$

→ at $V_{GS} = 3V$

$I_D = 0$

→ at $V_{GS} = 6V$

$I_D = 0.25 \times 10^{-3} (6-3)^2$

$= 0.25 \times 10^{-3} (3)^2$

$I_D = 2.25mA$

→ at $V_{GS} = 9$

$I_D = 0.25 \times 10^{-3} (9-3)^2$

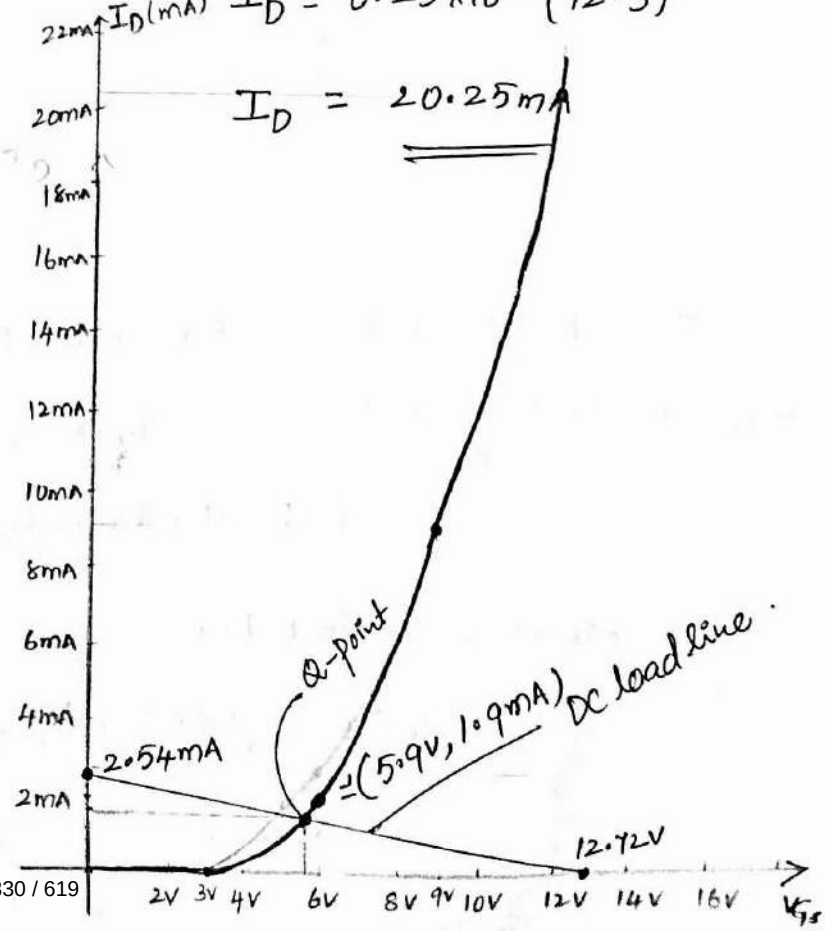
$I_D = 0.25 \times 10^{-3} (6)^2$

$I_D = 9mA$

→ at $V_{GS} = 12$

$I_D = 0.25 \times 10^{-3} (12-3)^2$

$I_D = 20.25mA$



By considering $V_{GS} = 3V, 6V, 9V$ and $12V$, I_D values $0mA, 2.25mA, 9mA, 20.25mA$ are located in the plot.

And from the circuit we have to find V_G by applying voltage divider rule.

$$V_G = \frac{R_2}{R_1+R_2} \cdot V_{DD}$$

$$= \frac{35K}{20K+35K} \cdot 20$$

$$= \frac{35K}{55K} \times 20$$

$$V_G = 12.72V$$

To find the DC load line equation, write the i/p KVL

$$-V_G + V_{GS} + I_D R_S = 0$$

$$V_{GS} = V_G - I_D R_S \quad \text{—— Load line eqn.}$$

When $I_D = 0$

$$V_{GS} = V_G$$

$$V_{GS} = 12.72V$$

When $V_{GS} = 0$

$$0 = V_G - I_D R_S$$

$$V_G = I_D R_S$$

$$I_D = \frac{V_G}{R_S} = \frac{12.72}{5\times10^3}$$

$$I_D = 2.54mA$$

This two points are located on the plot to draw the DC load line. From the intersecting point we can find Q-point (V_{GSQ}, I_{DQ}).

Q point $(V_{GSQ}, I_{DQ}) = (5.9V, 1.9mA)$

Write the output KVL

$$-20V + I_{DQ}\times3\times10^3 + V_{DSQ} + I_{DQ}\times5\times10^3 = 0$$

$$V_{DSQ} = 20 - I_{DQ}(8\times10^3)$$

$$= 20 - 1.9\times10^{-3}(8)\times10^3 \Rightarrow 20 - 15.2 = 4.8V$$

$\therefore (V_{DSQ}, I_{DQ})$

$\Downarrow$

$(4.8V, 1.9mA)$

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14. For a MOSFET, the threshold voltage is +3V, Gate-to Source voltage is 20V, W/L ratio is 5, process transconductance parameter is 40μA/V². Find drain to source current in saturation. (12)

Sol:- Given data :

$V_t = +3V$

$V_{GS} = 20V$

$\frac{W}{L} = 5$

$K_n' = 40\mu A/V^2$

I_D in saturation region ?

$$I_D = \frac{K_n'}{2} \cdot \frac{W}{L} (V_{GS} - V_t)^2$$

$$= \frac{40 \times 10^{-6}}{2} \times 5 (20-3)^2$$

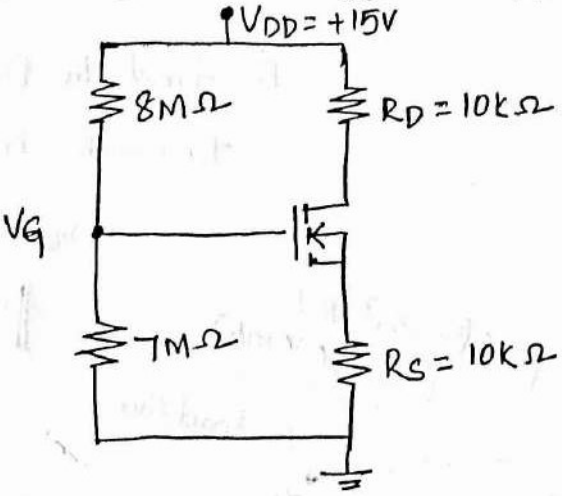
$$= 100 \times 10^{-6} (17)^2$$

$$= 28900 \times 10^{-6} A$$

(or)

$$I_D = 2.89mA$$

15. Find bias point for $V_t = 1V$, $K_n' W/2L = 1mA/V^2$ for given figure.



Sol:- Given data:

$V_t = 1V$

$K_n' W/L = 1mA/V^2$

Current in Saturation region

$$I_D = K_n' \frac{W}{L} (V_{GS} - V_t)^2$$

$$= K_n' \frac{W}{L} (V_{GS} - 1)^2$$

$$\boxed{I_D = 1 \times 10^{-3} (V_{GS} - 1)^2}$$

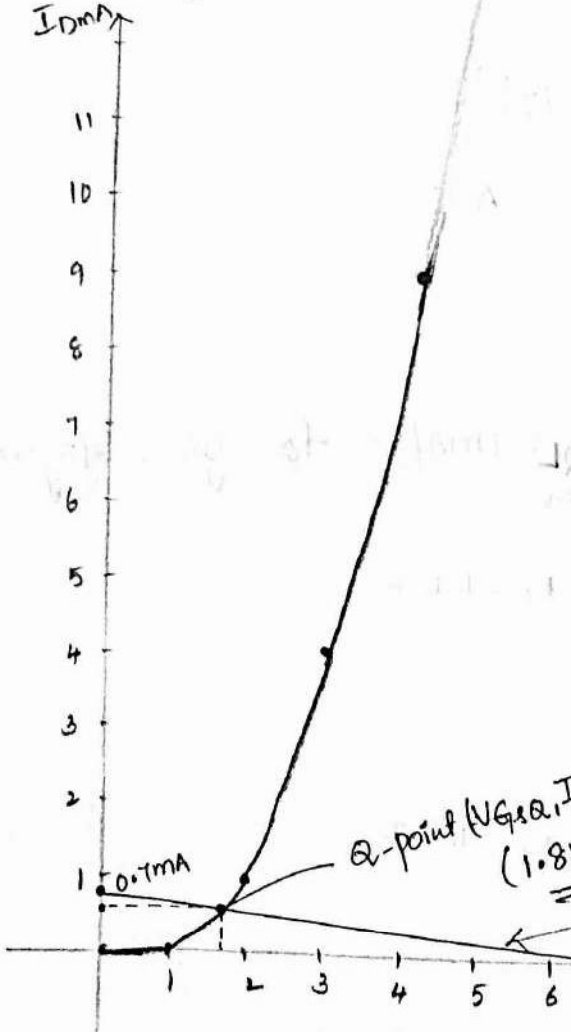
→ at $V_{GS} = 1V$, $I_D = 0$

→ at $V_{GS} = 2V$, $I_D = 1mA$

→ at $V_{GS} = 3V$, $I_D = 4mA$

→ at $V_{GS} = 4V$, $I_D = 9mA$

→ at $V_{GS} = 5V$, $I_D = 16mA$.



From given circuit

$$V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

$$= \frac{7M\Omega}{15M\Omega} \times 15$$

$$V_G = 7V$$

To find the DC load line, we have to write input KVL

$$-V_G + V_{GS} + I_D R_S = 0$$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

Load line eqn.

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In load line equation

when $I_D = 0$

$V_{GS} = V_G$

$V_{GS} = 7V$

when $V_{GS} = 0$

$0 = V_G - I_D R_S$

$V_G = I_D R_S$

$I_D = \frac{V_G}{R_S} = \frac{7}{10K\Omega}$

$I_D = 0.7mA$

Locate this two points on the plots.

from the plot Q-point $(V_{GSQ}, I_{DQ}) = (1.8V, 0.5mA)$

output KVL

$-15V + I_{DQ} R_D + V_{DSQ} + I_{DQ} R_S = 0$

$V_{DSQ} = 15V - I_{DQ}(R_D + R_S)$

$V_{DSQ} = 15V - 0.5\times10^{-3}(10K + 10K)$

$= 15V - 0.5\times10^{-3}(20\times10^{3})$

$V_{DSQ} = 15V - 10V$

$V_{DSQ} = 5V$

$\therefore (V_{DSQ}, I_{DQ}) = (5V, 0.5mA)$

Rajeev Gandhi Memorial College of Engineering and Technology
Autonomous
Department of Electronics and Communication Engineering

ACADEMIC YEAR	**: 2022-23**
SUBJECT	**: Electronic Devices and Circuits**
YEAR/SEM	**: II B.Tech I-Sem**
DEPARTMENT	**: Electronics & Communication Engineering**
FACULTY NAME	**: Mr. M. A. Vijay Kamalnath**

UNIT-I

SEMICONDUCTOR DIODES

- Semiconductors-Types
- PN junction materials
- Open junction PN junction
- Current components in a PN diode
- Diode equation and it's mathematical derivation
- Volt-ampere characteristics
- Energy band diagram of PN diode
- Temperature dependence of Volt-ampere characteristics
- Diode resistance (Static & Dynamic).
- Transition capacitance, Step and linear graded junction
- Diffusion capacitance
- Avalanche breakdown, V-I characteristics of Zener Diode, Zener breakdown.

Prepared
by
Mr. M.A Vijay Kamalnath,
Asst.Prof, Dept.of ECE,
RGMCET, Nandyal.

Introduction: Semiconductors are materials which have a conductivity between conductors (generally metals) and nonconductors or insulators (such as most ceramics).

- Semiconductors can be pure elements, such as silicon or germanium, or compounds such as gallium arsenide or cadmium selenide.

Types of Semiconductors:

Semiconductors can be classified as:

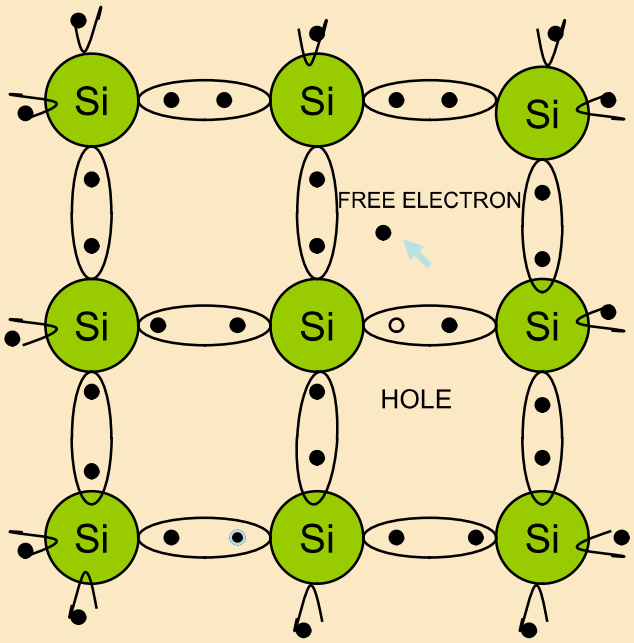
1. Intrinsic Semiconductor.

2. Extrinsic Semiconductor.

Extrinsic Semiconductors are further classified as:

a. n-type Semiconductors.
b. p-type Semiconductors.

Intrinsic Semiconductor



- Semiconductor in pure form is known as Intrinsic Semiconductor.
- Ex. Pure Germanium, Pure Silicon.
- At room temp. no of electrons equal to no. of holes.

Fig 1.

Intrinsic semiconductor energy band diagram

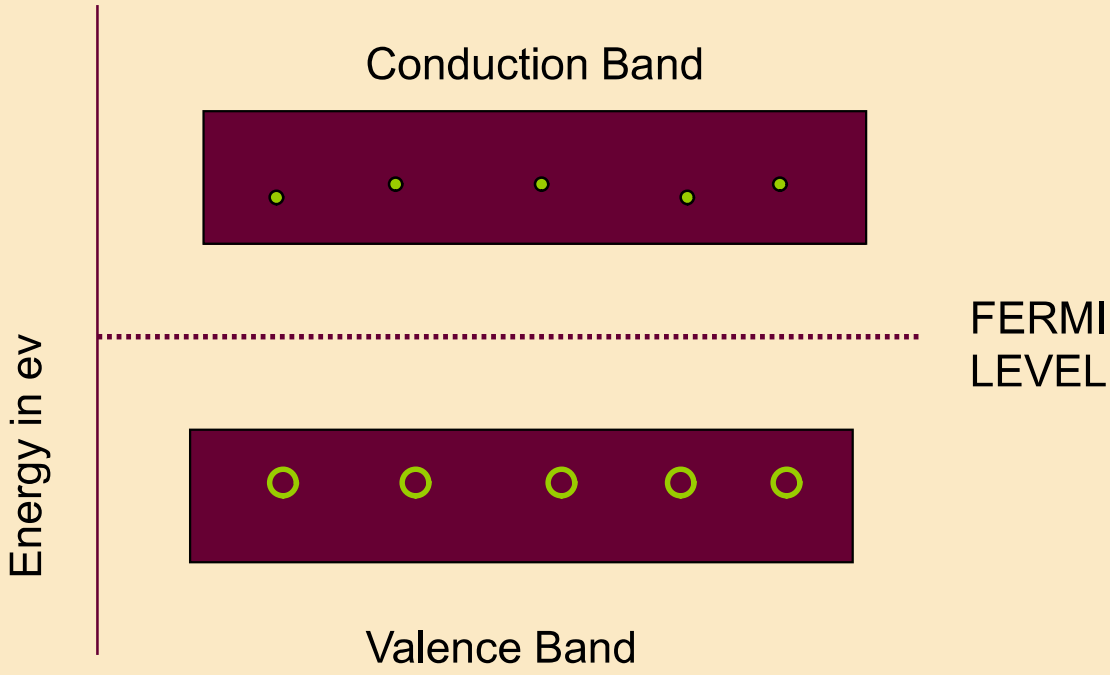


Fig 2.
Fermi level lies in the middle

Extrinsic Semiconductor

- When we add an impurity to pure semiconductor to increase the charge carriers then it becomes an Extrinsic Semiconductor.

- In extrinsic semiconductor without breaking the covalent bonds we can increase the charge carriers.

Comparison of semiconductors

Intrinsic Semiconductor	Extrinsic Semiconductor
1. It is in pure form.	1. It is formed by adding trivalent or pentavalent impurity to a pure semiconductor.
2. Holes and electrons are equal.	2. No. of holes are more in p-type and no. of electrons are more in n-type.

(Cont.,)

3. Fermi level lies in between valence and conduction Bands.	3. Fermi level lies near valence band in p-type and near conduction band in n-type.
4. Ratio of majority and minority carriers is unity.	4. Ratio of majority and minority carriers are equal.

Comparison between n-type and p-type semiconductors

N-type

- Pentavalent impurities are added.
- Majority carriers are electrons.
- Minority carriers are holes.
- Fermi level is near the conduction band.

P-type

- Trivalent impurities are added.
- Majority carriers are holes.
- Minority carriers are electrons.
- Fermi level is near the valence band.

N-type Semiconductor

- When we add a pentavalent impurity to pure semiconductor we get n-type semiconductor.

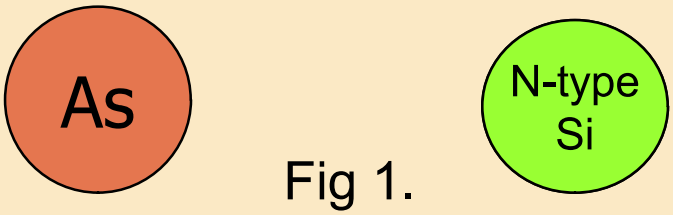


Fig 1.

N-type Semiconductor

- Arsenic atom has 5 valence electrons.
- Fifth electron is superfluous, becomes free electron and enters into conduction band.
- Therefore pentavalent impurity donates one electron and becomes positive donor ion. Pentavalent impurity known as donor.

P-type Semiconductor

- When we add a Trivalent impurity to pure semiconductor we get p-type semiconductor.

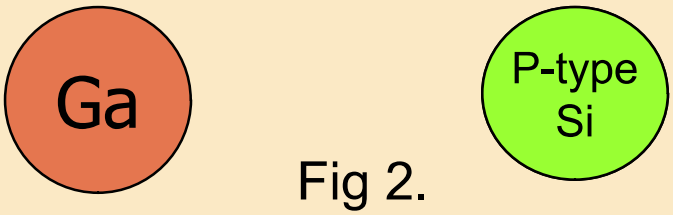


Fig 2.

P-type Semiconductor

- Gallium atom has 3 valence electrons.
- It makes covalent bonds with adjacent three electrons of silicon atom.
- There is a deficiency of one covalent bond and creates a hole.
- Therefore trivalent impurity accepts one electron and becomes negative acceptor ion. Trivalent impurity known as acceptor.

Carriers in P-type Semiconductor

- In addition to this, some of the covalent bonds break due temperature and electron hole pairs generates.
- Holes are majority carriers and electrons are minority carriers.

P and N type Semiconductors

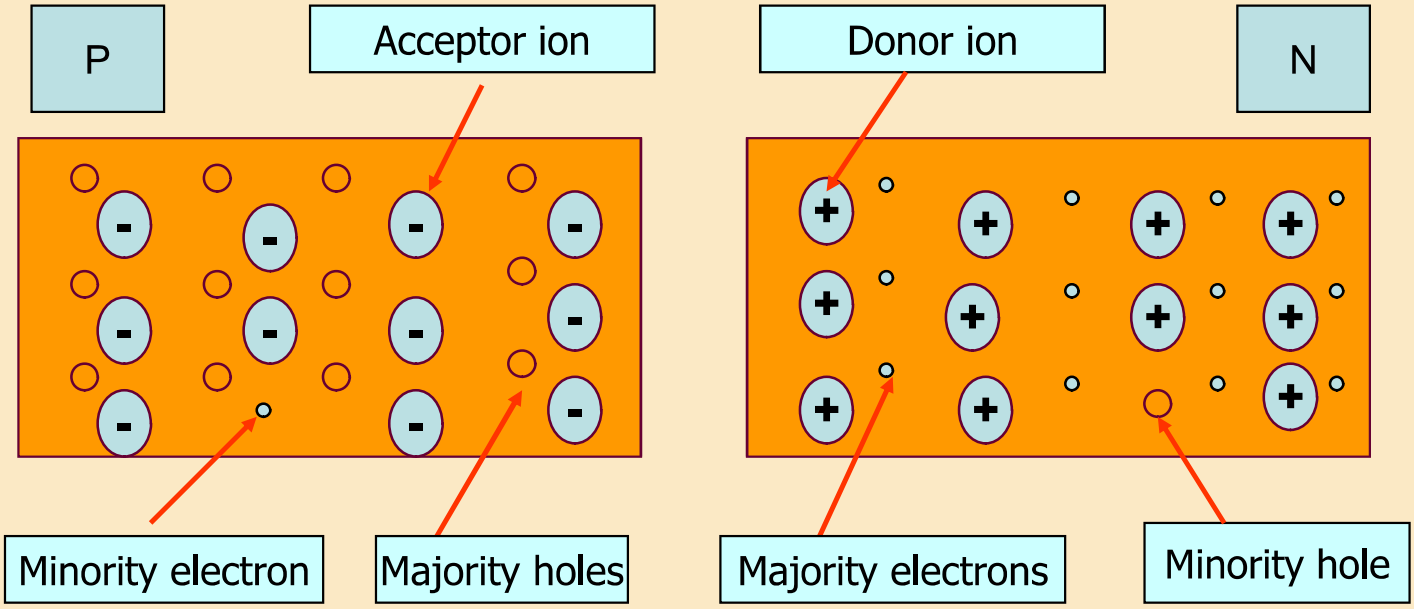


Fig 3.

Comparison of semiconductors

Intrinsic Semiconductor	Extrinsic Semiconductor
1. It is in pure form.	1. It formed by adding trivalent or pentavalent impurity to a pure semiconductor.
2. Holes and electrons are equal.	2. No. of holes are more in p-type and no. of electrons are more in n-type.
3. Fermi level lies in between valence and conduction Bands.	3. Fermi level lies near valence band in p-type and near conduction band in n-type.

Conduction in Semiconductors

Conduction is carried out by means of

1. Drift Process.

2. Diffusion Process.

Drift process

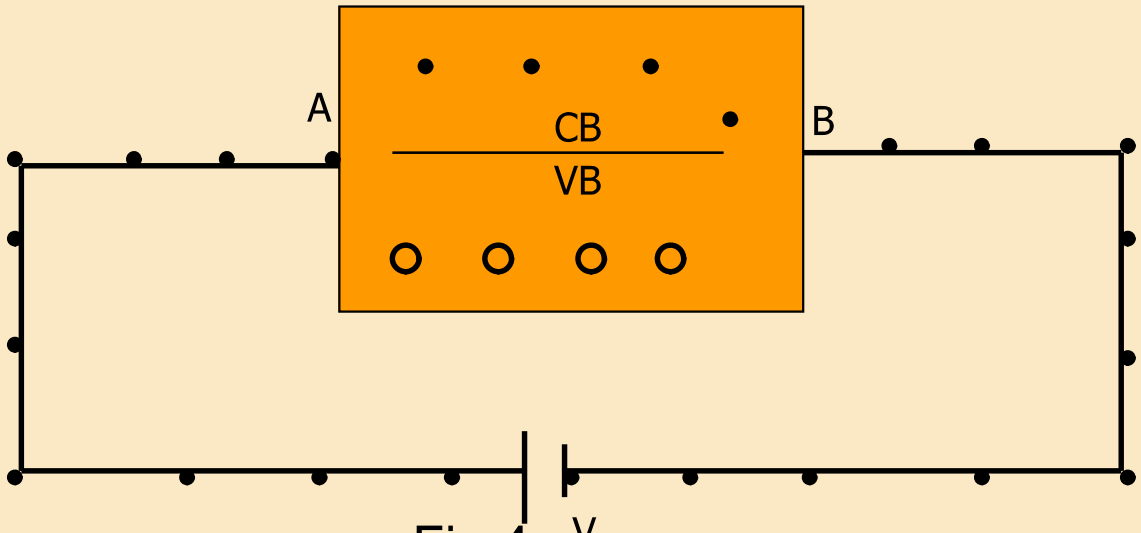


Fig 4.

- Electrons move from external circuit and in conduction band of a semiconductor.
- Holes move in valence band of a semiconductor.

Diffusion process

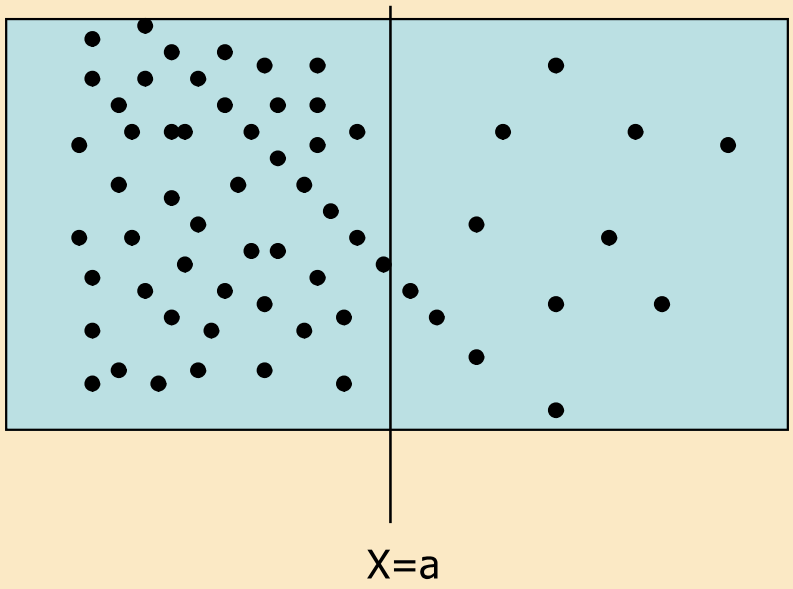


Fig 5.

- Moving of electrons from higher concentration gradient to lower concentration gradient is known as diffusion process.

P and N type Semiconductors

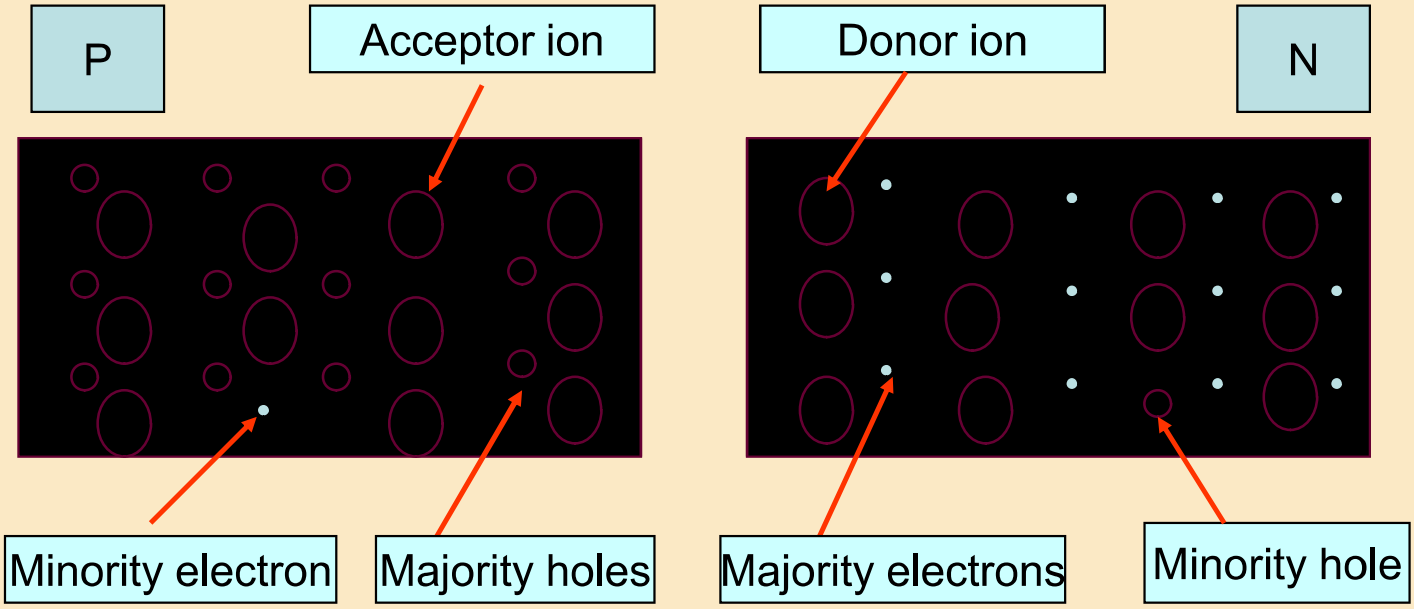


Fig 1.

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Formation of pn diode

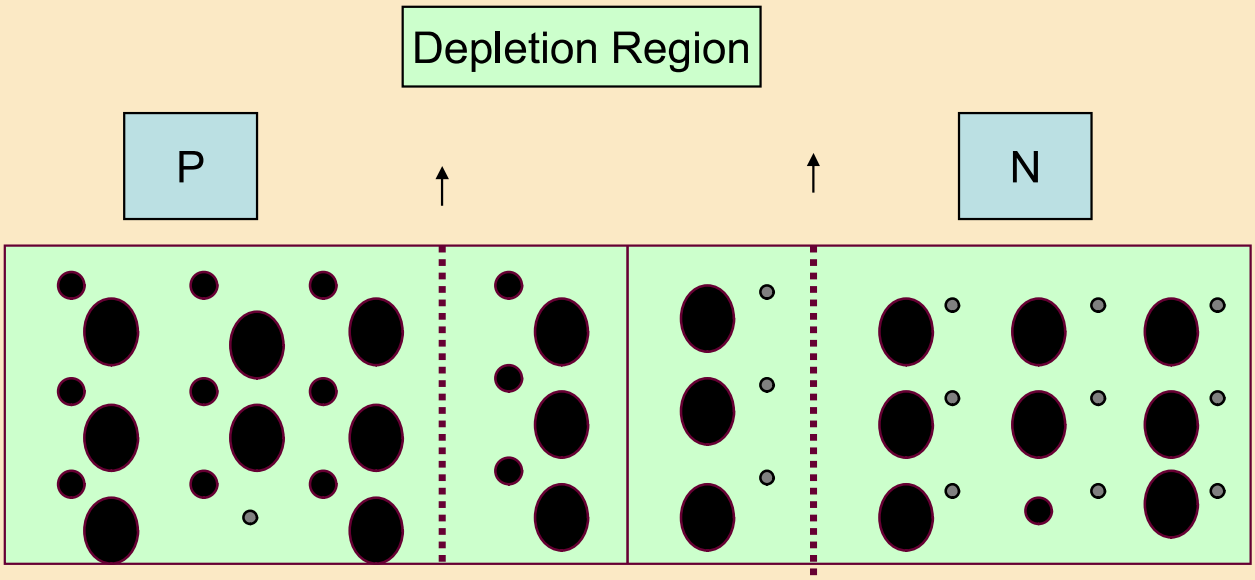
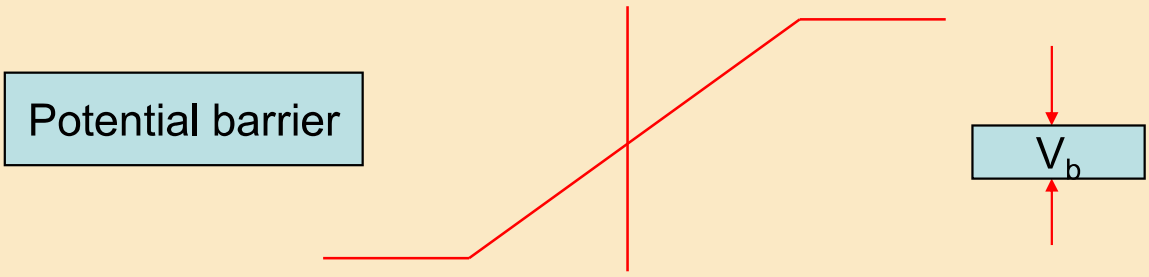


Fig 2.



20

Formation of pn diode

- A P-N junction is formed , if donor impurities are introduced into one side ,and acceptor impurities Into other side of a single crystal of semiconductor

- Initially there are P type carriers to the left side of the junction and N type carriers to the right side as shown in figure 1

- On formation of pn junction electrons from n-layer and holes from p-layer diffuse towards the junction and recombination takes place at the junction.

- And leaves an immobile positive donor ions at n-side and negative acceptor ions at p-side.

Formation of pn diode

- A potential barrier develops at the junction whose voltage is 0.3V for germanium and 0.7V for silicon.

- Then further diffusion stops and results a depletion region at the junction.

Depletion region

- Since the region of the junction is depleted of mobile charges it is called the depletion region or the space charge region or the transition region.

- The thickness of this region is of the order of 0.5 micrometers

Circuit symbol of pn diode

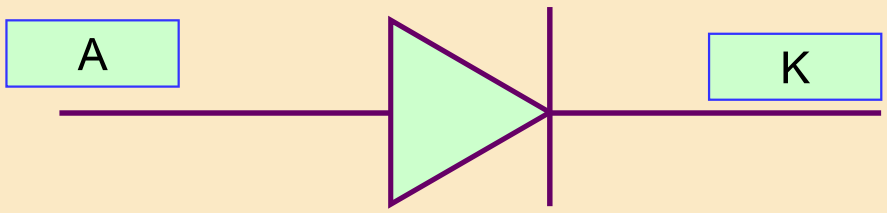


Fig 3.

- Arrow head indicates the direction of conventional current flow.

P-N Junction Diode- Forward Biasing

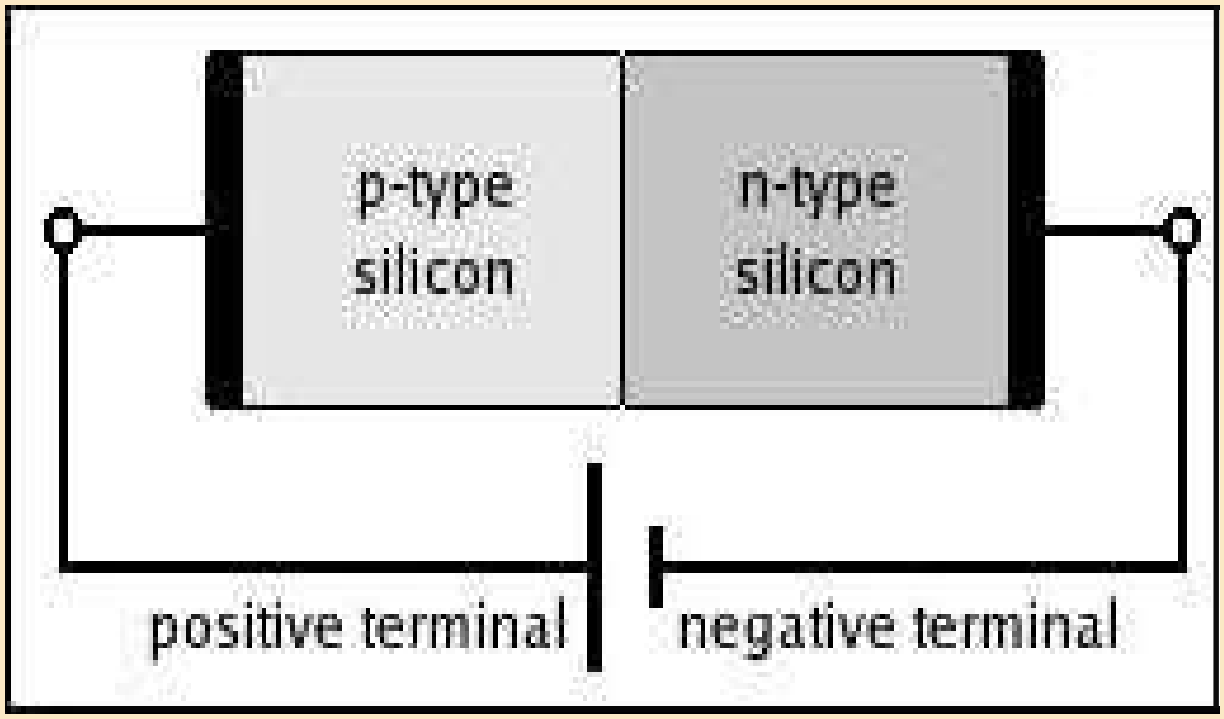
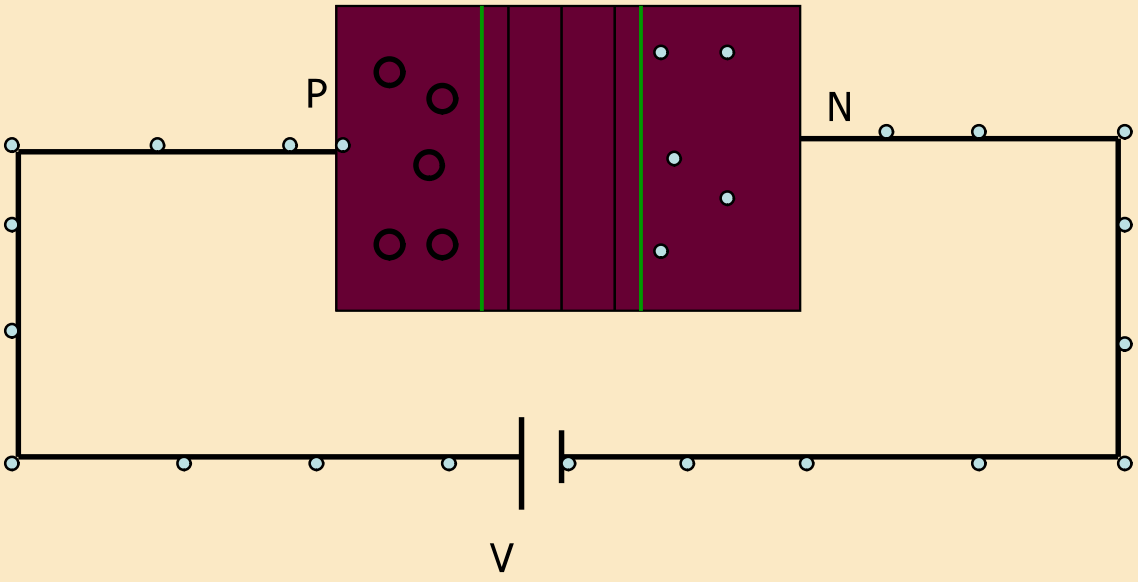


Fig. 1 P-N junction with FB

Working of P-N Junction under FB



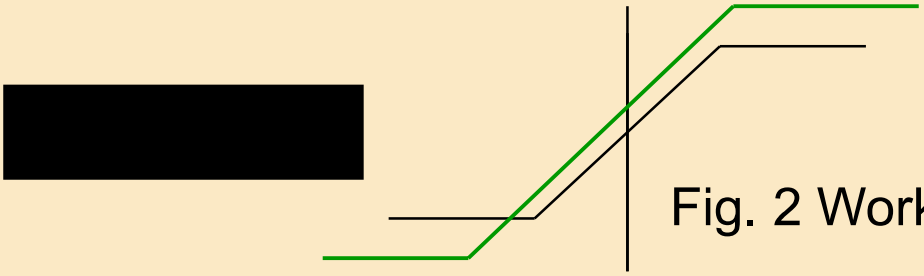


Fig. 2 Working of P-N junction

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Forward Bias

- An ext. Battery applied with +*ve* on *p*-side, −*ve* on *n*-side.
- The holes on *p*-side repelled from the +*ve bias,* the electrons on *n*- side repelled from the −*ve bias .*
- The majority charge carriers driven towards the junction.
- This results in reduction of depletion layer width and barrier potential.
- As the applied bias steadily increased from zero onwards the majority charge carriers attempts to cross junction.

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- Holes from *p*-side flow across to the −*ve terminal* on the *n*-side, and electrons from *n*-side flow across to the +*ve terminal* on the *p*-side.

- As the ext. bias exceeds the Junction barrier potential (*0.3 V* for *Germanium*, *0.7 V* for *Silicon*) the current starts to increase at an exponential rate.

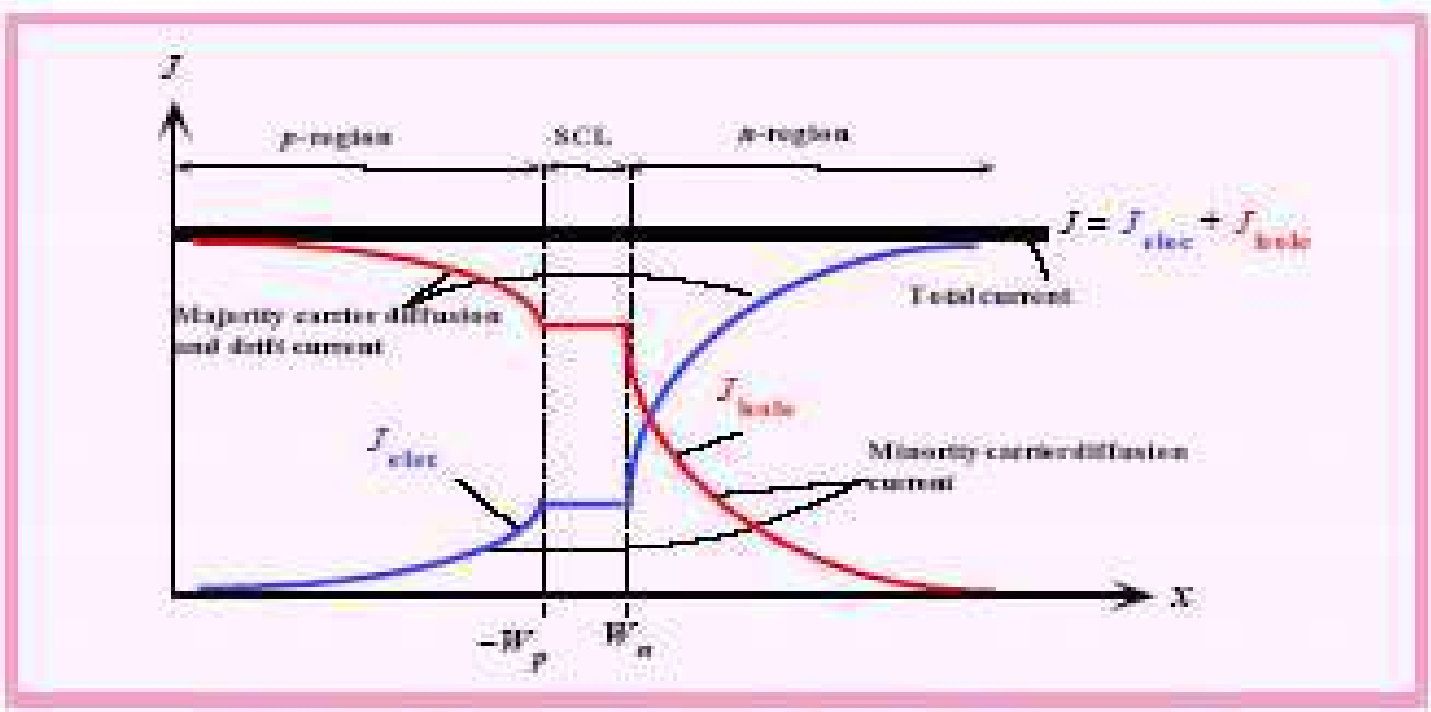
- Now, a little increase in forward bias will cause steep rise in majority current.

- The device simply behaves as a low resistance path.

Features:

- Behaves as a low resistor.
- The current is mainly due to the flow of majority carriers across the junction.
- Potential barrier, and the depletion layer is reduced

Current components



- The total current anywhere in the device is constant.
- Just outside the depletion region it is due to the diffusion of minority carriers.

Fig. 3 Current components

P-N Junction Diode- Reverse Biasing

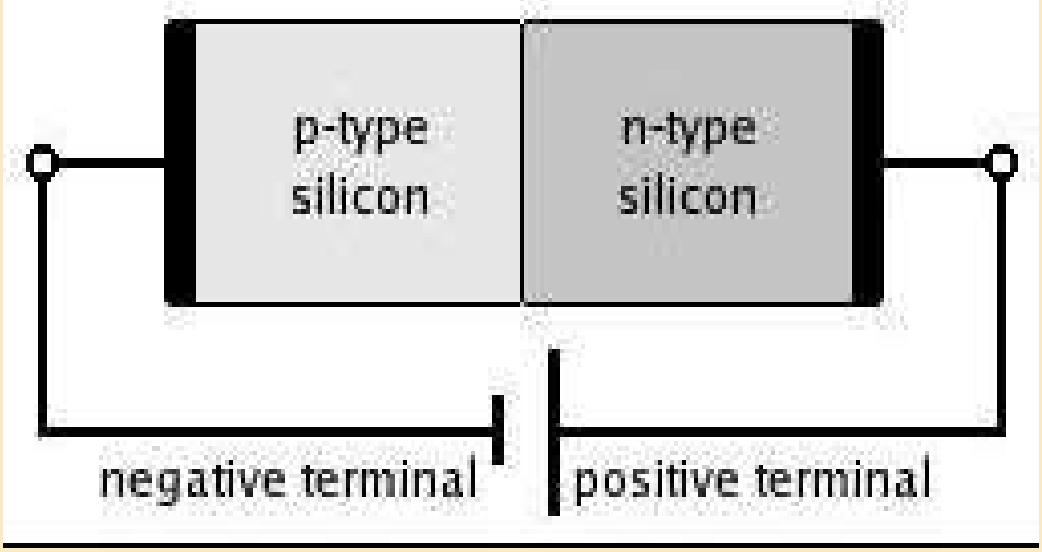


Fig.1 P-N Junction Diode with Reverse bias (RB)

P-N Junction working under reverse bias

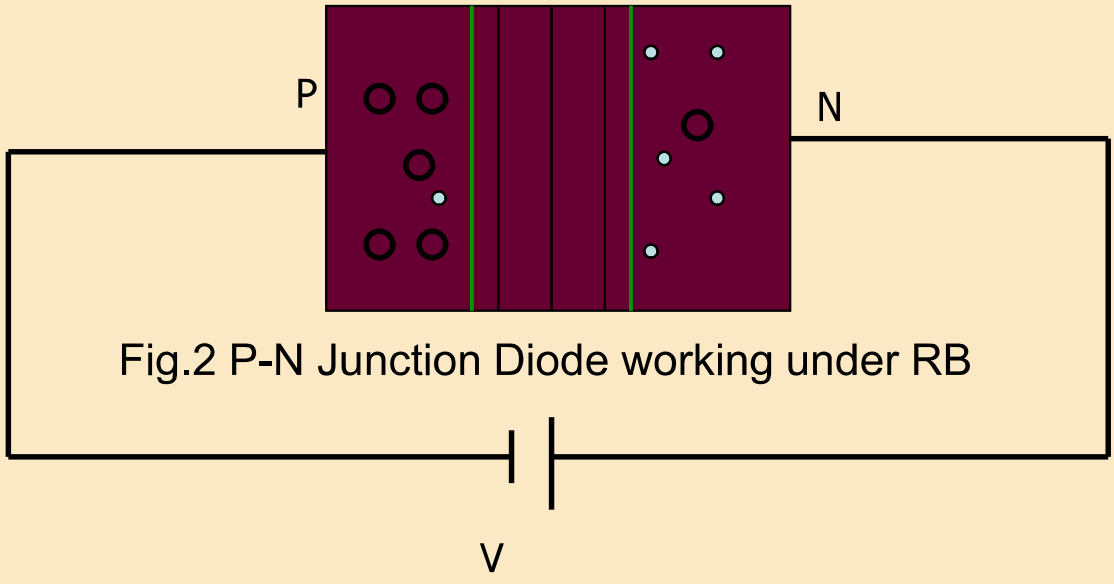
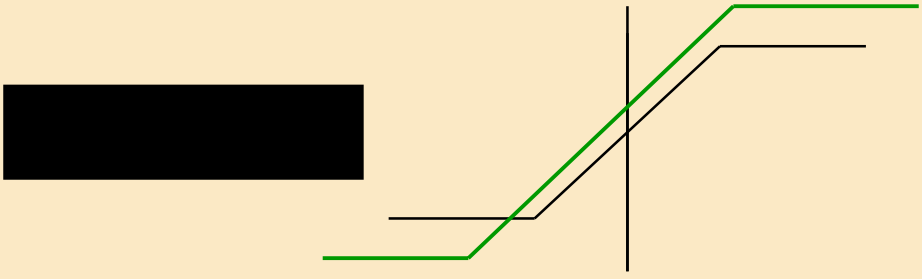


Fig.2 P-N Junction Diode working under RB



P-N Junction Diode- Reverse Bias

- External bias voltage applied with +*ve* on *n*-side, −*ve* on p-side.
- This RB bias aids the internal field.
- The majority carriers *i.e.* holes on *p*-side, the electrons on *n*-side attracted by the negative and positive terminal of the supply respectively.
- This widens the depletion layer width and strengthens the barrier potential.

- Few hole-electron pairs are created due to thermal agitation (minority carriers).
- As a result small current flows across the junction called as reverse saturation current I_0 (uA for Germanium, nA for Silicon).
- Behaves as a high impedance element.

- Further rise in reverse bias causes the collapse of junction barrier called breakdown of the diode.

- This causes sudden increase in flow of carriers across the junction and causes abrupt increase in current.

P-N JUNCTION

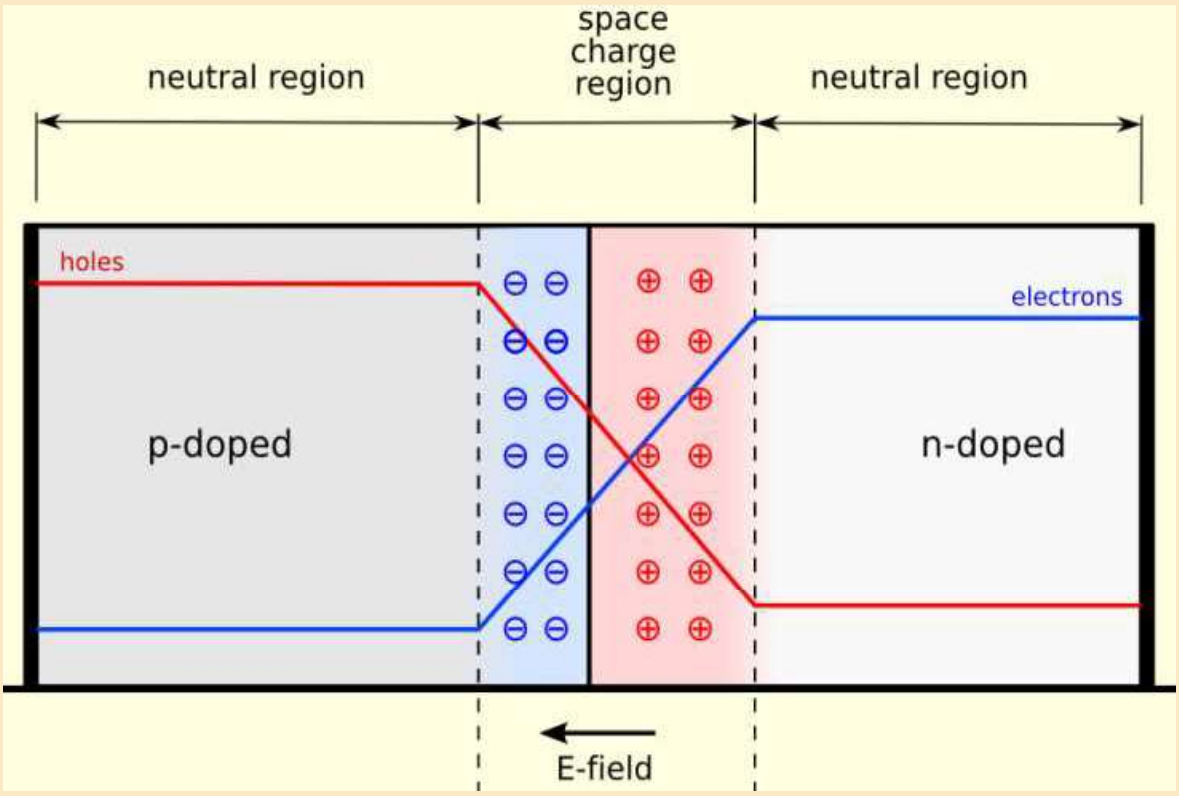


Fig 1.

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JUNCTION PROPERTIES

1. The junction contains immobile ions *i.e.* this region is depleted of mobile charges.

2. This region is called the *depletion region*, the *space charge region*, or *transition region.*

3. It is in the order of *1 micron width.*

1. The cut-in voltage is *0.3v* for *Ge, 0.6v* for *Si.*

(Contd..)

5. The reverse saturation current doubles for every *10 degree Celsius* rise in temperature.

6. Forward resistance is in the order *ohms*, the reverse resistance is in the order *mega ohms.*

7. The Transition region increases with reverse bias this region also considered as a variable capacitor and known as *Transition capacitance*

V-I Characteristics of P-N Junction Diode

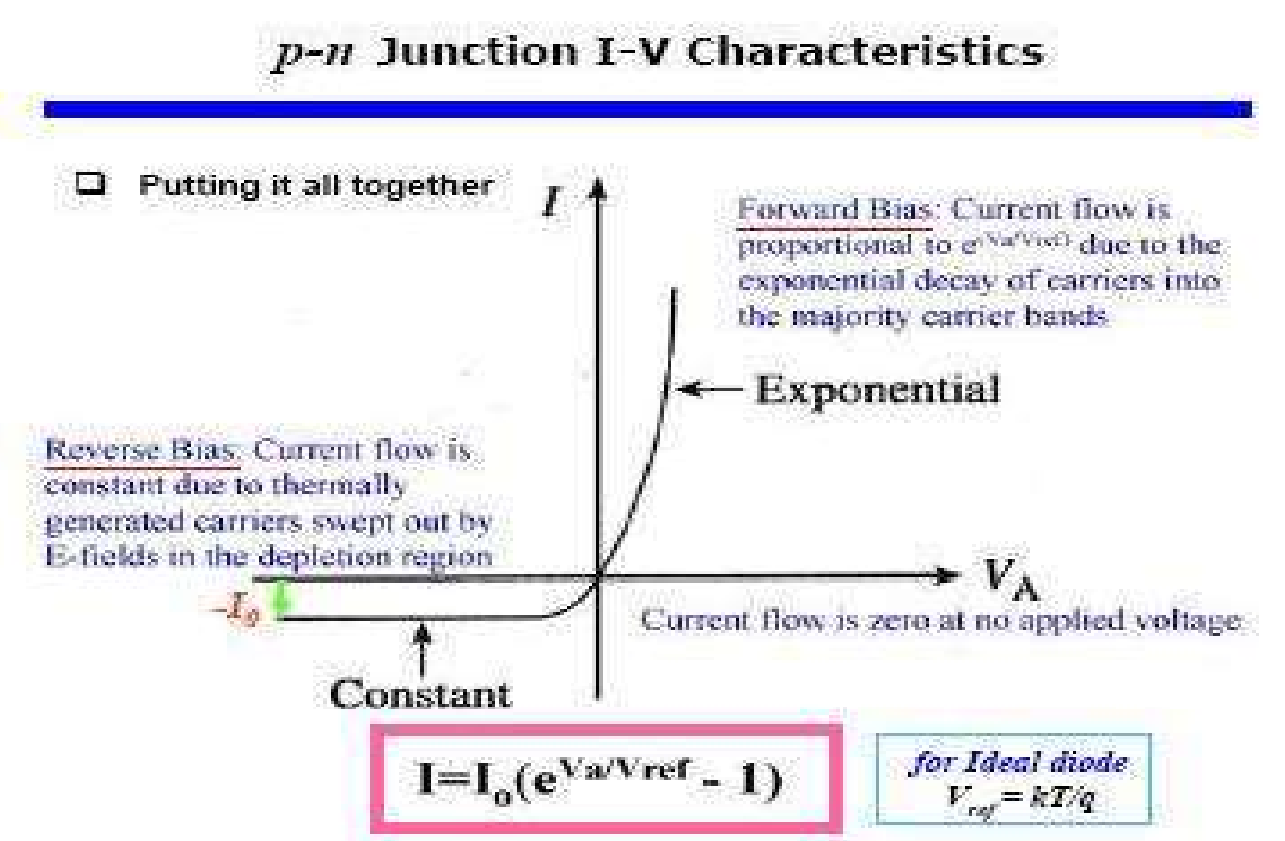

Fig 2.

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(Contd…)

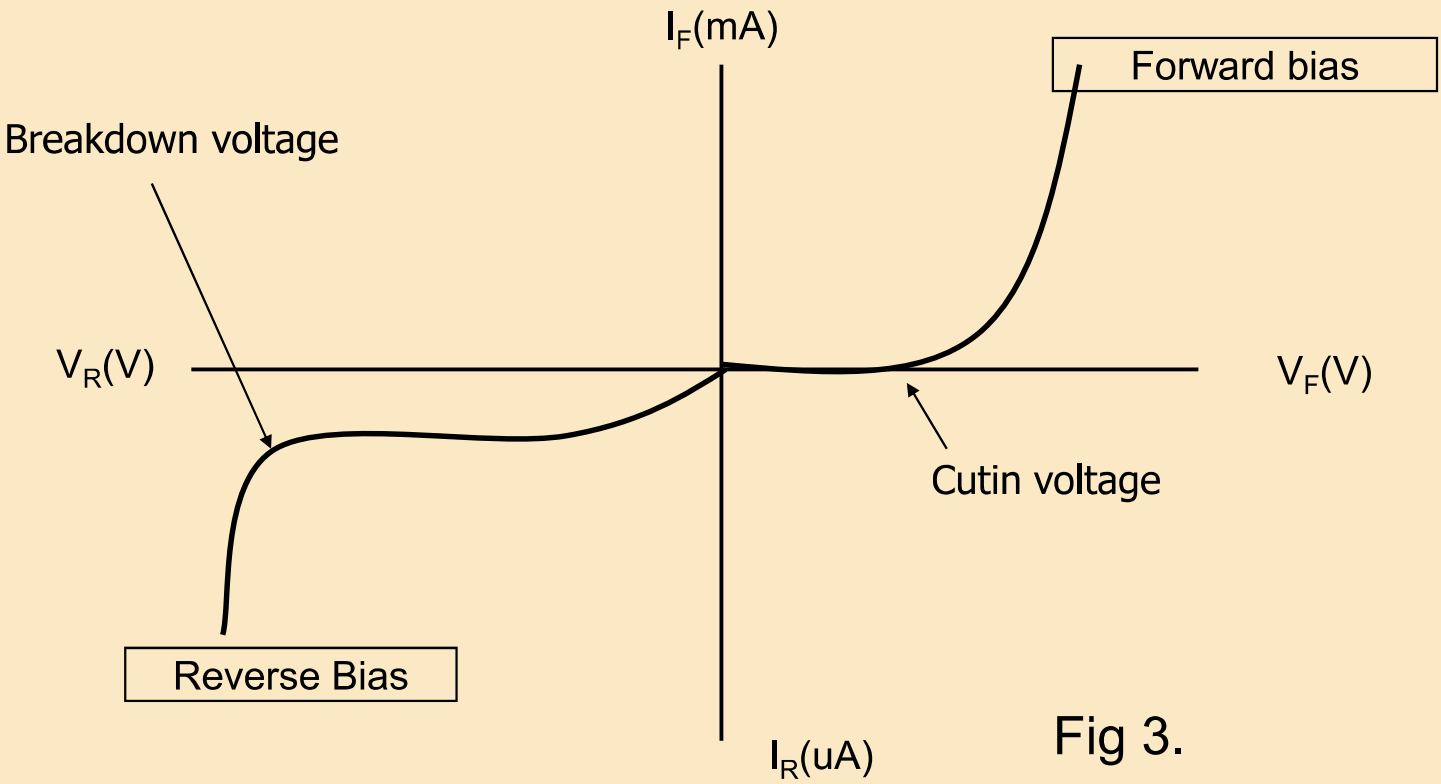
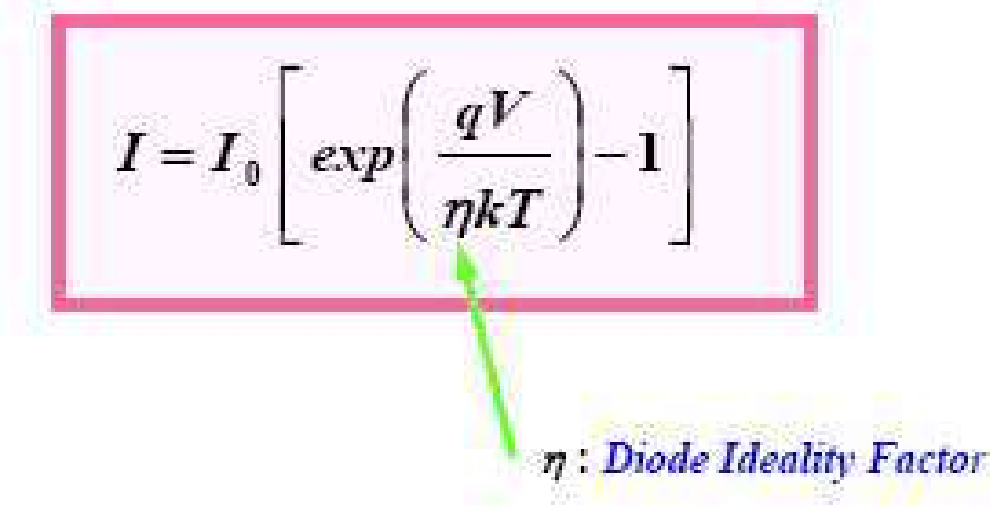

I_F(mA)
Forward bias
Breakdown voltage
V_R(V)
V_F(V)
Cutin voltage
Reverse Bias
I_R(uA)

Fig 3.

- Diode Equation



Diode Current

The expression for Diode current is

$$I = I_0\left(e^{\frac{V}{nV_t}} - 1\right)$$

Where $I_{o=}$Reverse Saturation current.

V=Applied Voltage.

V_t=Volt equivalent temperature=T(K)/11600.

n=1 for germanium and 2 for silicon.

Resistance calculation

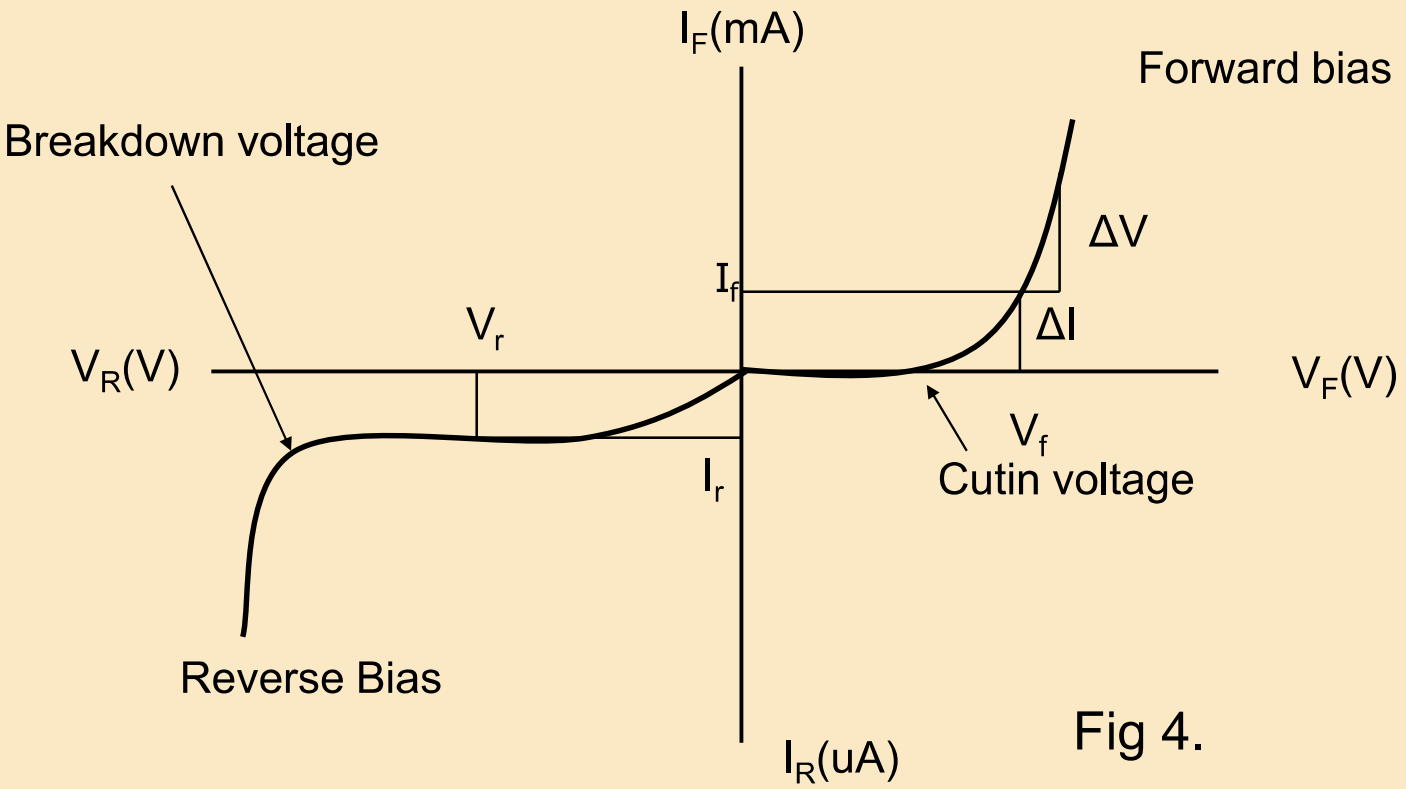


Fig 4.

Resistance calculation

Forward Resistance

1. Dynamic resistance (r_f)= $\Delta V / \Delta I$ ..ohms.

   Where ΔV, ΔI are incremental voltage and current values on Forward characteristics.

2. Static resistance (R_f)= V_f / I_f …ohms.

   Where V_f, I_f are voltage and current values on Forward characteristics.

(Contd..)

Reverse Resistance:

Static resistance = V_r / I_r …ohms

Where V_r, I_r are voltage and current values on Reverse characteristics.

Diode-Variants

- Rectifier diodes: These diodes are used for
  AC to DC conversion
  Over voltage protection.
- Signal diodes : Detection of signals in AM/FM Receivers.
- Zener diode: Voltage Regulation purpose.
- Varactor diode for variable capacitance
  Electronic tuning commonly used in TV receivers.

(contd…)

- Light Emitting Diodes (LED) :
  Display
  Light source in Fiber optic comm.
- Photo diodes : Light detectors in Fiber optic comm.
- Tunnel diode: Negative resistance for Microwave oscillations
- Gunn diode :Microwave Oscillator.
- Shottkey diode: High speed Logic circuits

Semiconductor diodes

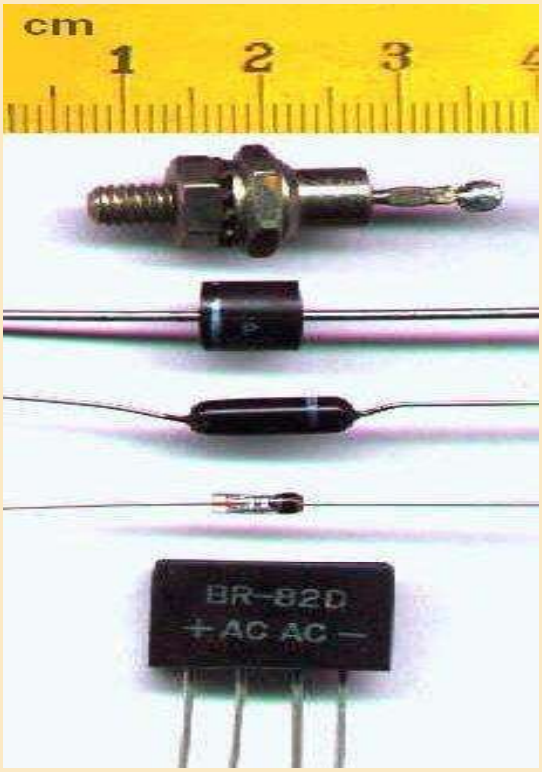
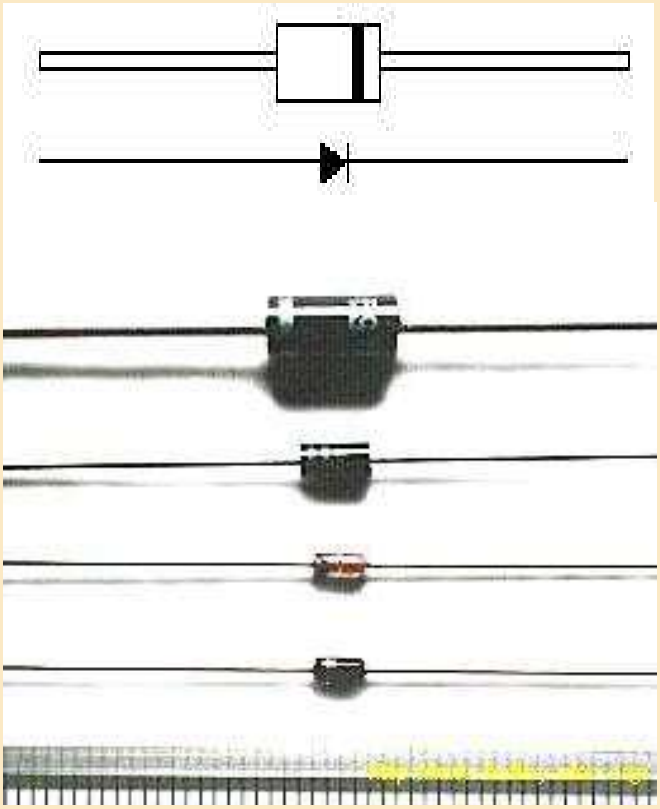


Fig. 1 Diode variants



Visual - 1

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Diode numbering

First Standard (EIA/JEDEC):

In this approach the semiconductor devices are identified with the no of junctions.

1N series : single junction devices such as
P-N junction Diode. *e.g.*: 1N4001,1N3020.

2N series : Two junction devices such as Transistors. *e.g.*: 2N2102,1N3904.

EIA= Electronic Industries association
JDEC=Joint Electron Engineering Council.

(contd…)

Second Standard

In this method devices given with alpha-numeric codes. And each alphabet has a specific information which tells about application, material of fabrication.

First Letter: material

A=Germanium.

B=Silicon.

C=Gallium arsenide.

R=compound material (e.g. Cadmium sulphide).

(contd..)

Second Letter: For device type and function

A= Diode.
B= Varactor.
C= AF Low Power Transistor.
D= AF Power Transistor.
E= Tunnel Diode.
F= HF Low Power Transistor.
L= HF Power Transistor.
S= Switching Transistor.
R= Thyristor/Triac.
Y= power device.
Z= Zener.

(contd..)

Third Letter: Tolerance

A :±1%.
B :±2%.
C :±5%.
D :±10%.

Examples:

1. AC128: Germanium AF low power Transistor.
2. BC149: Silicon AF low power Transistor.

(contd…)

3. BY114 : Silicon Crystal diode.
4. BZC 6.3 : Silicon Zener diode Vz= 6.3v.
5. BY127 : Silicon rectifier diode.

Lead Identification:

Commonly the cathode is identified with

a band marking

a dot marking or

with a rounded edge.

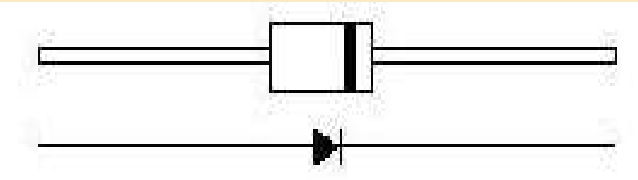


Fig. 2 Diode lead identification

Specifications

1. Peak inverse voltage (*PIV*)

   It is the max. voltage a diode can survive under reverse bias.

2. Max. Forward current (I_f).

   It is the maximum current that can flow through the diode under forward bias condition.

3. Reverse saturation current (I_o).

   Amount of current flow through the diode under reverse bias condition.

Specifications (contd…)

4. Max power rating (P_{max}).
   Maximum power that can be dissipated in the diode.

5. Operating Temperature (^oC).
   The range of temperature over which diode can be operated.

Applications

1. Rectifier circuits for AC-DC Conversion.
2. Over voltage protection circuits.
3. Limiter, Clamping, voltage doublers circuits.
4. Signal detector in AM/FM Receivers.
5. In transistor bias compensation networks.
6. Digital Logic gates.

ZENER DIODE

- Invented by “C.Zener”.
- Heavily doped diode.
- Thin depletion region.
- Sharp break down voltage called zener voltage V_z.
- Forward characteristics are same as pn diode characteristics.

CIRCUIT SYMBOL

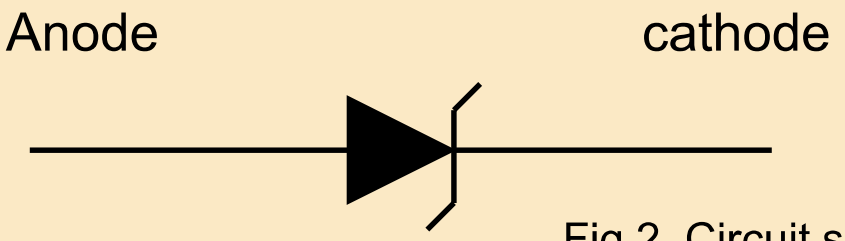


Fig 2. Circuit symbol of zener diode

- Arrow head indicates the direction of conventional current flow.

- “Z” symbol at cathode is a indication for zener diode.

PHOTOS OF ZENER DIODES

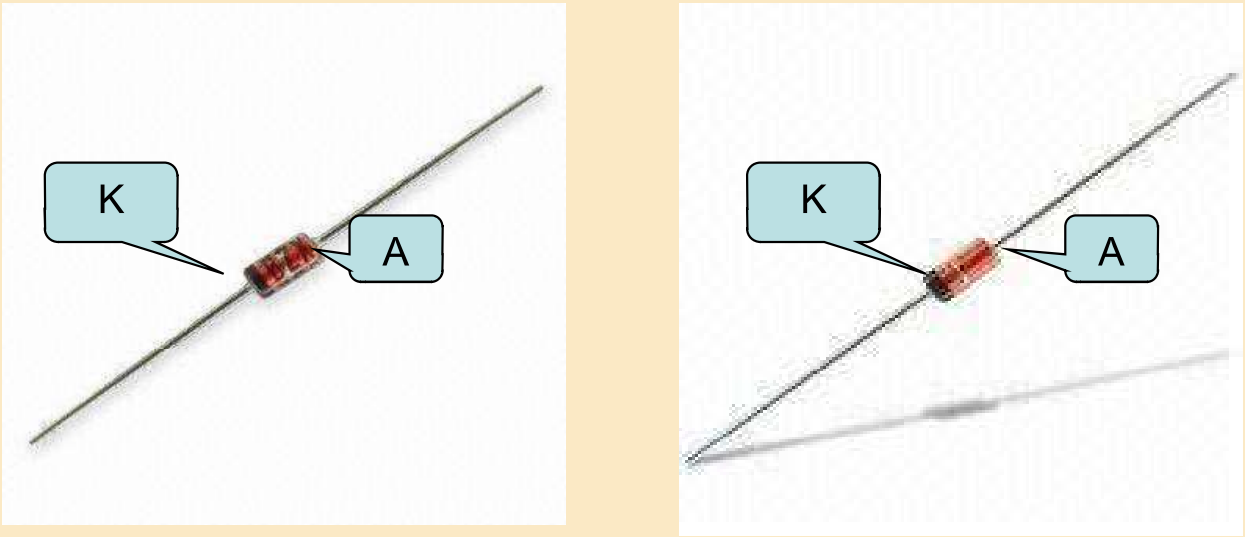


Fig 3. photos of Zener Diodes

PHOTOS OF ZENER DIODES

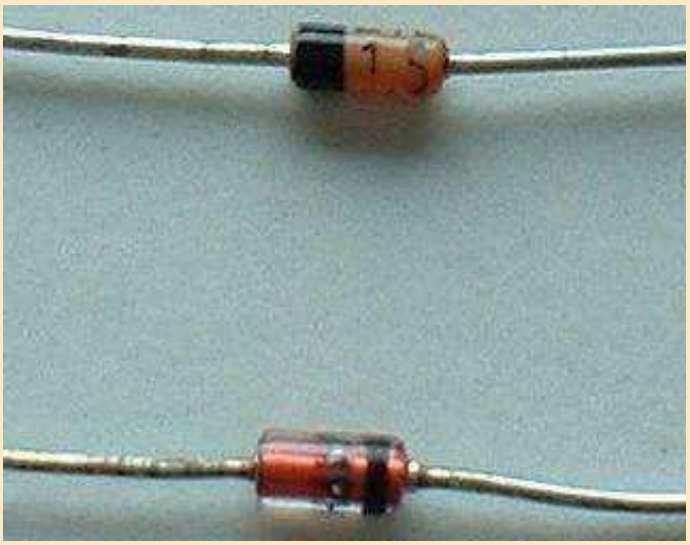
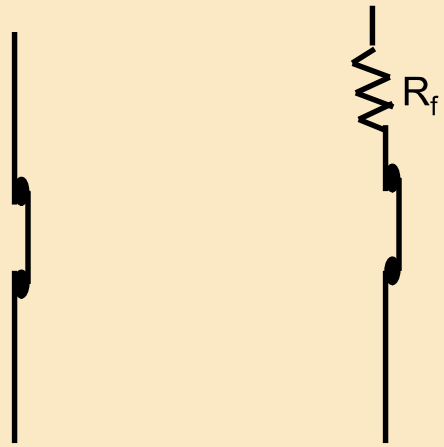


Fig. 4. Fig 3. photos of Zener Diodes

EQUIVALENT CIRCUIT

In forward bias



Ideal

Practical

Acts as a closed switch.

Fig 5. Equivalent circuit in forward bias

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EQUIVALENT CIRCUIT

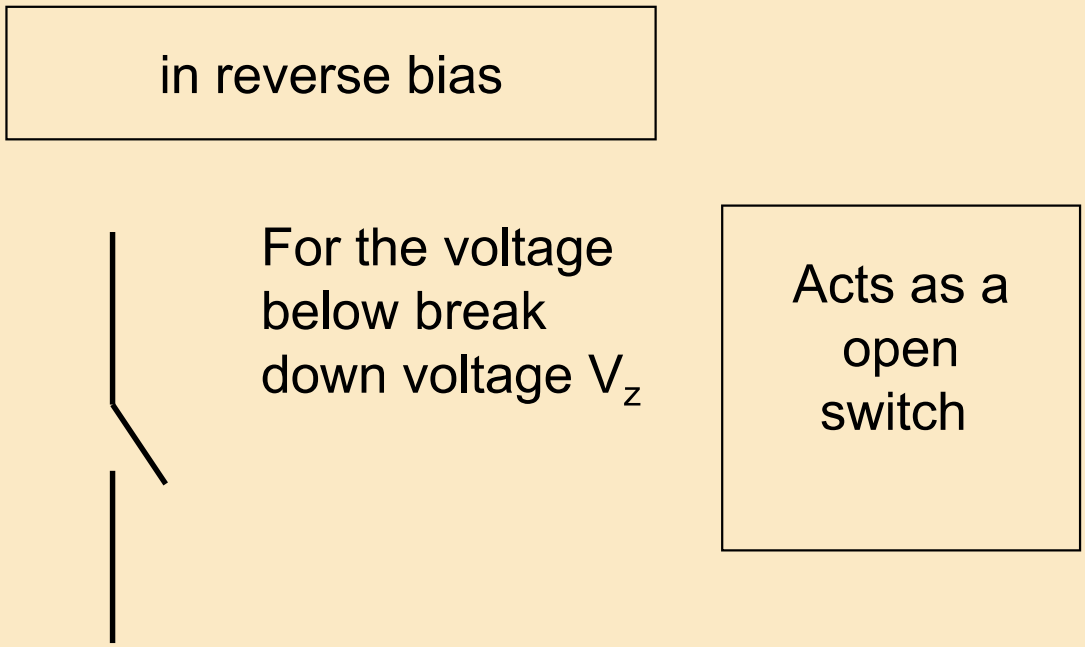

Fig 6. Equivalent circuit in reverse bias for voltage below V_z

EQUIVALENT CIRCUIT

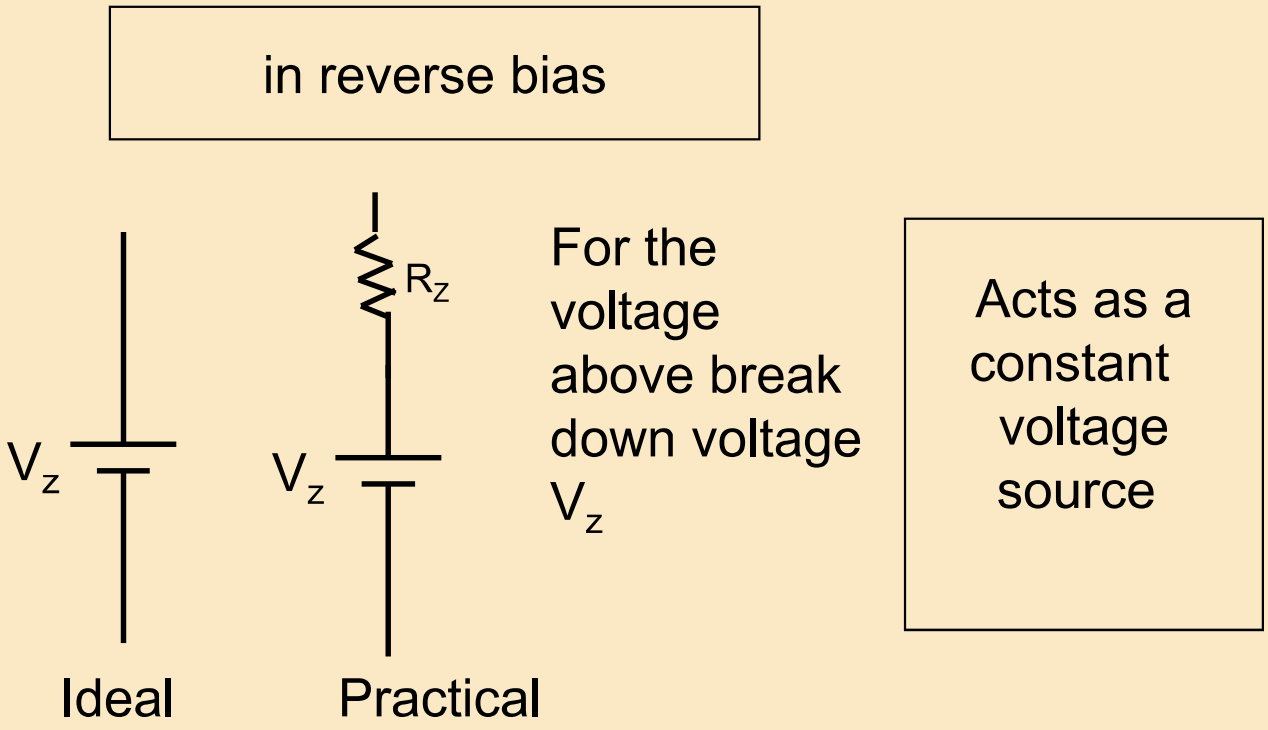

Fig 7. Equivalent circuit of zener diode for voltage above V_z

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ZENER BREAK DOWN

- Break down in Zener Diode.
- In heavily doped diode field intensity is more at junction.
- Applied reverse voltage setup strong electric field.
- Thin depletion region in zener diode.

ZENER BREAK DOWN MECHANISM

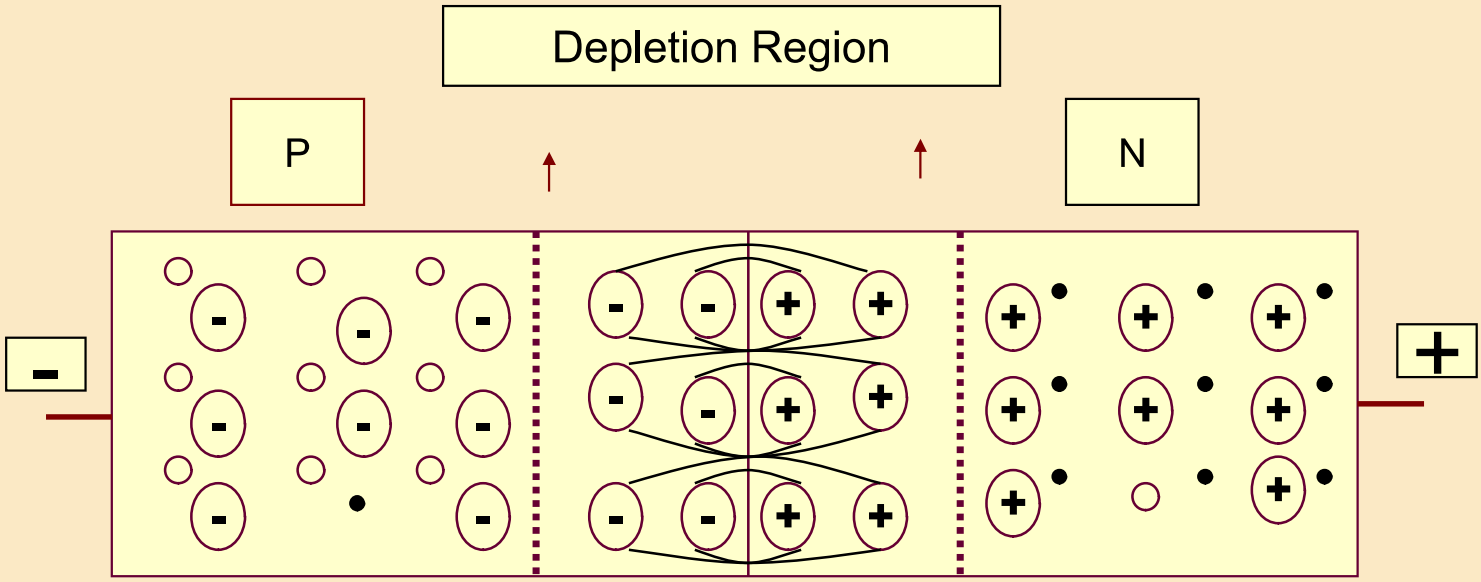

Fig 1. Zener Break down Mechanism animated

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ZENER BREAK DOWN MECHANISM

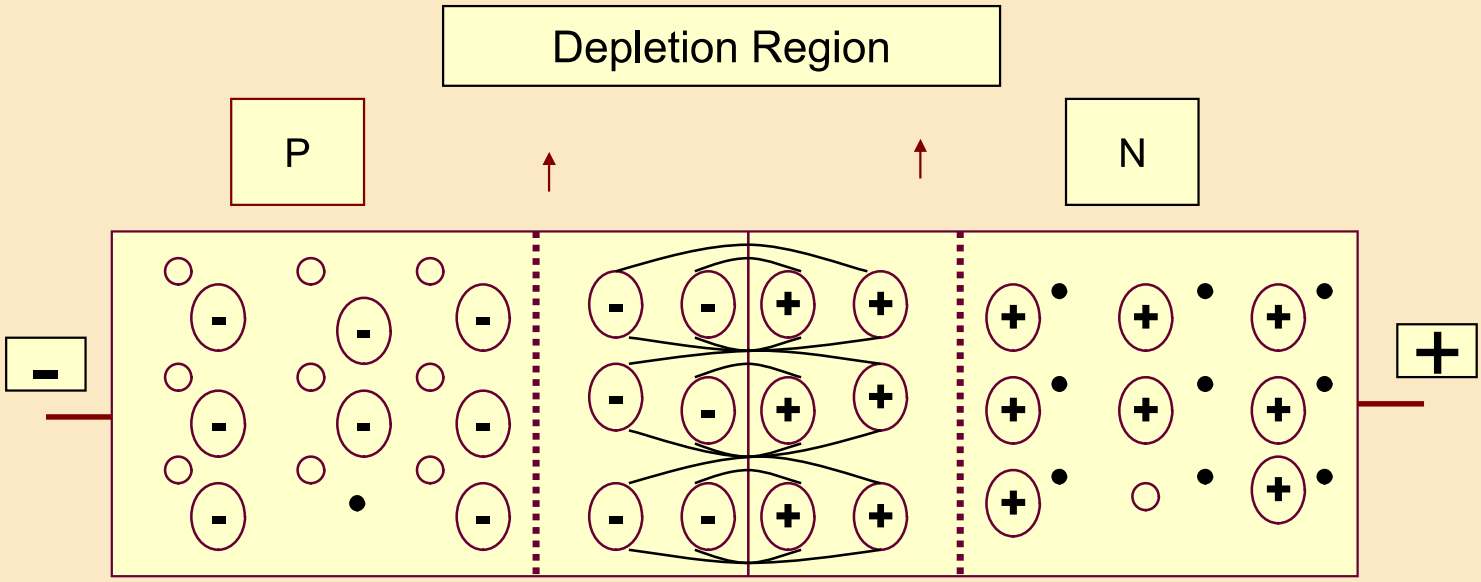

Fig 2. Zener Break down mechanism

ZENER BREAKDOWN

- Applied field enough to break covalent bonds in the depletion region.
- Extremely large number of electrons and holes results.
- Produces large reverse current.
- Known as Zener Current I_Z.

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ZENER BREAK DOWN

- This is known as “Zener Break down”.

- This effect is called “Ionization by an Electric field”.

AVALANCHE BREAK DOWN

- Break down in PN Diode.
- In lightly doped diode field intensity is not strong to produce zener break down.
- Depletion region width is large in reverse bias.

AVALANCHE BREAKDOWN MECHANISM

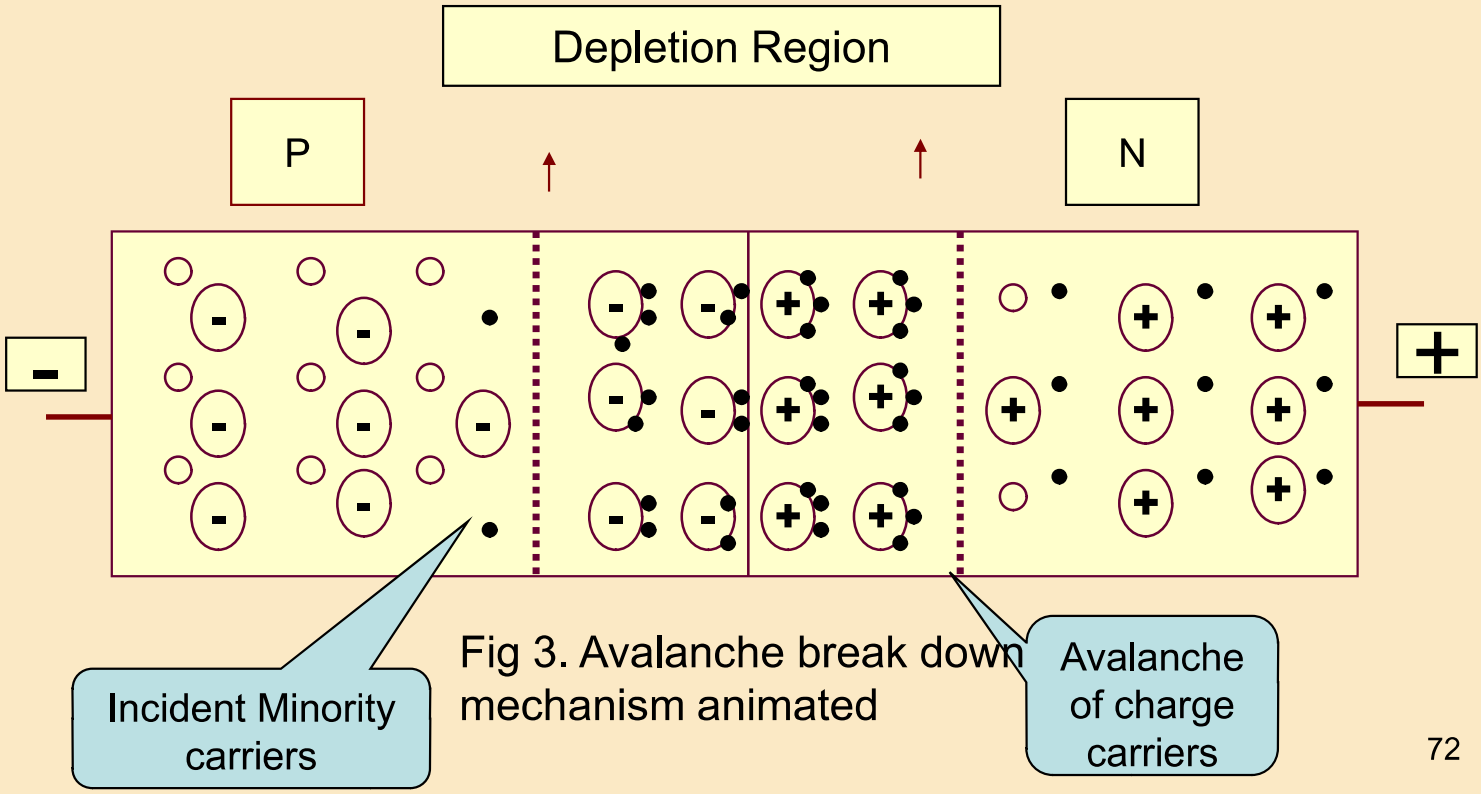


Fig 3. Avalanche break down mechanism animated

AVALANCHE BREAKDOWN MECHANISM

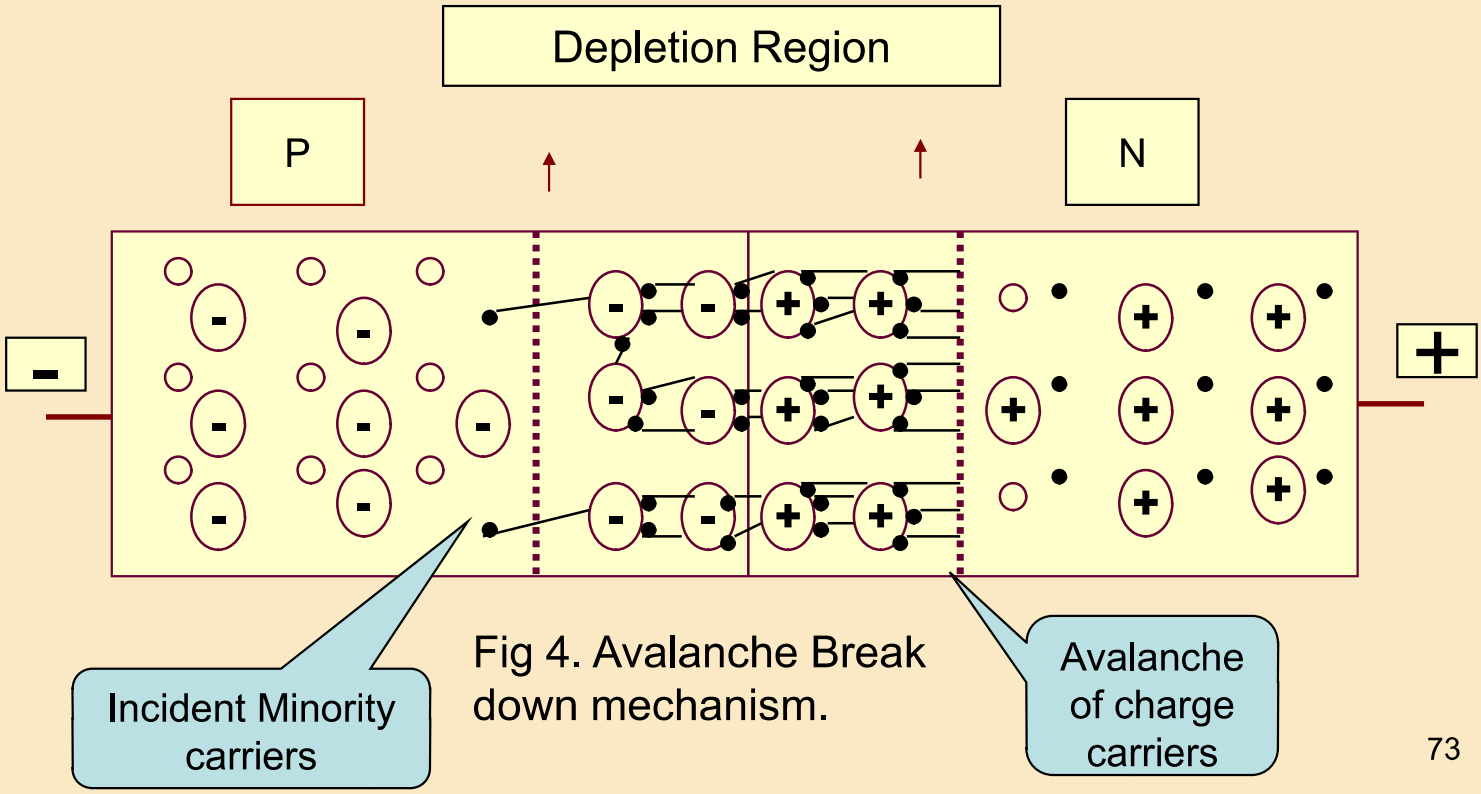


Fig 4. Avalanche Break down mechanism.

AVALANCHE BREAK DOWN

- Velocity of minority carriers increases with reverse bias.

- Minority carriers travels with great velocity and collides with ions in depletion region.

AVALANCHE BREAK DOWN

- Many covalent bonds breaks and generates more charge carriers.
- Generated charge carriers again collides with covalent bonds and again generates the carriers

AVALANCHE BREAK DOWN

- Chain reaction established.
- Creates large current..
- This effect is known as “Ionization by Collision”.
- Damages the junction permanently.

Differences between Zener and Avalanche break downs.

1. Occurs in heavily doped diodes.	1. Occurs in lightly doped diodes.
2. Ionization takes place by electric field.	2. Ionization takes place by collisions.
3. Occurs even with less than 5V.	3. Occurs at higher voltages.
4. After the breakdown voltage across the zener diode is constant.	4. After breakdown voltage across the pn diode is not constant.

VI CHARACTERISTICS OF ZENER DIODE

- Voltage versus current characteristics of zener diode.
- Characteristics in forward bias.
- Characteristics in reverse bias.

FORWARD BIAS CHARACTERSTICS

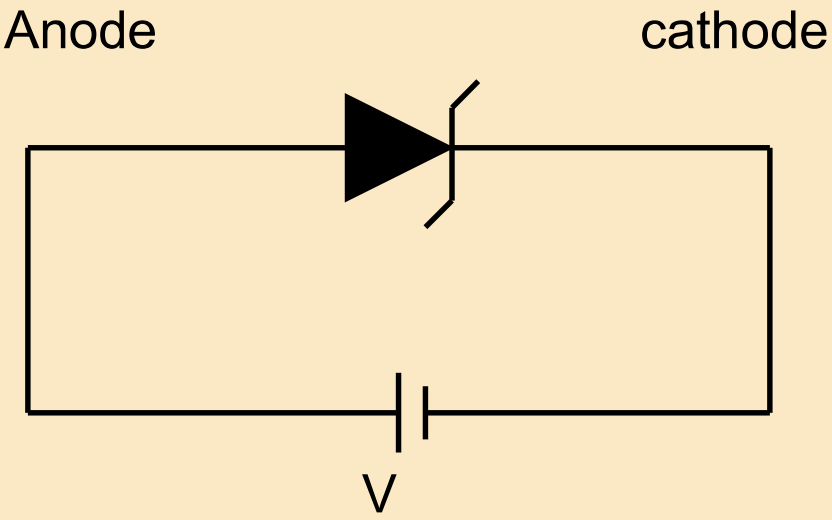


Fig 1. zener diode in forward bias

FORWARD BIAS CHARACTERSTICS

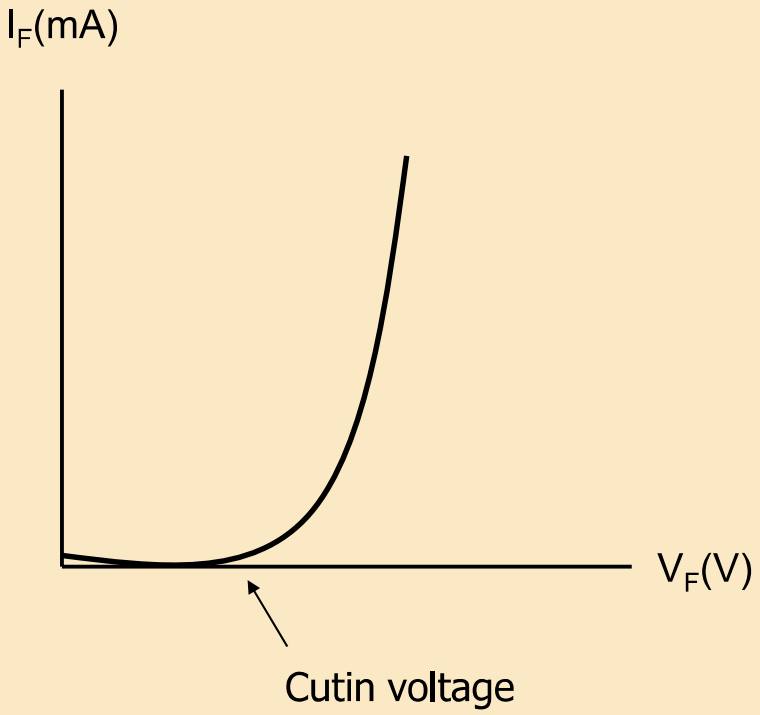


Fig2. Forward bias charactersticas of zener diode

FORWARD BIAS CHARACTERSTICS

- Characteristics same as pn diode.
- Not operated in forward bias.

REVERSE BIAS CHARACTERSTICS

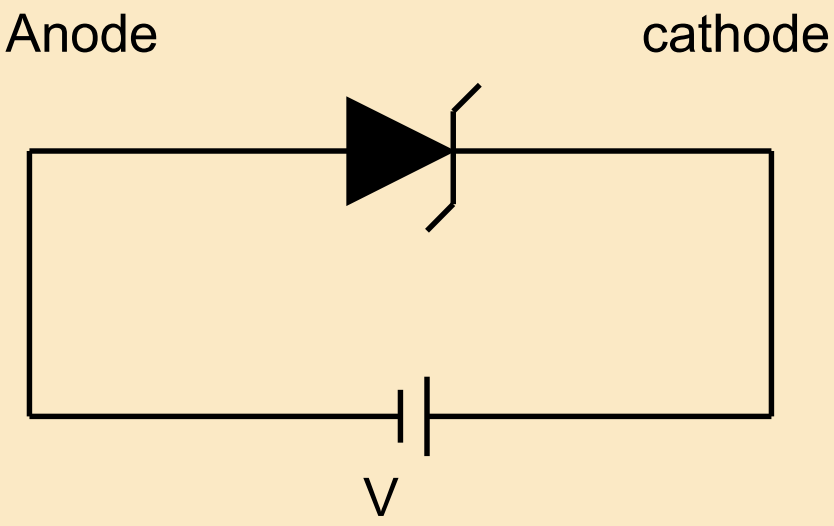


Fig 3. Zener diode in Reverse bias

REVERSE BIAS CHARACTERSTICS

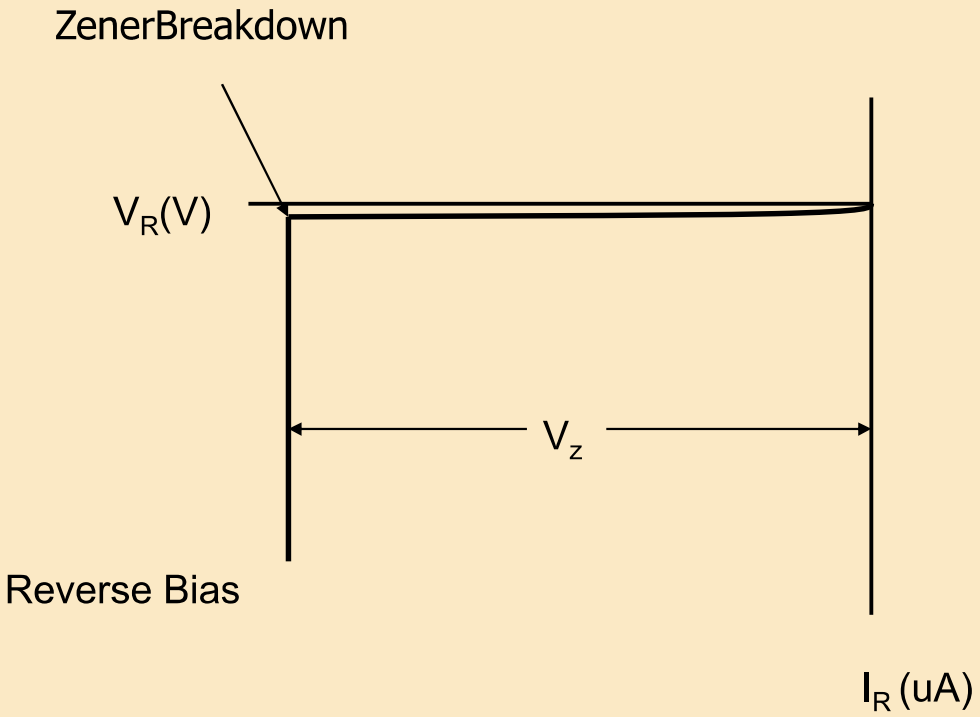


Fig 4. Reverse Bias characterstics of zener diode

REVERSE BIAS CHARACTERSTICS

- Always operated in reverse bias.
- Reverse voltage at which current increases suddenly and sharply
- known as Zener break down voltage.
- Zener break down occurs lower voltages than avalanche break down voltage.
- After break down the reverse voltage V_Z remains constant.

VI CHARACTERISTICS

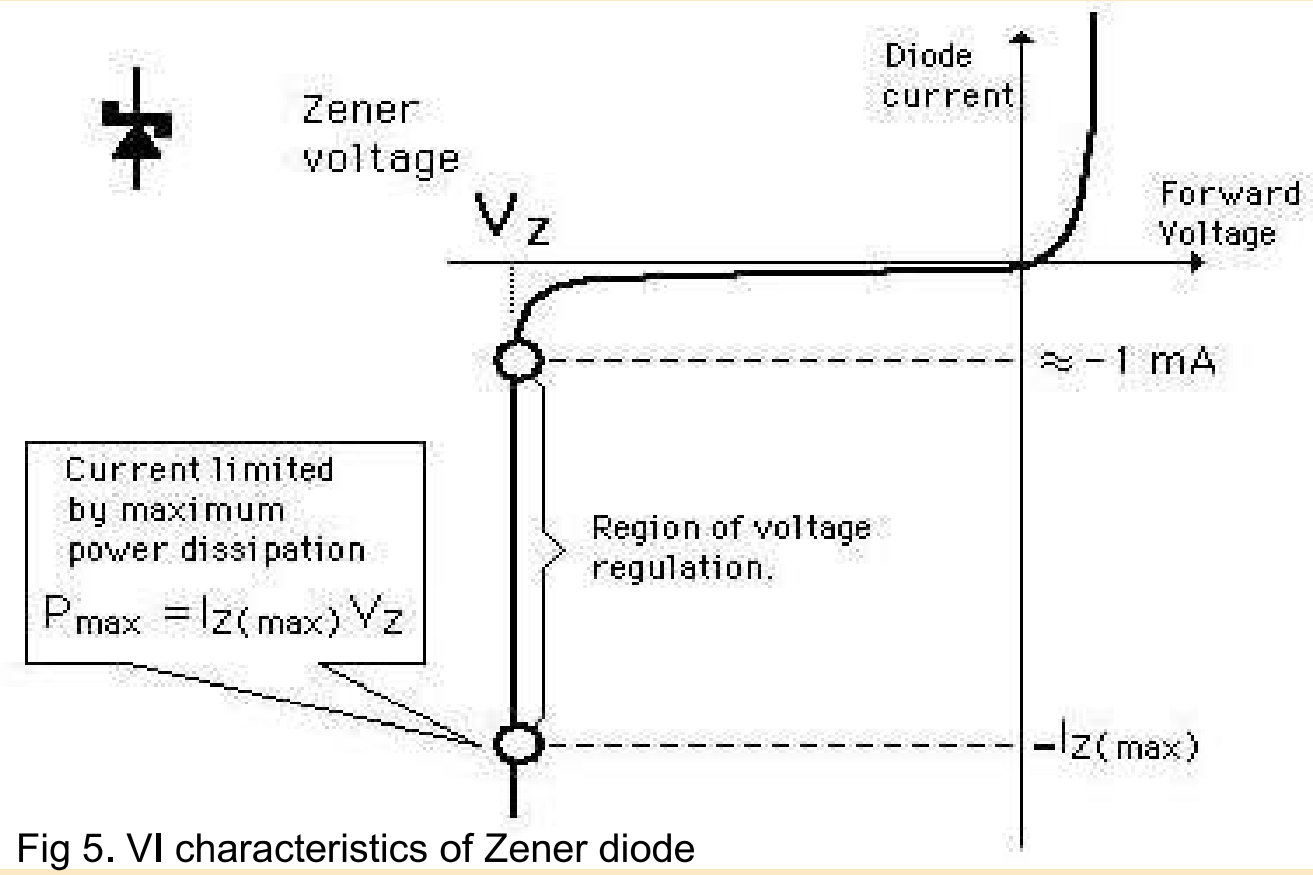


Fig 5. VI characteristics of Zener diode

APPLICATIONS OF ZENER DIODE

- Used as voltage regulator.
- Also used in clipper circuits

SPECIFICATIONS OF ZENER DIODE

Specifications of 1n746 zener diode.

Zener Voltage:	3.3V
Tolerance range of zener voltage:	±5% to ±10%
Test current I_{ZT}:	20 mA
Maximum zener Impedance Z_{ZT}:	28 ohms

SPECIFICATIONS OF ZENER DIODE

Specifications of 1n746 zener diode.

Maximum d.c. zener current:	110mA
Reverse leakage current I_s:	10uA
Maximum power dissipation:	500 mw up to 75 w

UNIT-II

DIODE APPLICATIONS

- Introduction
- Diode as switch
- Forward recovery and reverse recovery times of a diode
- Rectifier-HW & FW,
- Bridge wave reciter, PIV.
- Filters: Inductor & Capacitors,
  L-Section & Pi-section Filters
- Zener Diode as voltage regulator
- Brief introduction to Clipping & Clamping circuits.

Prepared
by
Mr. M.A Vijay Kamalnath,
Asst.Prof, Dept.of ECE,
RGMCET, Nandyal.

The Basic DC Power Supply

- Power supply is a group of circuits that convert the ***standard ac voltage*** (120 V, 60 Hz) provided by the wall outlet to ***constant dc voltage***.
- The voltage produced is used to power all types of electronic circuits including:
  - Consumer electronics (ex: radio, television, DVD, etc.)
  - Computers
  - Industrial controllers
  - Most laboratory instrumentation systems and equipment
- The dc voltage level required depends on the application, but most applications require relatively low voltage.
- There are two basic types of power supplies: a linear power supply and a switching power supply. These components are described as follows:
  1. A ***linear power supply*** is one that provides a ***constant current path*** between its input and its load.
  2. A ***switching power supply*** provides an ***intermittent current path*** between its input and its output.

Half-Wave Rectifiers

Diode – ability to conduct current in one direction and block current in other direction

→ used in circuit called **RECTIFIER (ac →dc)**

Objective:

- Discuss the operation of half-wave rectifiers
- Describe a basic dc power supply & half-wave rectifications
- Determine the average value, V_{AVG} of half-waves rectified voltage
- Discuss the effect of barrier potential, V_P on a half-wave rectifier output
- Define *Peak Inverse Voltage* (PIV)
- Describe Transformer-couple half-wave rectifier

2-2 Half-Wave Rectifiers (cont.)

(The Half-Wave Rectifier)

•A half wave rectifier(ideal) allows conduction for only 180° or half of a complete cycle.

•During first one cycle:

-*Vin* goes positive – diode *FB* – conduct current

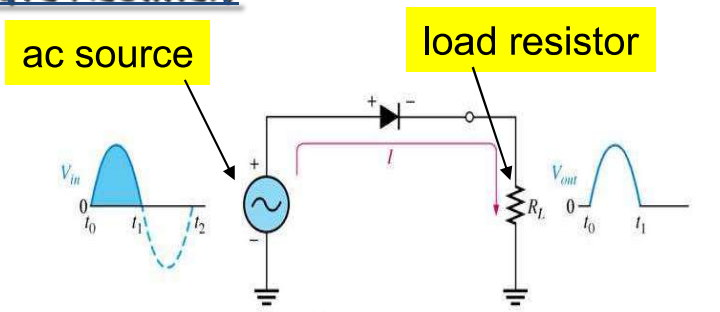
-*Vin* goes negative – diode *RB* – no current- 0V

•The output frequency is the same as the input (same shape).

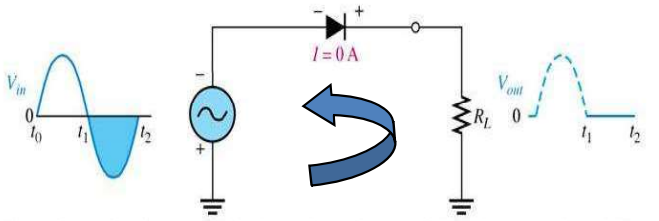
The average value V_{DC} or V_{AVG} :

$$V_{AVG} = \frac{V_p}{\pi}$$

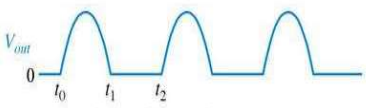
-Measure on dc voltmeter



(a) During the positive alternation of the 60 Hz input voltage, the output voltage looks like the positive half of the input voltage. The current path is through ground back to the source.



(b) During the negative alternation of the input voltage, the current is 0, so the output voltage is also 0.



(c) 60 Hz half-wave output voltage for three input cycles

Ideal diode model

Half-Wave Rectifiers (cont.)

(Effect of the Barrier Potential on the Half-Wave Rectifier Output)

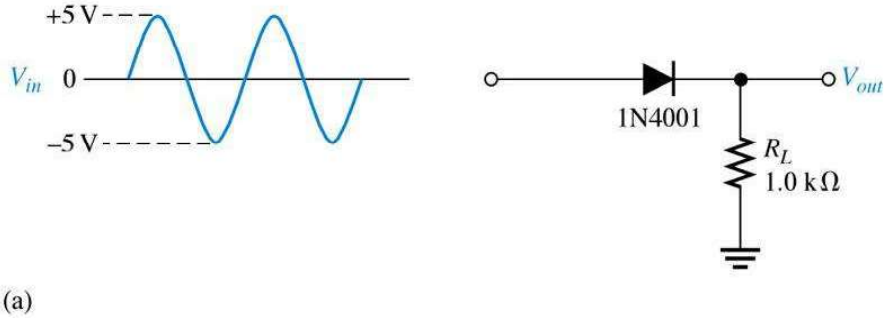
- Practical Diode – barrier potential of 0.7V (Si) taken into account.
- During +ve half-cycle – V_{in} must overcome $V_{potential}$ for forward bias.

- Example 1: Calculate the peak o/p voltage, $V_{p(out)}$?

The peak o/p voltage:

$$V_{p(out)} = V_{p(in)} - 0.7V$$

$$V_{p(out)} = V_{p(in)} - 0.7V$$
$$= 5V - 0.7V$$
$$= 4.30V$$

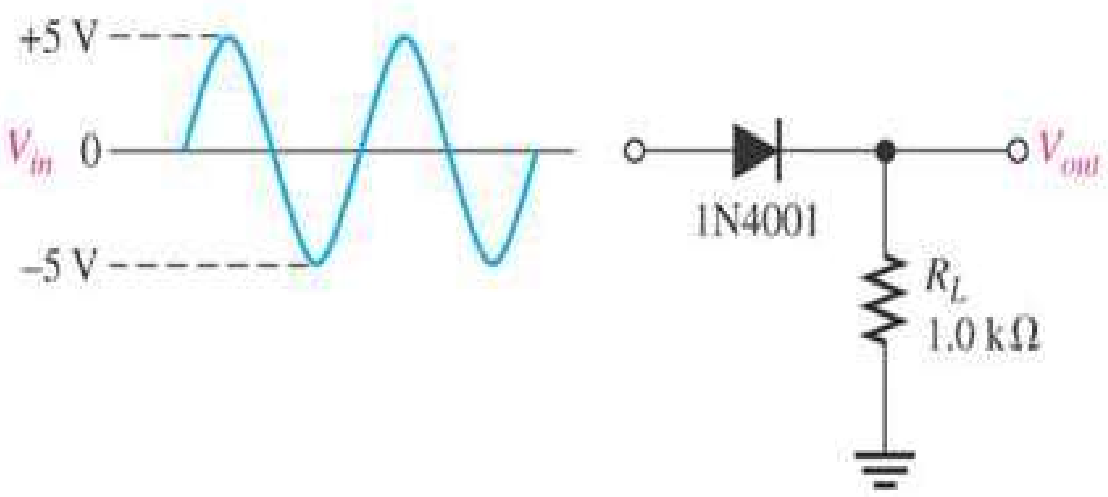


(a)

2-2 Half-Wave Rectifiers (cont.)

(Effect of the Barrier Potential on the Half-Wave Rectifier Output)

Example 2:

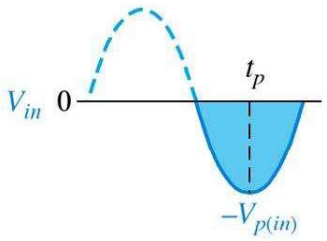


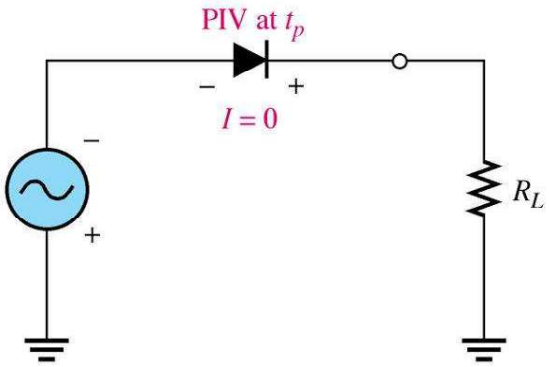
Sketch the output V_o and determine the output level voltage for the network in above figure.

Half-Wave Rectifiers (cont.)

[Peak Inverse Voltage (PIV)]

- Peak inverse voltage (PIV) is **the *maximum voltage* across the diode when it is in *reverse bias*.**





The diode must be capable of withstanding this amount of voltage.

$$PIV = V_{p(in)}$$

Half-Wave Rectifiers (cont.)

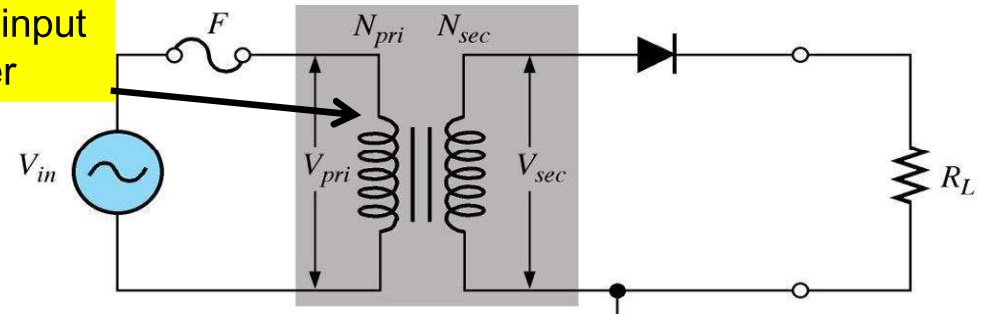
(Half-Wave Rectifier with Transformer-Coupled Input Voltage)

- Transformers are often used for voltage change and isolation.
- The *turns ratio, n* of the primary to secondary determines the *output versus the input.*

$$V_{\text{sec}} = nV_{pri}$$

- The advantages of transformer coupling:
  1) allows the source voltage to be stepped up or down
  2) the ac source is electrically isolated from the rectifier, thus prevents shock hazards in the secondary circuit.

to couple ac input to the rectifier



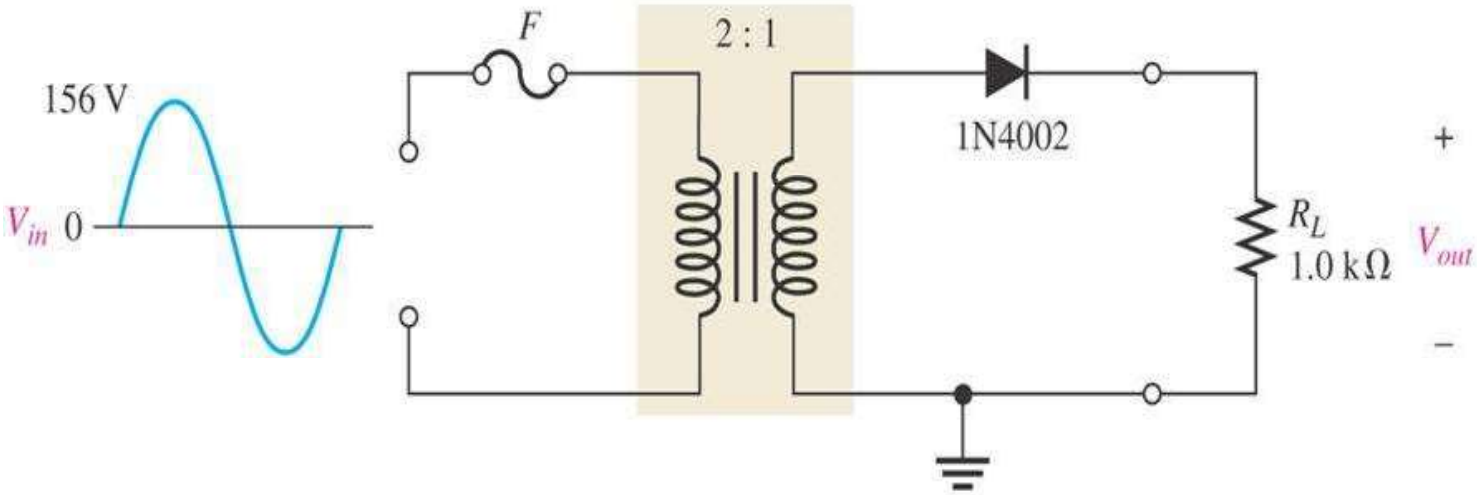
$$n = \frac{N_{\text{sec}}}{N_{pri}}$$

If n>1, Vsec is greater than Vpri.
If n<1, Vsec is less than Vpri.
If n=1, Vsec= Vpri.

$$V_{p(out)} = V_{p(\text{sec})} - 0.7V$$
$$PIV = V_{p(\text{sec})}$$

Example 3:

Determine the peak value of output voltage as shown in below Figure.



Full-Wave Rectifiers

(Introduction)

Objective:

- Explain & Analyze the operation of Full-Wave Rectifier.
- Discuss how full wave rectifier differs from half-wave rectifier
- Determine the average value
- Describe the operation of center-tapped & bridge.
- Explain effects of the transformers turns ratio
- PIV
- Comparison between center-tapped & bridge.

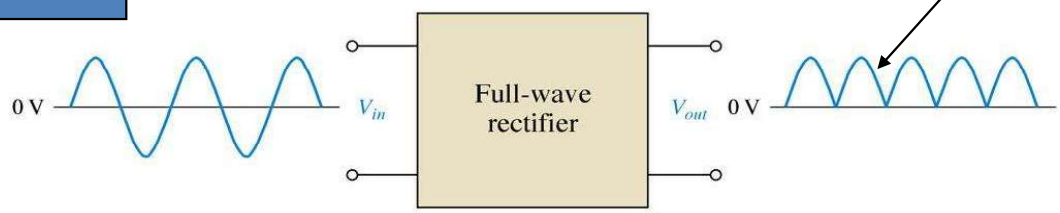
Full-Wave Rectifiers (cont.)

(Introduction)

- A full-wave rectifier allows current to flow during both the positive and negative half cycles or the full 360º whereas half-wave rectifier allows only during one-half of the cycle.
- The no. of +ve alternations is twice the half wave for the same time interval
- The output frequency is twice the input frequency.
- The average value – the value measured on a dc voltmeter

$$V_{AVG} = \frac{2V_p}{\pi}$$

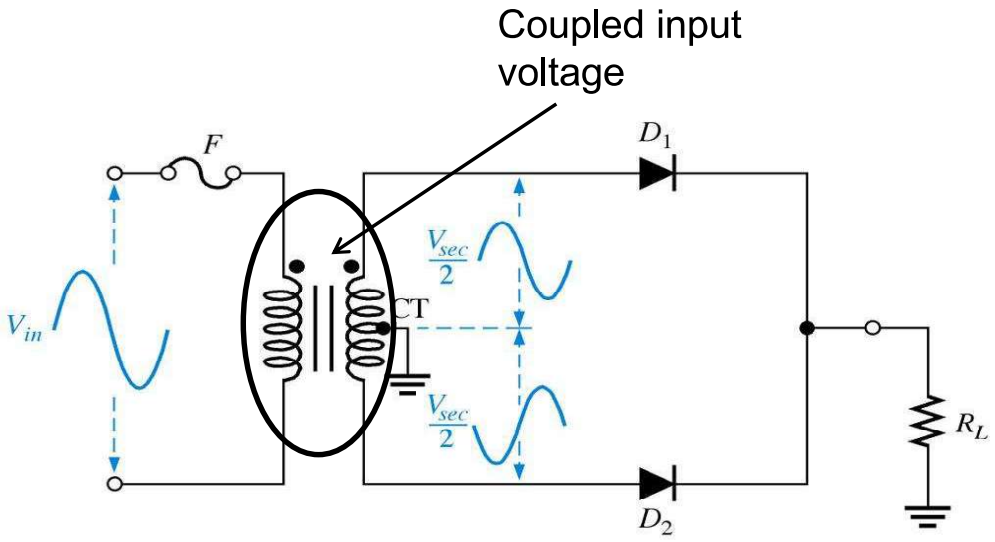
63.7% of V_p



Full-Wave Rectifiers

(i - The Center-Tapped Full-Wave Rectifier)

- This method of rectification employs *two diodes* connected to a secondary center-tapped transformer.
- The i/p voltage is coupled through the transformer to the center-tapped secondary.



Full-Wave Rectifiers (cont.)

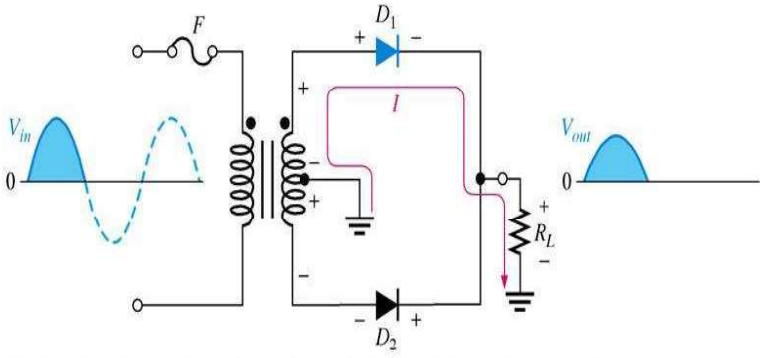
(i – The Center-Tapped Full-Wave Rectifier)

•+ve half-cycle input voltage (forward-bias D_1 & reverse-bias D_2)-the current pass through the D_1 and R_L

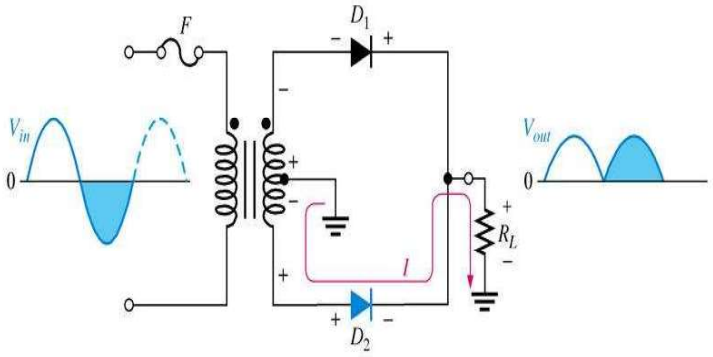
•-ve half-cycle input voltage (reverse-bias D_1 & forward-bias D_2)-the current pass through D_2 and R_L

•The output current on both portions of the input cycle – same direction through the load.

•The o/p voltage across the load resistors – full-wave rectifiers



(a) During positive half-cycles, D_1 is forward-biased and D_2 is reverse-biased.



(b) During negative half-cycles, D_2 is forward-biased and D_1 is reverse-biased.

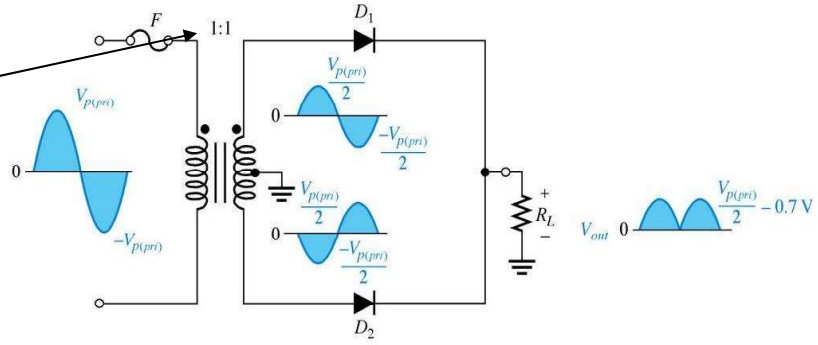
Full-Wave Rectifiers (cont.)

(i - The Center-Tapped Full-Wave Rectifier)

-Effect of the Turns Ratio on the Output Voltage-

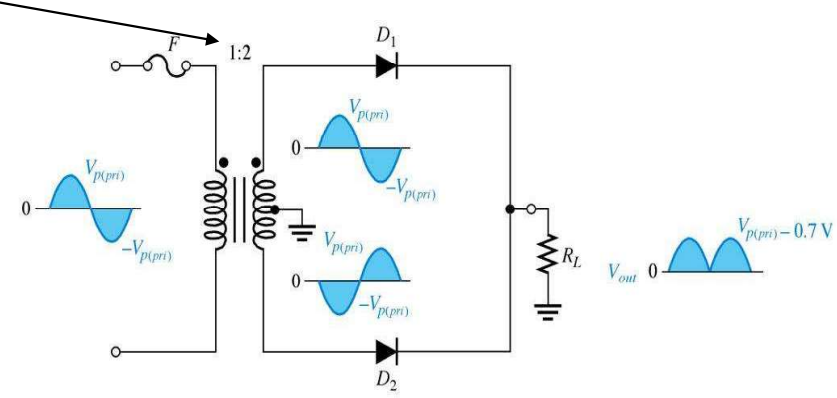
If n=1, $V_{p(out)}=\frac{V_{p(pri)}}{2}-0.7V$

- $V_{p(sec)}=V_{p(pri)}$



If n=2, $V_{sec}=2V_{pri}$

$$V_{p(out)}=V_{p(pri)}-0.7$$



- In any case, the o/p voltage is always one-half of the total secondary voltage minus the diode drop (barrier potential), no matter what the turns ratio.

$$V_{out}=\frac{V_{sec}}{2}-0.7V$$

Full-Wave Rectifiers (cont.)

(i - The Center-Tapped Full-Wave Rectifier)

-Peak Inverse Voltage (PIV)-

- Maximum anode voltage: $D_1 = +\frac{V_{p(\sec)}}{2}$ $D_2 = -\frac{V_{p(\sec)}}{2}$

D1: forward-bias – its cathode is at the same voltage of its anode minus diode drop; This is also the voltage on the cathode of D2.

- **PIV across D2** :

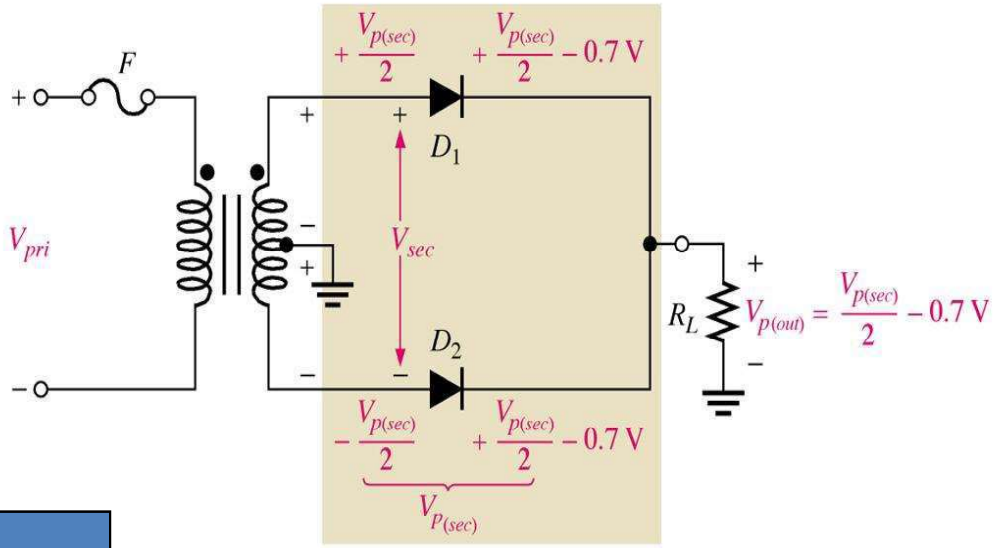
$$PIV = \left(\frac{V_{p(\sec)}}{2} - 0.7V\right) - \left(\frac{-V_{p(\sec)}}{2}\right)$$
$$= V_{p(\sec)} - 0.7V$$

- We know that

$$V_{p(out)} = \frac{V_{p(\sec)}}{2} - 0.7V$$
$$\rightarrow \quad V_{p(\sec)} = 2V_{p(out)} + 1.4V$$

- Thus;

$$PIV = 2V_{p(out)} + 0.7V$$



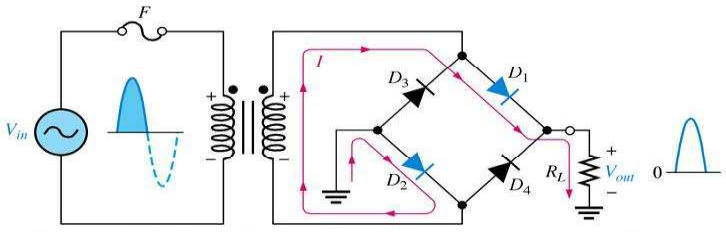
Full-Wave Rectifiers (cont.)

(ii - The Bridge Full-Wave Rectifier)

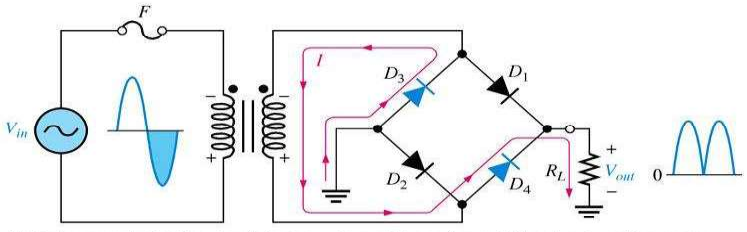
- It employs four diodes arranged such that current flows in the direction through the load during each half of the cycle.

- When Vin +ve, D1 and D2 FB and conduct current. A voltage across R_L looks like +ve half of the input cycle. During this time, D3 and D4 are RB.

- When Vin –ve, D3 and D4 are FB and conduct current. D1 and D2 are RB.



(a) During positive half-cycle of the input, D_1 and D_2 are forward-biased and conduct current. D_3 and D_4 are reverse-biased.



(b) During negative half-cycle of the input, D_3 and D_4 are forward-biased and conduct current. D_1 and D_2 are reverse-biased.

Used 4 diode:
2 diode in forward
2 diode in reverse

Without diode drop (ideal diode):

$$V_{p(out)} = V_{p(\sec)}$$

2 diode always in series with load resistor during +ve and –ve half cycle .

With diode drop (practical diode):

$$V_{p(out)} = V_{p(\sec)} - 1.4V$$

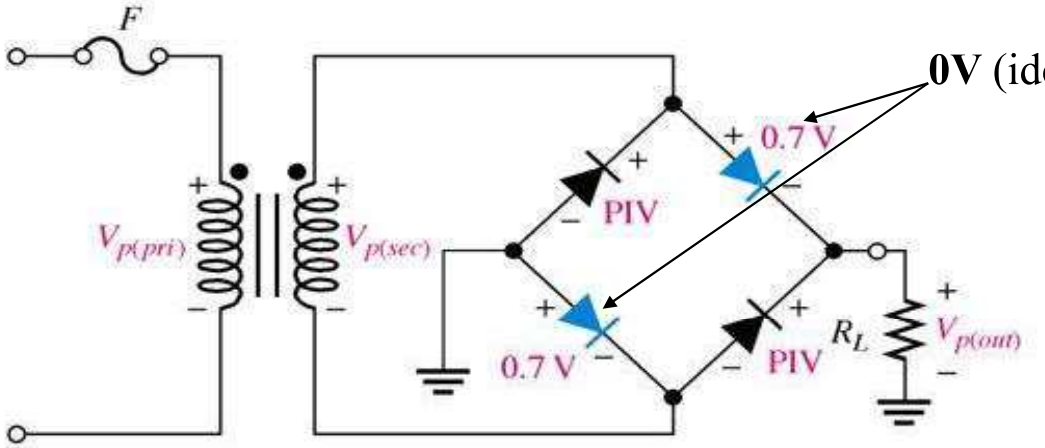
16

Full-Wave Rectifiers (cont.)

(ii - The Bridge Full-Wave Rectifier)

For ideal diode, *PIV* = $V_{p(out)}$

For each diode,



(b) For the practical diode model (forward-biased diodes D_1 and D_2 are shown in blue). PIV = $V_{p(out)}$ + 0.7 V

Note that in most cases we take the diode drop into account.

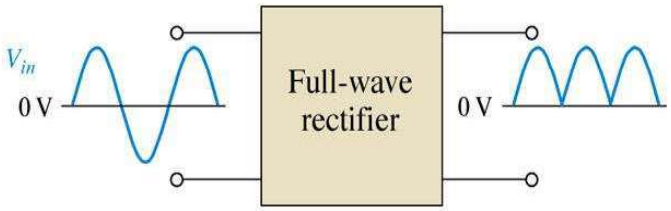
Power Supply Filters And Regulators (cont.)

(introduction)

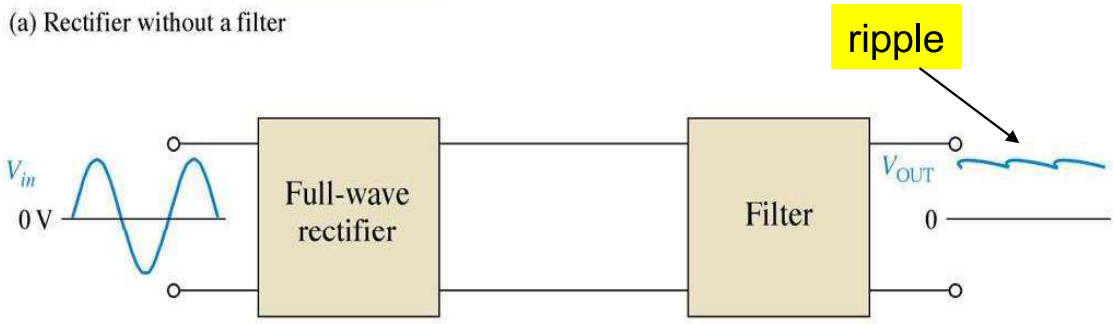
•In most power supply – 60 Hz ac power line voltage is converted to constant dc voltage.

•60Hz pulsating dc output must be filtered to reduce the large voltage variation.

•Small amount of fluctuation in the filter o/p voltage - ripple



(a) Rectifier without a filter



(b) Rectifier with a filter (output ripple is exaggerated)

2-4 Power Supply Filters And Regulators (cont.)

(Capacitor-Input Filter)

Capacitive Filter

- Capacitive filter is simply a *capacitor* connected in *parallel* with the *load resistance* or connected from the *rectifier output* to *ground*, as shown in Fig.2-39.

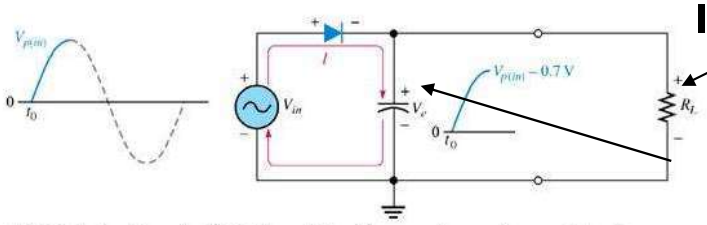
- During the *positive first quarter-cycle* of the input, the diode is forward-biased, allowing the capacitor charges rapidly, as illustrated in Fig.2-39(a).

- When the input begins to go *negative*, the diode is reverse-biased, and the capacitor slowly discharges through the load resistance (Fig.2-39(b)). As the output from the rectifier drops below the charged voltage of the capacitor, the capacitor acts as the *voltage source* for the load.

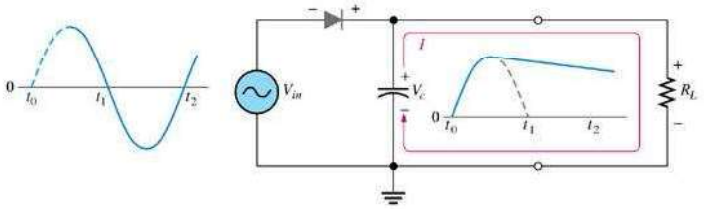
- During first quarter of the next cycle, as illustrated in part (c), the diode will again become forward-biased when the input voltage exceeds the capacitor voltage.

load

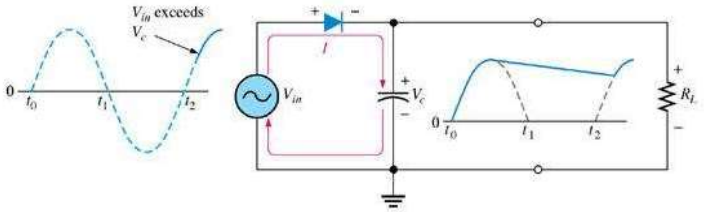
capacitor



(a) Initial charging of capacitor (diode is forward-biased) happens only once when power is turned on.



(b) The capacitor discharges through R_L after peak of positive alternation when the diode is reverse-biased. This discharging occurs during the portion of the input voltage indicated by the solid blue curve.



(c) The capacitor charges back to peak of input when the diode becomes forward-biased. This charging occurs during the portion of the input voltage indicated by the solid blue curve.

Ripple Voltage

Ripple voltage is the *fluctuation* in the *capacitor voltage* due to the difference between the charge and discharge times.
The difference between the charge and discharge times is caused by two distinct *RC time constant* in the circuit. One time constant is found as:

$$\tau = RC$$

where R and C are the total circuit resistance and capacitance, respectively.
Since it takes *five* time constants for a capacitor to charge or discharge fully, this time period (*T*) can be found as:

$$T = 5RC = 5\tau$$

For example, refer to Fig. 2-40(a), the capacitor charges through the diode. Assuming that diode has a forward resistance of 5 Ω, so the time constant for the circuit is found as:

$$\tau = (5\,\Omega)(100\ \mu F) = 500\ \mu s$$

and the total capacitor charge time is found as:

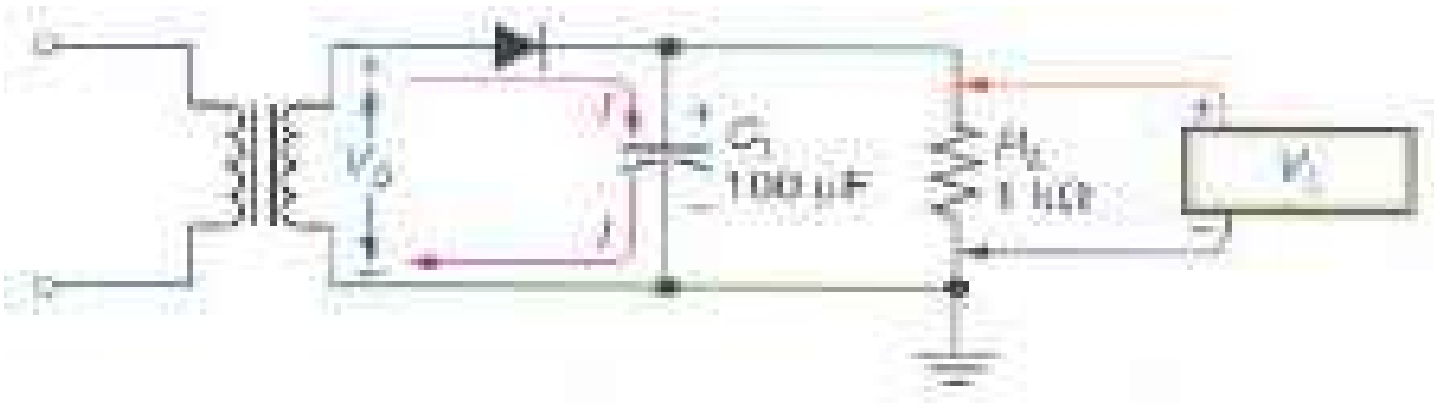
$$T = (5)(500\ \mu s) = 2.5\,ms$$

The discharge path for the capacitor is through the resistor as shown in Fig. 2-40(b). For this circuit, the time constant is found as:

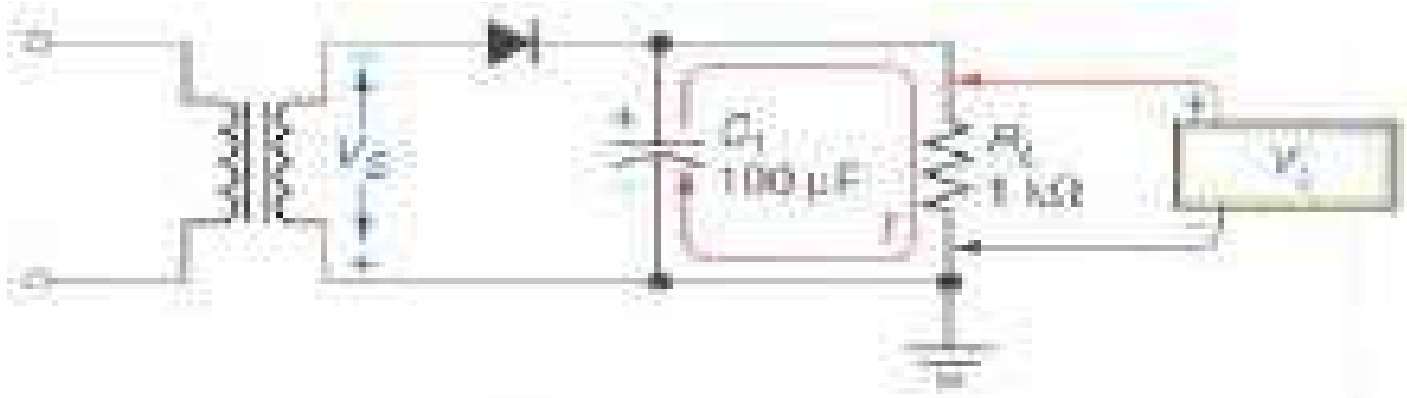
$$\tau = (1\,k\Omega)(100\ \mu F) = 100\,ms$$

and the total capacitor discharge time is found as:

$$T = (5)(100\,ms) = 500\,ms$$



(a) Charge circuit



(b) Discharge circuit

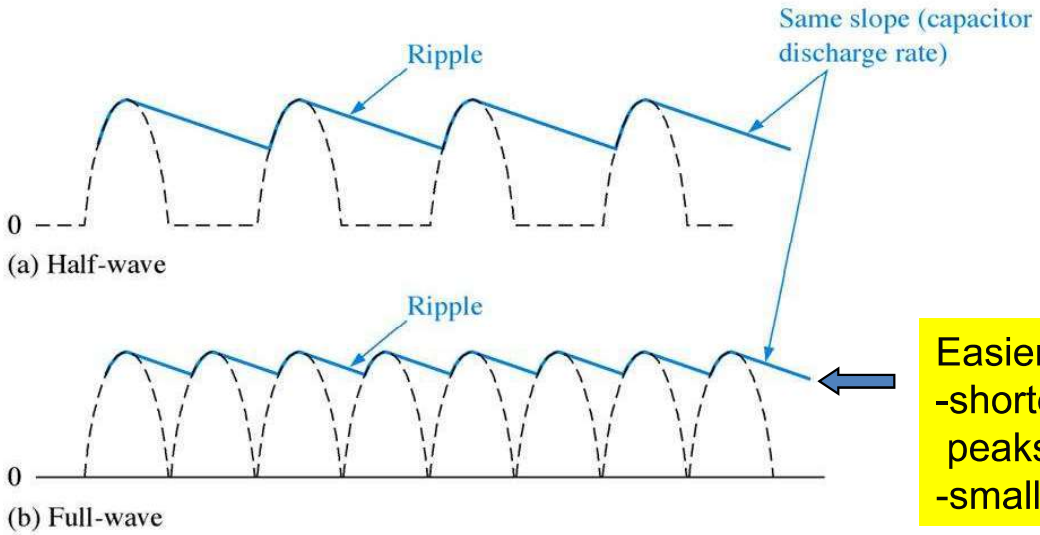
Fig.2-40: The basic capacitive filter.

Power Supply Filters And Regulators (cont.)

(Capacitor-Input Filter)

***Ripple Voltage**:* the variation in capacitor voltage due to the charging and discharging times.

The advantage of a full-wave rectifier over a half-wave is quite clear. The capacitor can more effectively reduce the *ripple* when the time between peaks is *shorter*.



Easier to filter
-shorted time between peaks.
-smaller *ripple*.

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Power Supply Filters And Regulators (cont.)

(Capacitor-Input Filter)

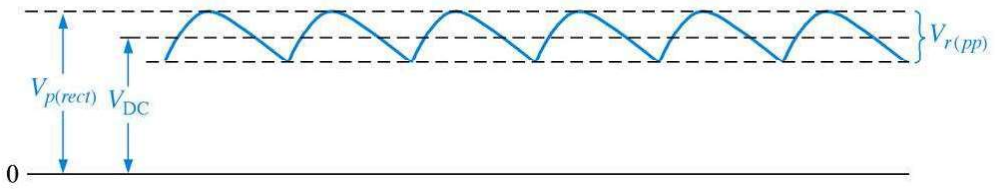
Ripple factor: indication of the effectiveness of the filter

$$r = \frac{V_{r(pp)}}{V_{DC}}$$ [half-wave rectifier]

$V_{r(pp)}$ = peak to peak ripple voltage; $V_{DC} = V_{AVG}$ = average value of filter's output voltage.

- Lower ripple factor → better filter

[can be lowered by increasing the value of filter capacitor or increasing the load resistance]



- For the full-wave rectifier:

$$V_{r(pp)} \cong \left(\frac{1}{fR_LC}\right)V_{p(rect)}$$

$$V_{DC} = V_{AVG} = \left(1 - \frac{1}{2fR_LC}\right)V_{p(rect)}$$

$V_{p(rect)}$ = unfiltered peak.

Power Supply Filters And Regulators (cont.)

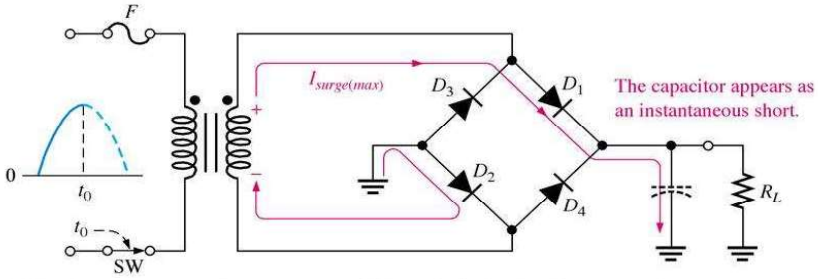
(Capacitor-Input Filter)

***Surge Current in the Capacitor-Input Filter*:**

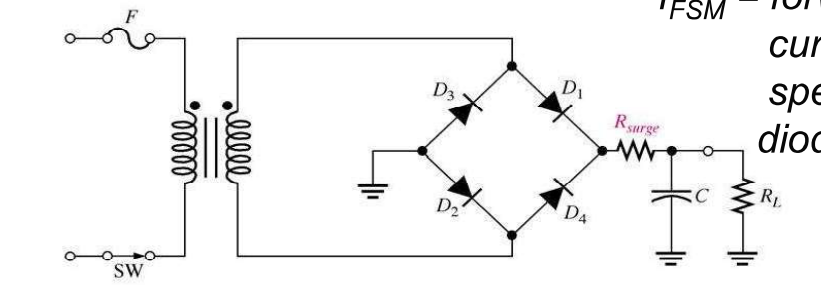
When you first turn on power supply, the filter capacitor has no accumulated charge to oppose $V_{p(sec)}$. For first instant, the capacitor appears as a short circuit, thus the current through the diodes can momentarily be quite high. To reduce risk of damaging the diodes, a surge current limiting resistor is placed in series with the filter and load.

The min. surge Resistor values:

$$R_{surge} = \frac{V_{p(sec)}}{I_{FS}}$$



(a) Maximum surge current occurs when switch is closed at peak of an input cycle.



(b) A series resistor (R_{surge}) limits the surge current.

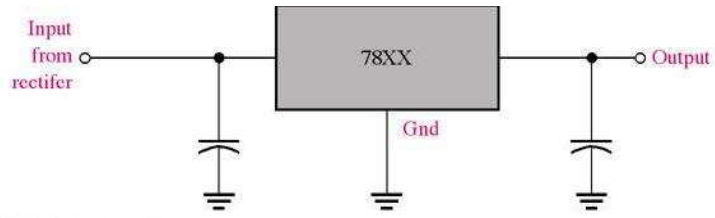
I_{FSM} = *forward surge current rating specified on diode data sheet.*

Power Supply Filters And Regulators (cont.)

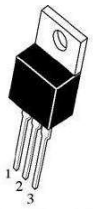
(IC Regulators)

- Connected to the output of a filtered & maintains a constant output voltage (or current) despite changes in the input, load current or temperature.
- Combination of a large capacitor & an IC regulator – inexpensive & produce excellent small power supply
- Popular IC regulators have 3 terminals:
  (i) input terminal
  (ii) output terminal
  (iii) reference (or adjust) terminal
- Type number: 78xx (xx –refer to output voltage)

i.e 7805 (output voltage +5.0V); 7824 (output voltage +24V)



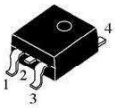
(a) Standard configuration



TO–220
T SUFFIX
CASE 221A

Heatsink surface
connected to Pin 2.

Pin 1. Input
2. Ground
3. Output



D²PAK
D2T SUFFIX
CASE 936

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

(c) Typical packages

Power Supply Filters And Regulators (cont.)

(IC Regulators)

Regulation is the last step in eliminating the remaining ripple and maintaining the output voltage to a specific value. Typically this regulation is performed by an integrated circuit regulator. There are many different types used based on the voltage and current requirements.

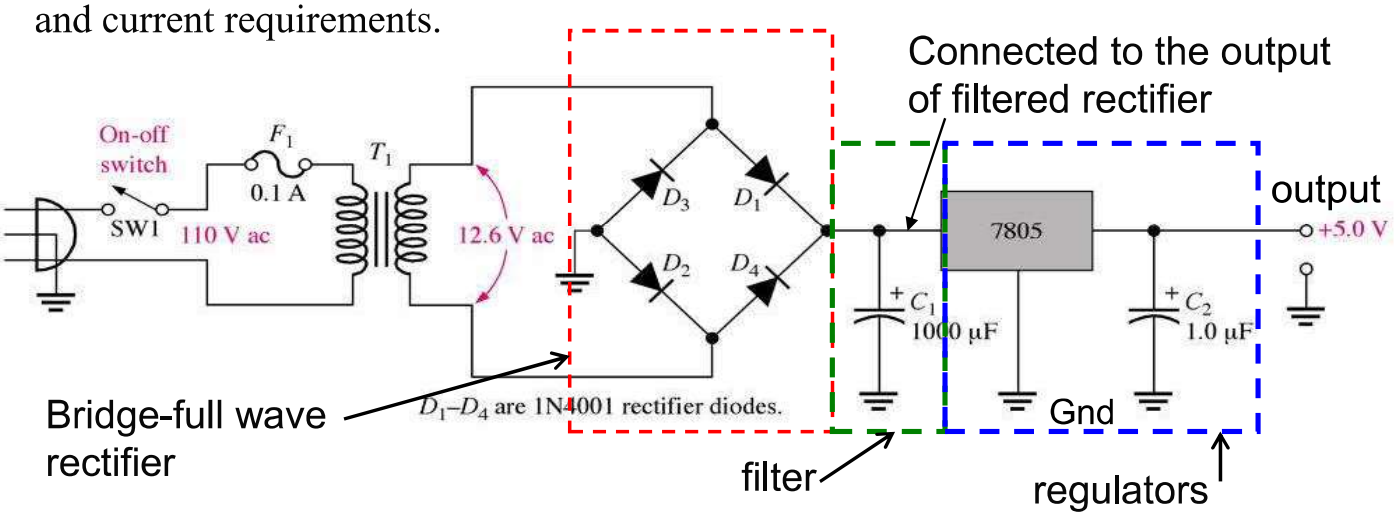


Fig. 2-23 : A basic +5.0V regulated power supply

Power Supply Filters And Regulators (cont.)

(Percent Regulations)

Percent Regulation

The regulation can be stated in a percentage in terms of *input (line) regulation* or *load regulation*.

- Line regulation specifies how much change occurs in the output voltage for a given change in the input voltage. It is mathematically defined as a ratio of a change in output voltage for a corresponding change in the input voltage expressed as a percentage.

$$Line\,regulation = \left(\frac{\Delta V_{OUT}}{\Delta V_{IN}} \right) x100\%$$

- Load regulation specifies how much change occurs in the output voltage over a certain range of load current values, usually from minimum current (no load, NL) to maximum current (full load, FL). It can be mathematically determined with the following formula:

$$Load\,regulation = \left(\frac{V_{NL} - V_{FL}}{V_{FL}} \right) x100\%$$

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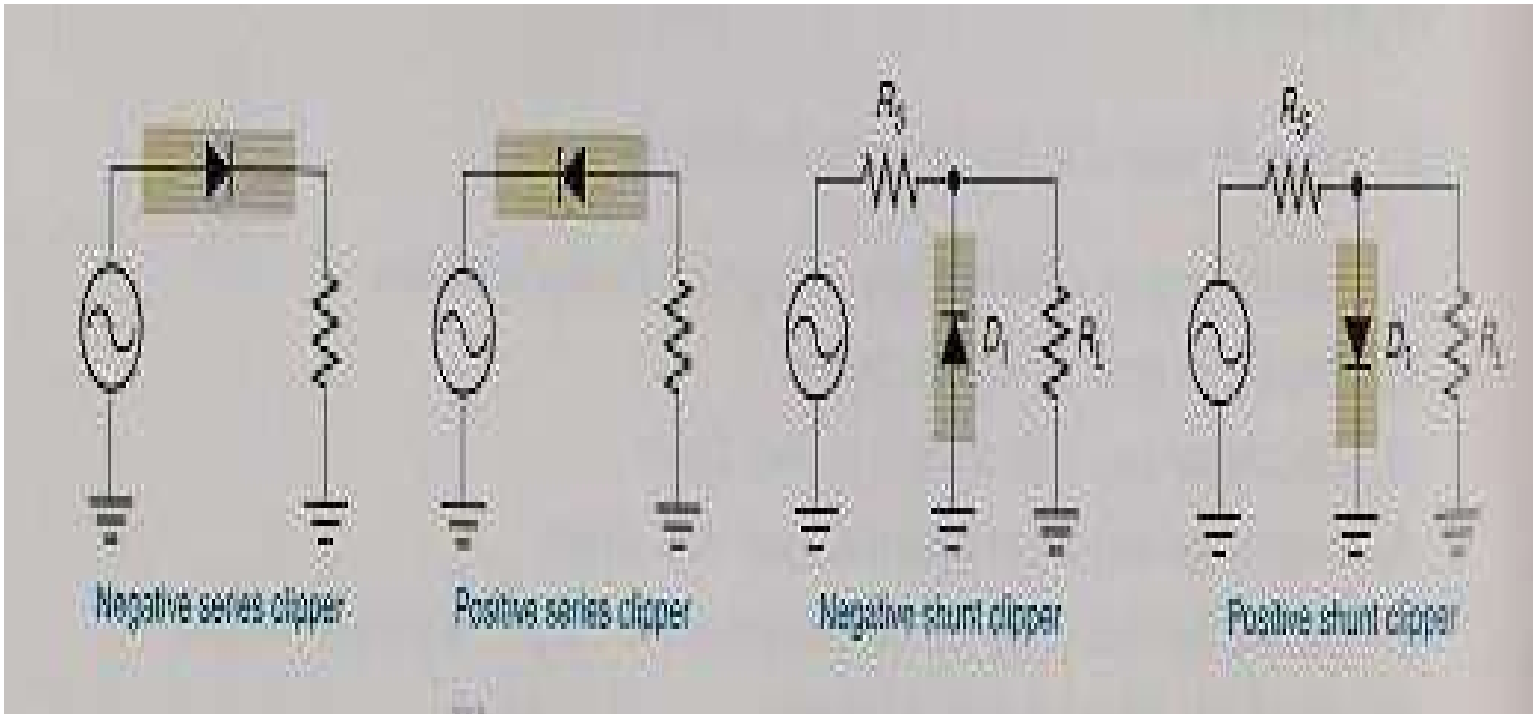
Diode Limiting & Clamping Circuits (Diode Limiters)

- Diode limiters/clippers – that limits/clips the portion of signal voltage above or below certain level.
- Limiting circuits limit the positive or negative amount of an input voltage to a specific value.
- 4 basic clipper configuration:
  - Negative series clipper } diode is in series with its load
  - Positive series clipper }
  - Negative shunt clipper } diode is in parallel with its load
  - Positive shunt clipper }

2-5 Diode Limiting & Clamping Circuits (Diode Limiters)



Clipper configuration

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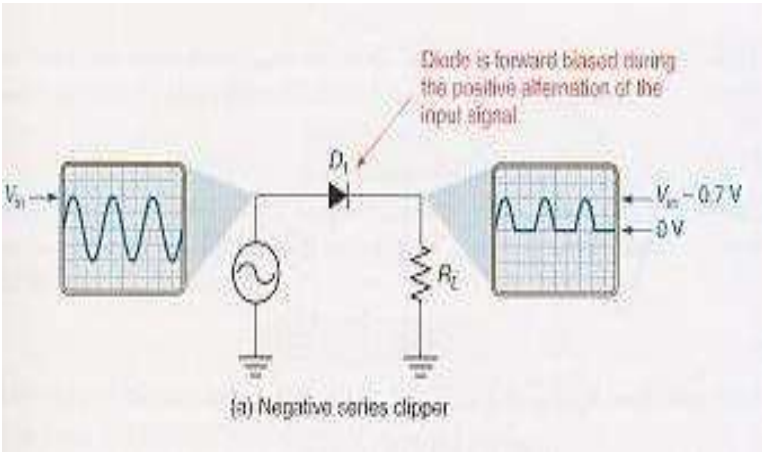
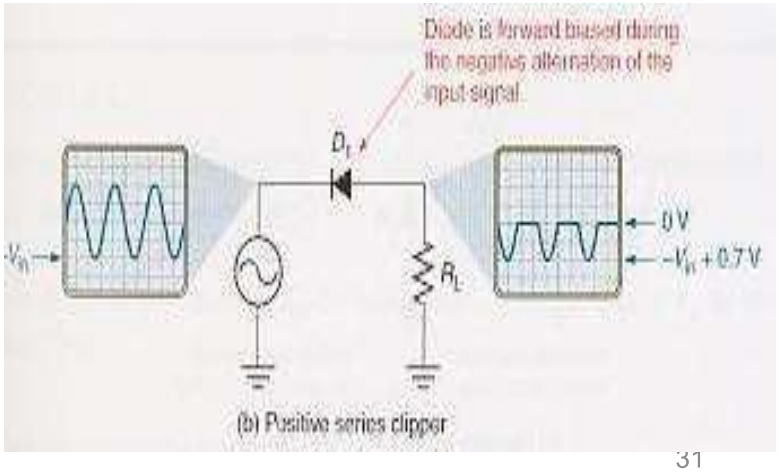
2-5 Diode Limiters (series clipper/limiter)

- Negative series clipper
- Diode is forward-biased during +ve alternation of i/p signal.
- Diode is reverse-biased when i/p signal is –ve.
- Eliminates negatives alternation of its i/p.

- Positive series clipper
- Diode is reverse-biased during +ve alternation of i/p signal.
- Diode is forward-biased when i/p signal is –ve.
- Eliminates positive alternation of its input.



(a) Negative series clipper



(b) Positive series clipper

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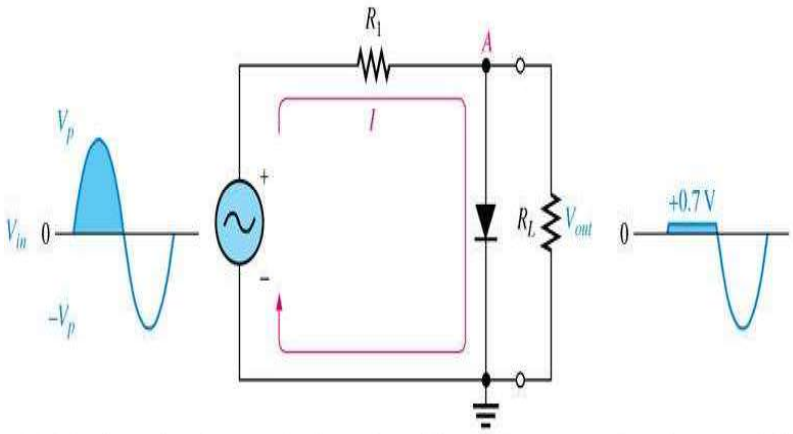
2-5Diode Limiters (shunt clipper/limiter)



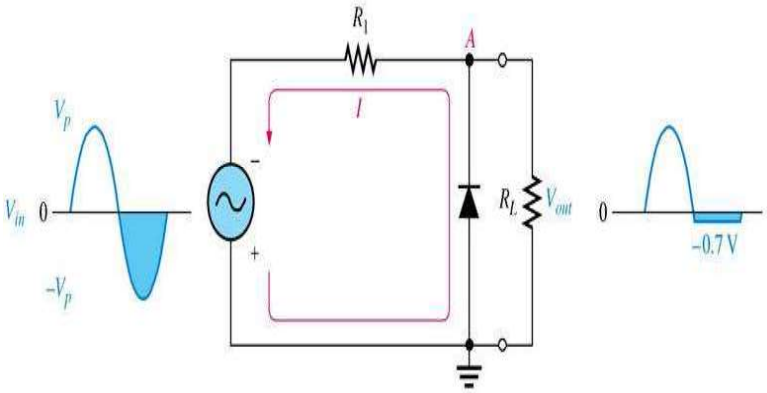
(a) Limiting of the positive alternation. The diode is forward-biased during the positive alternation (above 0.7 V)

Positive shunt clipper

- Forward-biased diode when i/p is +ve cycle.
- Reverse-biased diode when i/p is in –ve cycle.
- o/p signal is limit/clip to +0.7V during +ve cycle of i/p signal.

Negative shunt clipper

- Reverse-biased diode act as open cct during +ve cycle.
- Forward-biased diode act as short cct during –ve cycle.
- o/p signal is limit/clip to -0.7V during –ve cycle of i/p signal.



(b) Limiting of the negative alternation. The diode is forward-biased during the negative alternation (below –0.7 V) and reverse-biased during the positive alternation.

2-5 Diode Limiting & Clamping Circuits (Diode Limiters)

Series clipper

- When diode in –ve series clipper is FB, load voltage is: $V_L=V_{in} – 0.7V$
- When diode is RB, doesn't conduct, so:
  - $V_L = 0V$
- +ve series clipper operates the same. The only differences are:
  - O/p voltage polarities are reversed. $V_L=-V_{in} + 0.7V$
  - Current direction through cct are reversed.

Shunt clipper

- For –ve shunt, when i/p signal +ve cycle, diode is RB (open circuit), thus:

$$V_{out} = \left(\frac{R_L}{R_1 + R_L} \right) V_{in}$$

- During –ve cycle, diode is FB, load voltage is equal to diode forward voltage.

$$V_L = -V_F = -0.7V$$

- For +ve shunt, o/p voltage and current direction are reversed.

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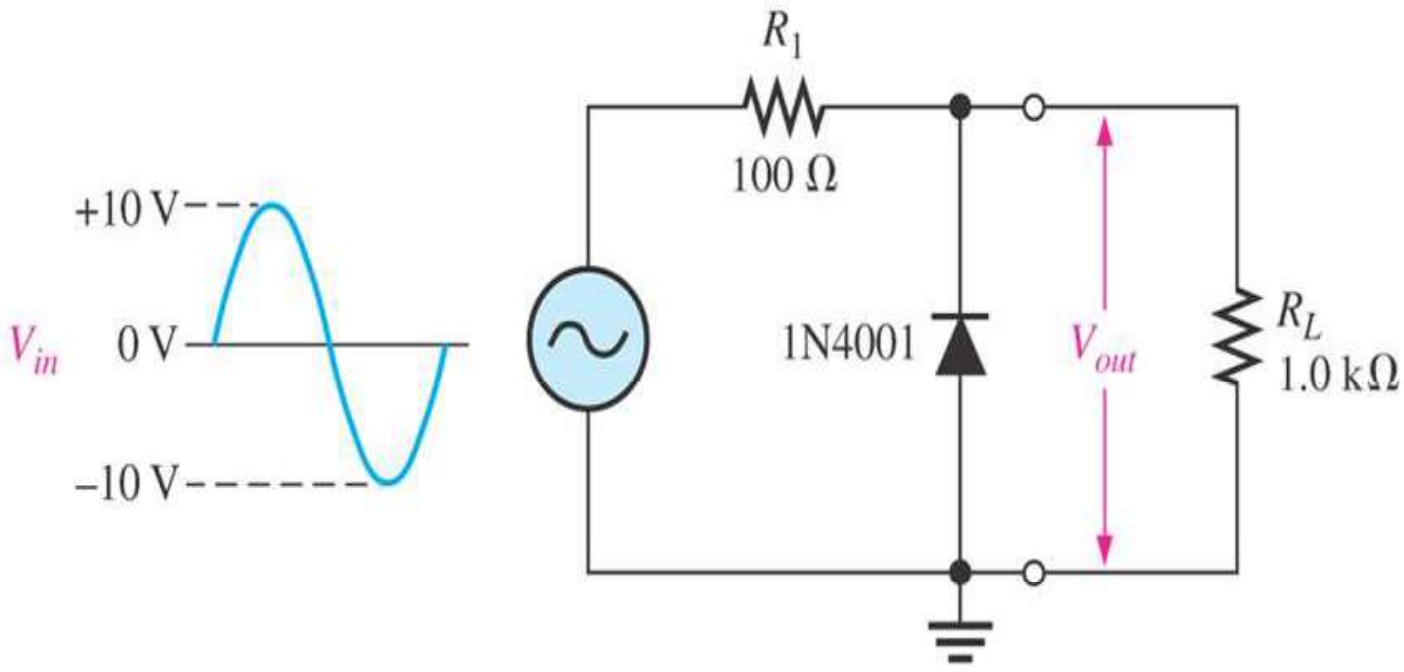
Question 4:
What would you expect to see displayed on an oscilloscope connected across RL in the limiter shown below.



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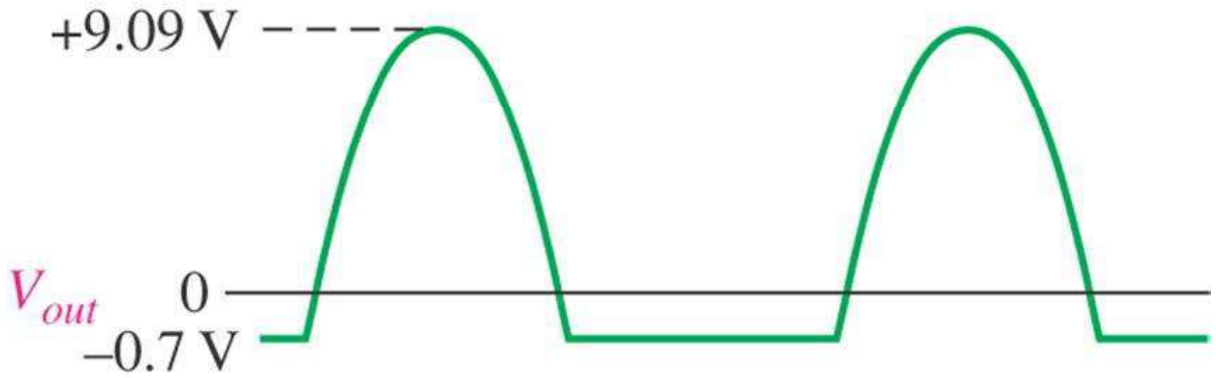
- Solution question 4
- The diode is forward biased and conducts when input voltage goes below -0.7V. So, for –ve limiter, the peak output voltage across RL is:

$$V_{p(out)} = \left(\frac{R_L}{R_1 + R_L}\right) V_{p(in)} = \left(\frac{1.0k\Omega}{1.1k\Omega}\right) 10V = 9.09V$$

- The waveform is shown below:
-



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2.5 Diode Limiting & Clamping Circuits (cont.)
(Diode Limiters)

Biased Limiters **:**

• Use dc biasing source, V_{BIAS} to set limit on the circuit output voltage.

• This allow the circuit to clip input waveform at values other than diode forward voltage, 0.7V.

• In each circuit, bias voltage is in series with shunt diode. As a result, the diode conducts and clips the i/p waveform when signal voltage equals sum of V_F and V_{BIAS}.

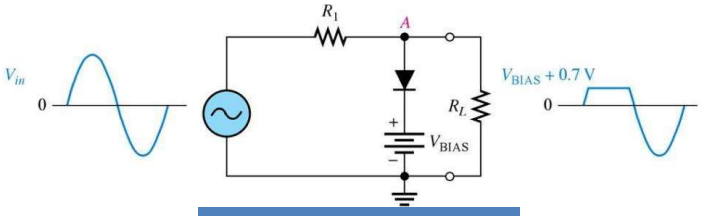
• 2 type of biased limiter: →**positive-biased limiter** →**negative-biased limiter**

• ***Positive limiter***

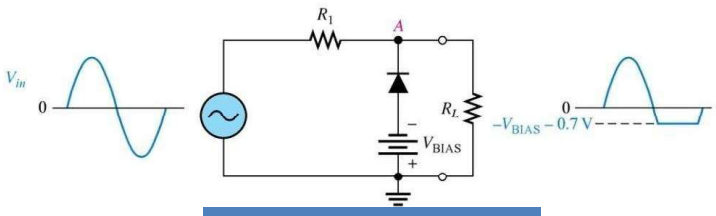
- The voltage at point A must equal V_{BIAS}+0.7V before diode become FB and conduct.
- Once diode begin to conduct, voltage at point A is limited to V_{BIAS}+0.7V, so all i/p voltage above this level is clipped off.

• **Negative limiter**

- Voltage at point A must go below $-V_{BIAS}$ - 0.7V to forward-bias the diode and initiate limiting action.



A positive limiter



A negative limiter

2-5 Diode Limiting & Clamping Circuits (cont.)
(Diode Limiters)

***Voltage-Divider Bias*:**

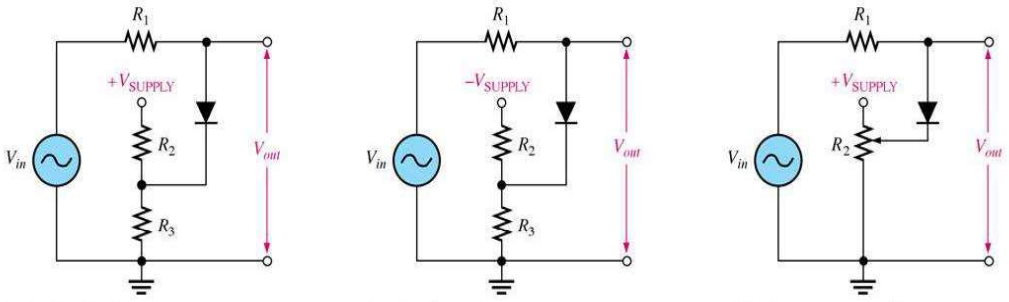
• The bias voltage source – used to illustrate the basic operation of diode limiters can be replace by a *resistive voltage divider* that derives the desired bias voltage from dc *Vsupply* .

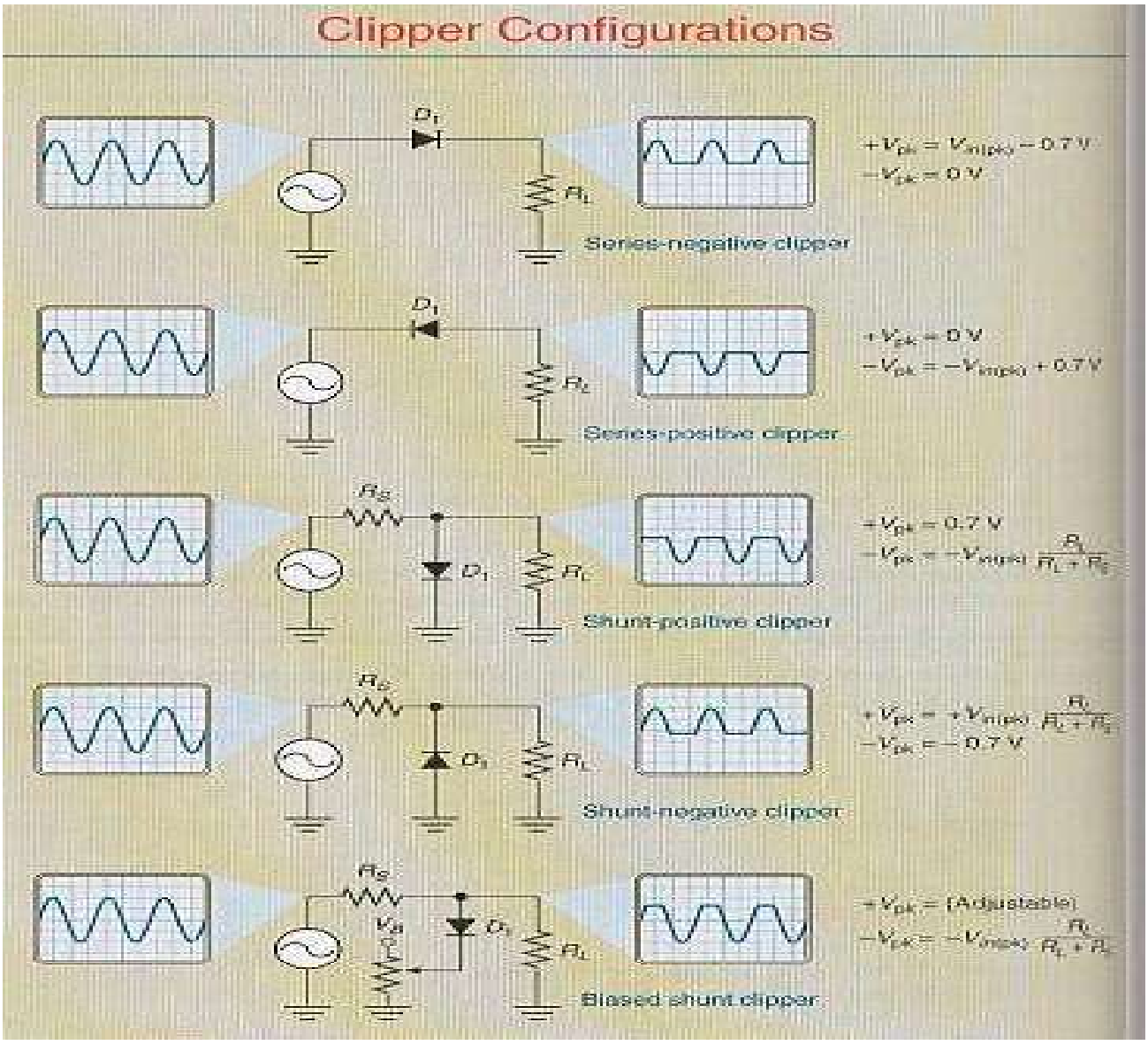
• V_{BIAS} – set by the resistor values according to the voltage-divider formula:

$$V_{BIAS} = \left(\frac{R_3}{R_2 + R_3} \right) V_{SUPPLY}$$

• The desired amount of limitation can be attained by a power supply or voltage divider. The amount clipped can be adjusted with different levels of V_{BIAS}.

• The bias resistor << R_1- the forward current through the diode will not effect V_{BIAS}




Clipper Configurations
Series-negative clipper
Series-positive clipper
Shunt-positive clipper
Shunt-negative clipper
Biased shunt clipper
+Vpk = Vin(pk) − 0.7 V
−Vpk = 0 V
+Vpk = 0 V
−Vpk = −Vin(pk) + 0.7 V
+Vpk = 0.7 V
+Vpk = +Vin(pk) RL / (RL + RS)
−Vpk = −0.7 V
+Vpk = (Adjustable)
−Vpk = −Vmax RL / (RL + RS)

2-5 Diode Limiting & Clamping Circuits (cont.) (Diode Limiter Applications)

- **Half-wave rectifier**
  - Circuit alters the shape of ac signal and change it to pulsating dc.
- **Transient protection circuit**
  - Transient → abrupt current or voltage spike in short duration.
  - Many digital circuits have i/p that cannot tolerate voltage fall outside a specified range which can cause serious damage. A clipper can be used to protect these circuits.
- **AM detector**
  - Eliminate –ve portion of i/p waveform, so capacitor charges and discharges at rate of peak i/p variations. This provides a signal at load that is a reproduction of i/p signal.

Diode Limiting & Clamping Circuits (cont.)
(Diode Clampers)

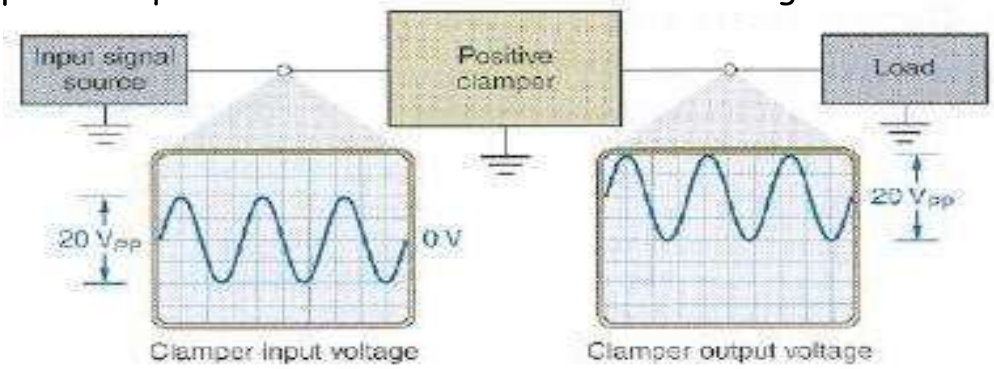
2.7 Clampers (DC Restorers)

- Clamper is a *diode circuit* designed to shift a waveform either above or below a given reference voltage without distorting the waveform.

- There are two types of clampers: the *positive clamper* and the *negative clamper.*

1. A **positive clamper** shifts its input waveform so that the *negative* peak of the waveform is equal to the clamper dc reference voltage.

   For example: Fig. 2-54 shows what happens when a 20 V_{pp} sin wave is applied to a positive clamper with a dc reference of 0 V. The input and output waveforms have the value of 20 V_{pp}. However, the clamper output waveform has the positive peak of +20 V and the negative peak of 0 V. The positive clamper has shifted the entire waveform so that its negative peak is equal to the circuit's dc reference voltage.



UNIT-III

BIPOLAR JUNCTION TRANSISTOR

- Introduction, Transistor structure
- Current components & their relations
- PNP & NPN transistors, Active mode of operations, Symbols & conversion,
- Transistor equations
- Transistor as an amplifier,
- Input & output characteristics of Common Base (CB), Common Emitter (CE), and Common Collector (CC) configurations,
- DC analysis of CB, CE and CC circuits

Prepared
by
Mr. M.A Vijay Kamalnath,
Asst.Prof, Dept.of ECE,
RGMCET, Nandyal.

Introduction

- **IN THIS UNIT STUDENTS WILL LEARN**
  - The physical structure of the bipolar transistor and how it works.
  - How the voltage between two terminals of the transistor controls the current that flows through the third terminal, and the equations that describe these current-voltage relationships.
  - How to analyze and design circuits that contain bipolar transistors, resistors, and dc sources.
  - How the transistor can be used to make an amplifier.

Introduction

- **IN THIS CHAPTER YOU WILL LEARN**
  - How to obtain linear amplification from the fundamentally nonlinear BJT.
  - The three basic ways for connecting a BJT to be able to construct amplifiers with different properties.
  - Practical circuits for bipolar-transistor amplifiers that can be constructed by using discrete components.

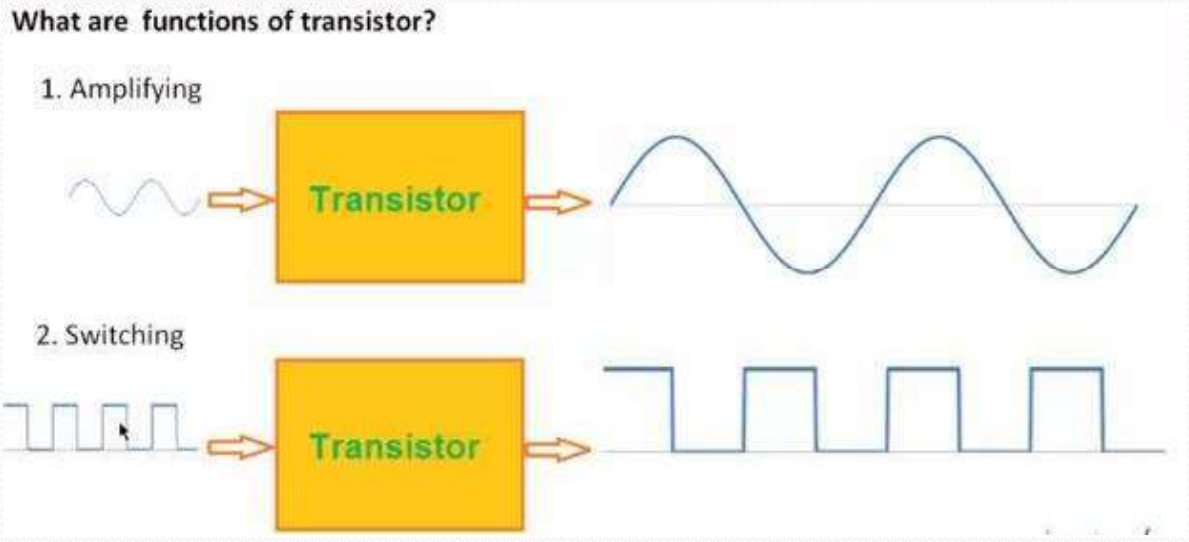
Introduction

- This chapter examines a three-terminal device.
  - **bipolar junction transistor**
- BJT was invented in 1948 at Bell Telephone Laboratories.
  - Ushered in a new era of solid-state circuits.
  - It was replaced by MOSFET as predominant transistor used in modern electronics.

Introduction

- Three-terminal devices are more useful than two-terminal ones, such as the diodes, because they can be used in a multitude of applications:
  1. signal amplification
  2. design of digital logic and memory circuits.
- The basic principle is the use of the voltage between two terminals to control the current flowing in the third terminal.
- In this way, a three-terminal device can be used to realize a controlled source.

Introduction



6.1. Device Structure and Physical Operation

- Figure 6.1 shows simplified structure of BJT.
- Consists of three semiconductor regions:
  - **emitter** region (*n*-type)
  - **base** region (*p*-type)
  - **collector** region (*n*-type)
- Type described above is referred to as *npn*.
  - However, *pnp* types do exist.

6.1. Device Structure and Physical Operation

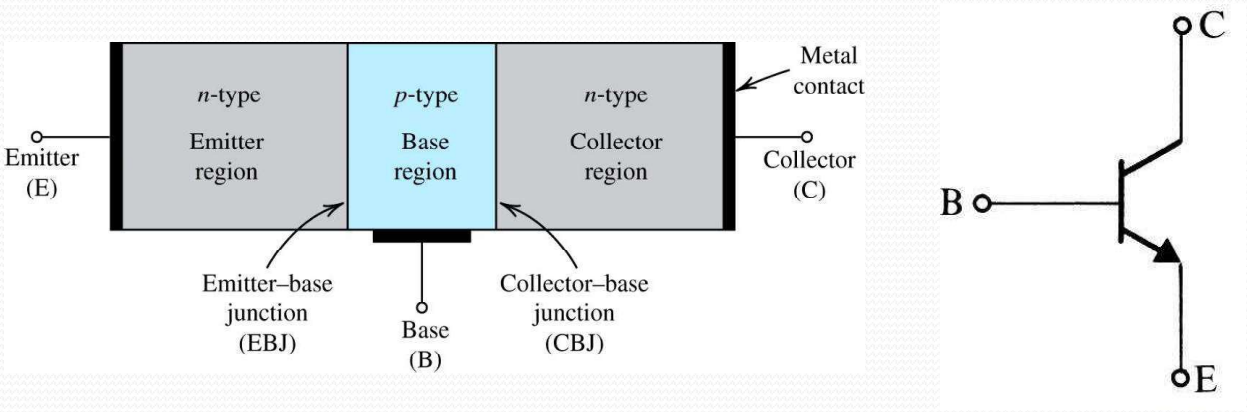


Figure 6.1: A simplified structure of the *npn* transistor.

6.1. Device Structure and Physical Operation

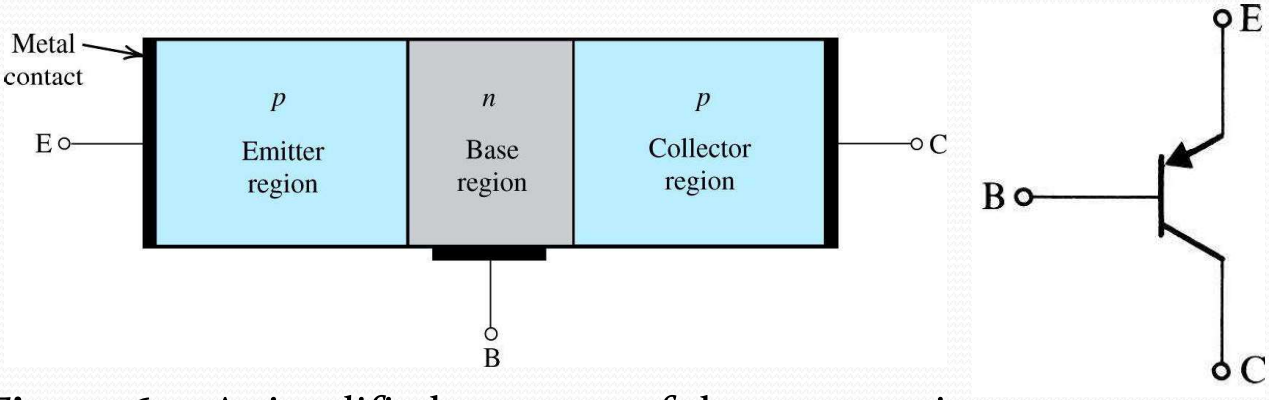


Figure 6.2: A simplified structure of the *pnp* transistor.

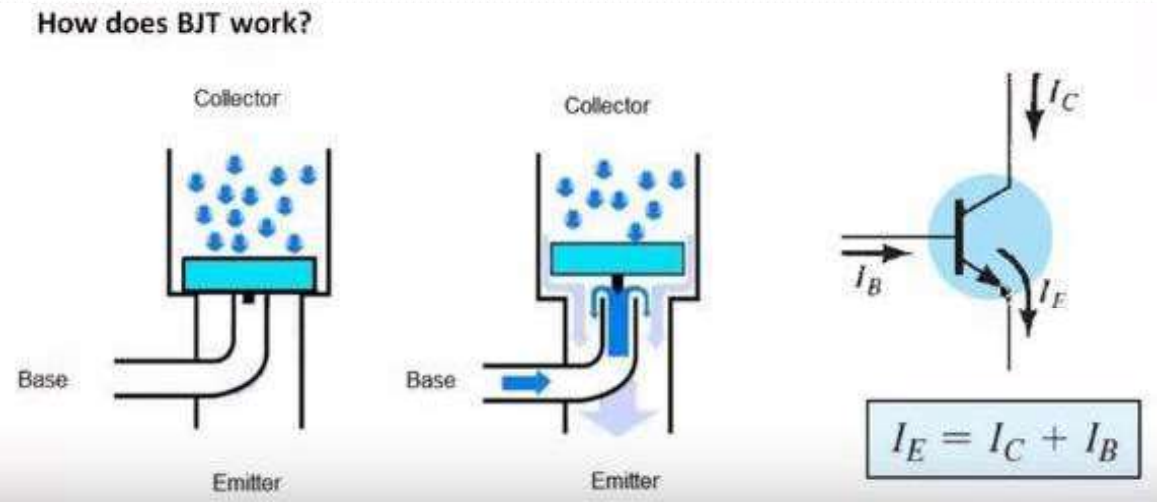
6.1.1. Simplified Structure and Modes of Operation

- Transistor consists of two *pn*-junctions:
  - **emitter-base** junction (EBJ)
  - **collector-base** junction (CBJ)
- Operating mode depends on biasing.
  - **active** mode – used for amplification
  - **cutoff** and **saturation** modes – used for switching.

Table 6.1 BJT Modes of Operation

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

6.1. Device Structure and Physical Operation



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6.1.2. Operation of the *npn*-Transistor in the Active Mode

- Active mode is the "most important."
- Two external voltage sources are required for biasing to achieve it.
- Refer to Figure 6.3.

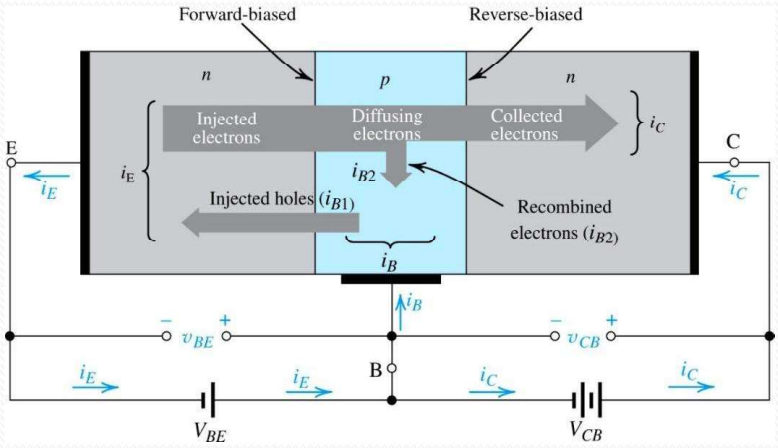

Figure 6.3: Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

The Collector Current

- It is observed that most diffusing electrons will reach boundary of collector-base depletion region.
- Because collector is more positive than base, these electrons are swept into collector.
  - **collector current** (i_C) is approximately equal to I_n.
  - $i_C = I_n$

(eq6.3) $i_C = I_S \mathbf{e}^{v_{BE}/V_T}$

saturation current: $I_S = \dfrac{A_E q D_n n_{p0}}{W}$

(eq6.4) $I_S = \dfrac{A_E q D_n}{W} \dfrac{n_i^2}{N_A}$

ni= intrinsic carrier density
NA= doping concentration of base

The Collector Current

- Magnitude of i_C is independent of v_{CB}.
  - As long as collector is positive, with respect to base.
- **saturation current** (I_S) – is inversely proportional to W and directly proportional to area of EBJ.
  - Typically between 10^{-12} and $10^{-18} A$
  - Also referred to as **scale current**.

The Base Current

β= transistor parameter

(eq6.5) $$i_B = \frac{i_C}{\beta}$$

(eq6.6) $$i_B = \frac{I_S}{\beta} \mathbf{e}^{v_{BE}/V_T}$$

The Base Current

- **common-emitter current gain** (β) – is influenced by two factors:
  - width of base region (W)
  - relative doping of base emitter regions (N_A/N_D)
- High Value of β
  - thin base (small W in nano-meters)
  - lightly doped base / heavily doped emitter (small N_A/N_D)

    β is in the range 50 to 200

The Emitter Current

- All current which enters transistor must leave.
  - $i_E = i_C + i_B$
- Equations (6.7) through (6.13) expand upon this idea.

this expression is generated through combination of (6.5) and (6.7)

(eq6.8/6.9) $$i_E = \frac{\beta+1}{\beta} i_C = \frac{\beta+1}{\beta}\underbrace{\left(I_S \mathbf{e}^{v_{BE}/V_T}\right)}_{i_C}$$

(eq6.10) $$i_C = \alpha i_E$$

---

this parameter is reffered to as **common-base current gain**

(eq6.11) $$\alpha = \frac{\beta}{\beta+1}$$, (eq6.13) $$\beta = \frac{\alpha}{1-\alpha}$$

(eq6.12) $$i_E = \frac{I_S}{\alpha}\mathbf{e}^{v_{BE}/V_T}$$

Recapitulation and Equivalent-Circuit Models

- Next slides present first-order BJT model.
  - Assumes *npn* transistor in active mode.
- Basic relationship is collector current (i_C) is related exponentially to forward-bias voltage (v_{BE}).
  - It remains independent of v_{CB} as long as this junction remains reverse biased.
    - $v_{CB} > 0$
- Thus in the active mode the collector terminal behaves as an ideal constant-current source where the value of the current is determined by v_{BE}.

Thus α is called the common-base current gain.

Thus β is called the common-emitter current gain.

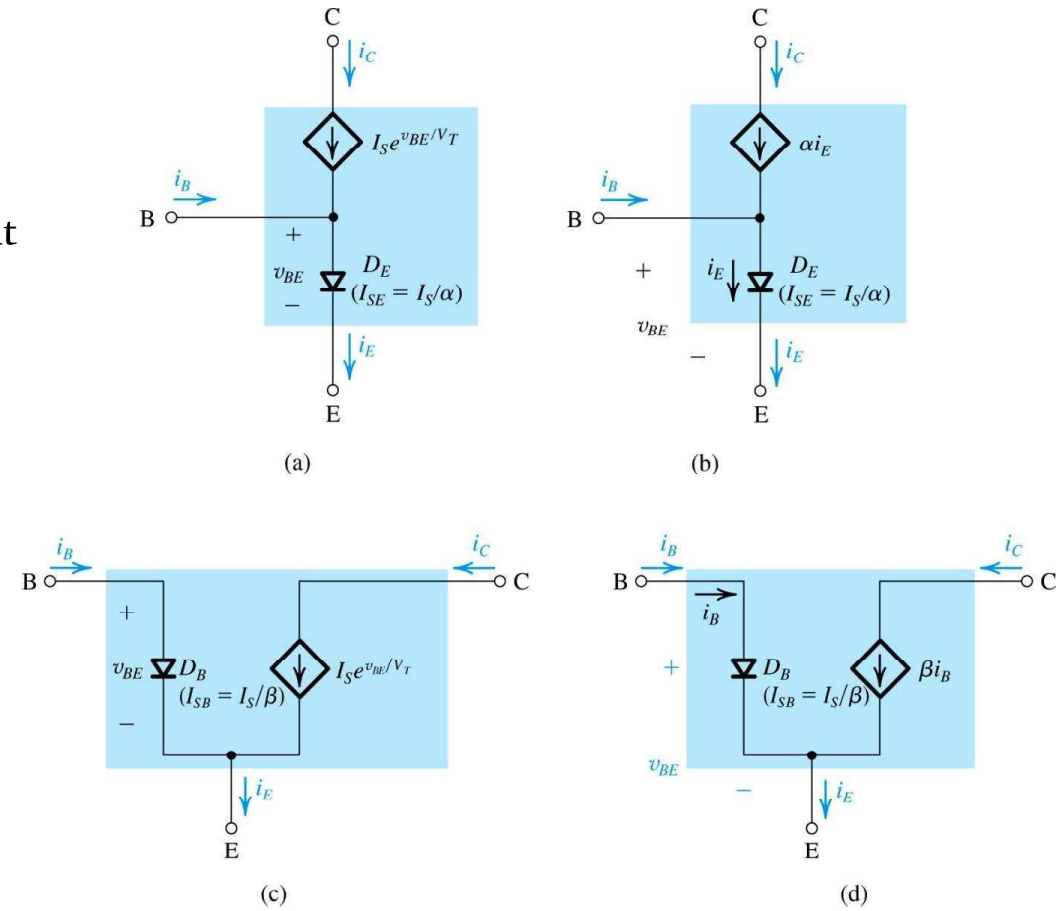

Figure 6.4: Large-signal equivalent-circuit models of the *npn* BJT operating in the active mode (a), (b) common base configuration. (c), (d) common emitter configuration.

6.1.4. Operation in Saturation Mode

- For BJT to operate in active mode, CBJ must be reverse biased.
  - However, for small values of forward-bias, a *pn*-junction does not operate effectively.
- As such, active mode operation of *npn*-transistor may be maintained for v_{CB} down to approximately -0.4V.
  - Only after this point will "diode" begin to really conduct.

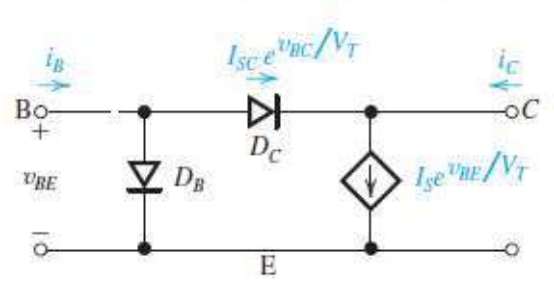

Figure 6.5 Modeling the operation of an *npn* transistor in saturation by augmenting the model of Fig. 6.5(c) with a forward conducting diode *DC*. Note that the current through *DC* increases i_B and reduces i_C.

6.1.4. Operation in Saturation Mode

(eq6.14) collector current in saturation region : $i_C = \overbrace{I_S e^{v_{BE}/V_T}}^{I_{SC}=} - \underbrace{I_{SC} e^{v_{BC}/V_T}}_{\text{this terms plays bigger role as } v_{BC} \text{ exceeds 0.4V}}$

(eq6.15) base current in saturation region : $i_B = \frac{I_S}{\beta} e^{v_{BE}/V_T} + I_{SC} e^{v_{BC}/V_T}$

(eq6.16) forced β : $\underbrace{\beta_{forced} = \left.\frac{i_C}{i_B}\right|_{saturation} \le \beta}_{\text{As } v_{BC} \text{ is increased, the value of } \beta \text{ is forced lower and lower.}}$

6.1.4. Operation in Saturation Mode

- Two questions must be asked to determine whether BJT is in saturation mode, or not:
  - Is the CBJ forward-biased by more than $0.4V$?
  - Is the ratio i_C/i_B less than β?
- The collector-to-emitter voltage v_{CE} of a saturated transistor can be found from Fig. 6.9 as the difference between the forward-bias voltages of the EBJ and the CBJ,

$$V_{CEsat} = V_{BE} - V_{BC}$$

- Recalling that the CBJ has a much larger area than the EBJ, V_{BC} will be smaller than V_{BE} by 0.1 to 0.3 V. Thus,

$$V_{CEsat} \simeq 0.1 \; to \; 0.3 \text{ V}$$

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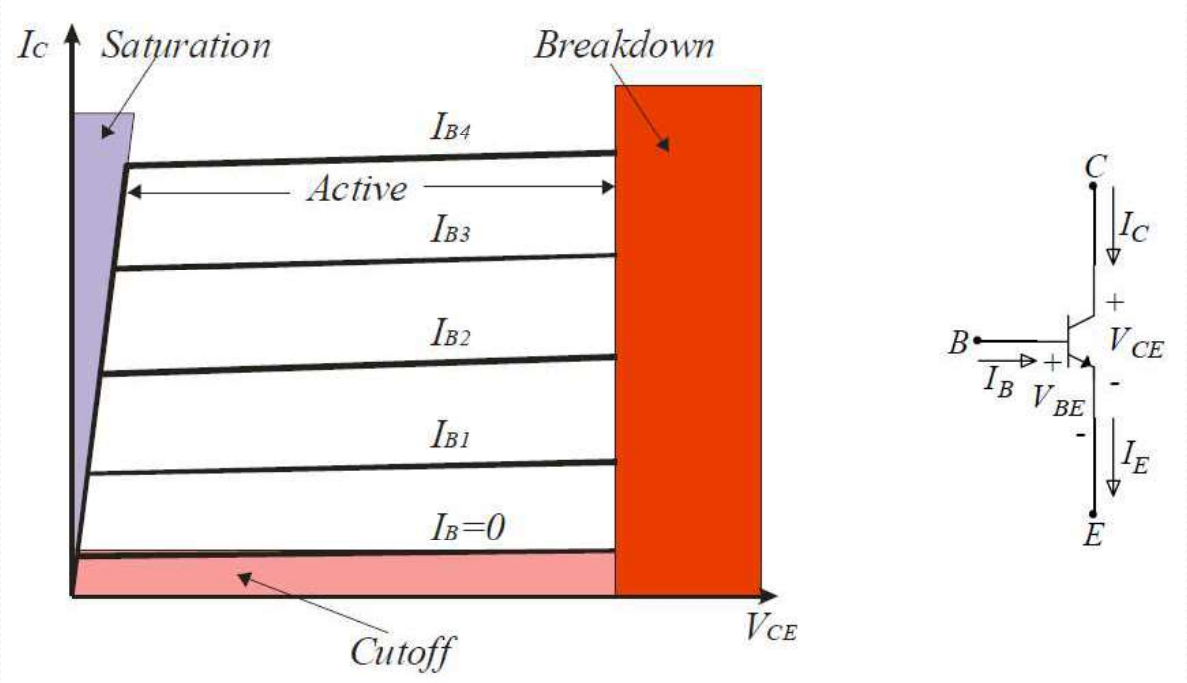
BJT regions of operation



The characteristics of each region of operation are summarized below.

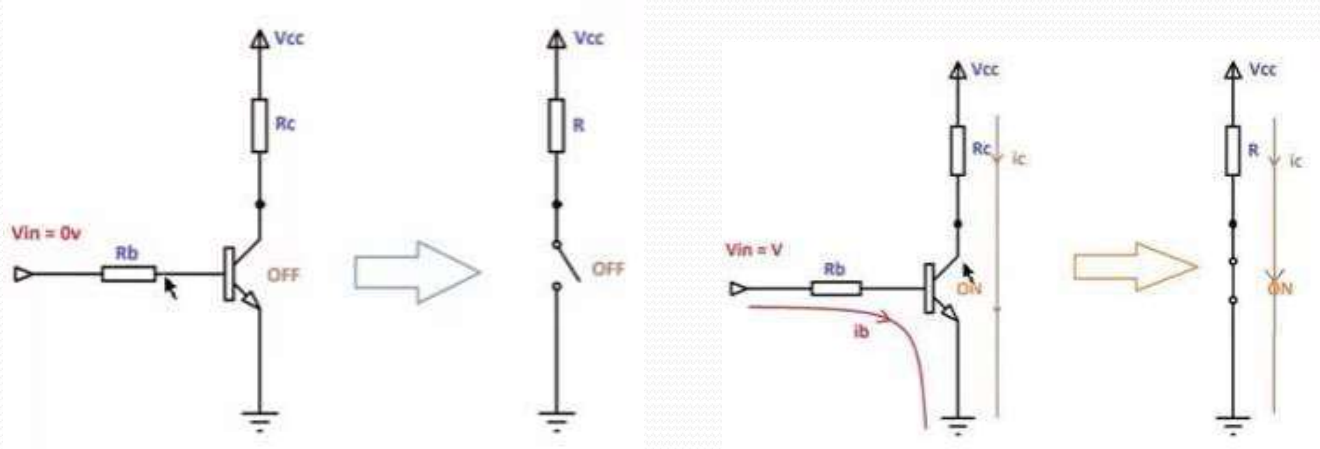
1. **cutoff region:**
   B-E junction is reverse biased. No current flow

2. **saturation region:**
   B-E and C-B junctions are forward biased
   Ic reaches a maximum which is independent of I_B and β.
   $V_{CE} < V_{BE}$. No control.

3. **active region:**
   B-E junction is forward biased, C-B junction is reverse biased
   $V_{BE} < V_{CE} < V_{CC}$, $I_C = \beta I_B$. Control

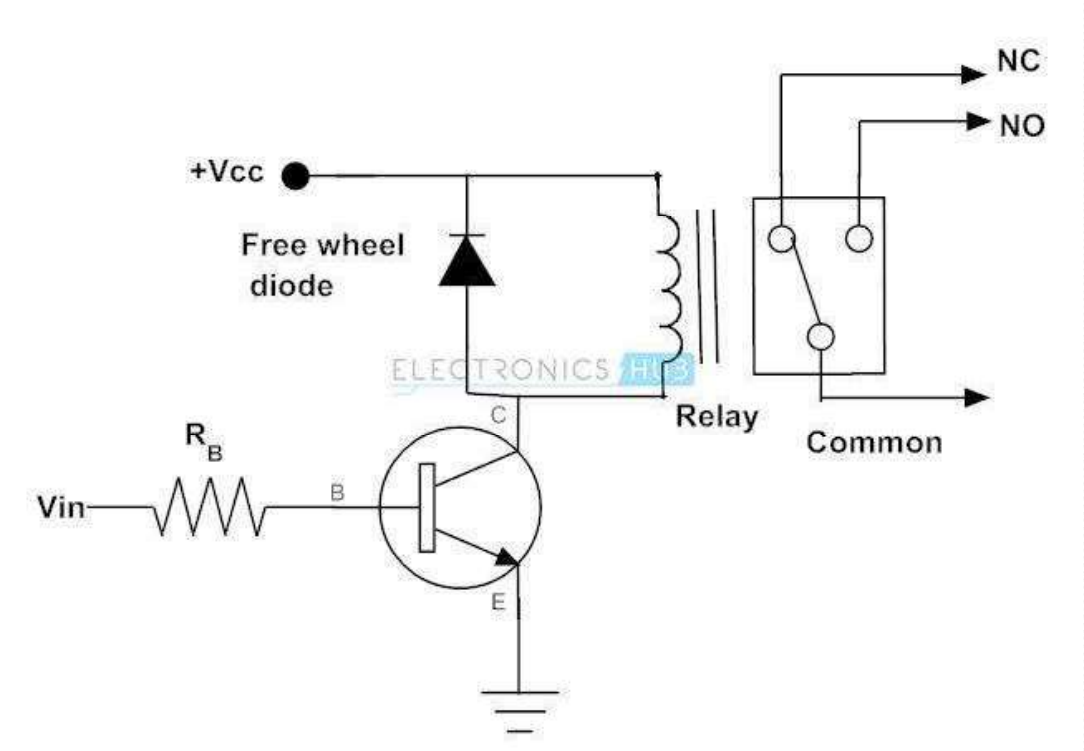
4. **breakdown region:**
   I_C and V_{CE} exceed specifications
   damage to the transistor

BJT applications



NPN BJT switch circuit

BJT applications



NPN BJT switch circuit

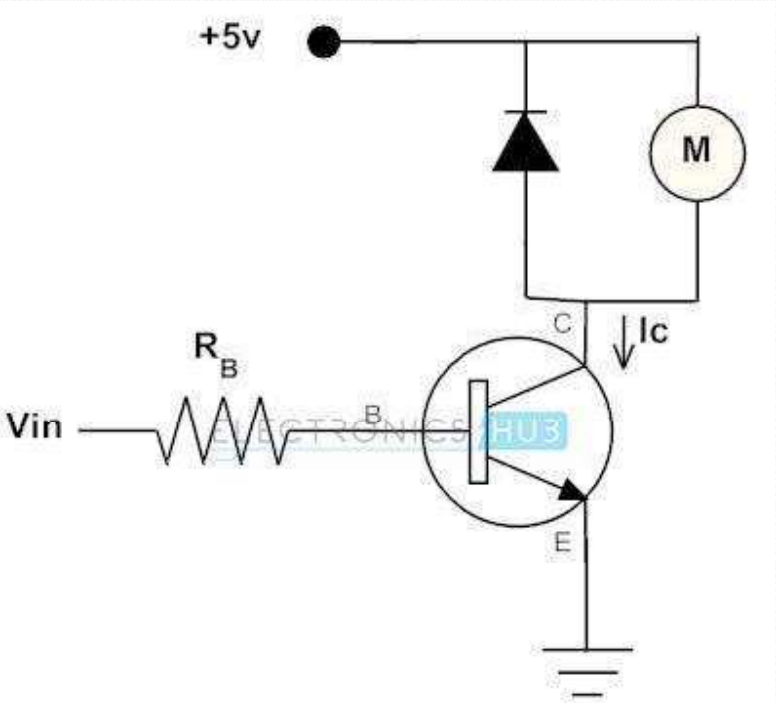
Use relay to separate the control circuit from the high current/voltage electrical circuit

BJT applications

Transistor to Drive the Motor

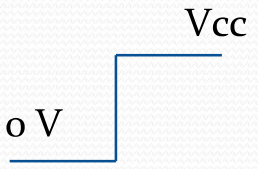
- A transistor can also used to drive and regulate the speed of the DC motor in a unidirectional way by switching the transistor in regular intervals of time.
- the DC motor is also an inductive load so we have to place a freewheeling diode across it to protect the circuit.
- By switching the transistor in cutoff and saturation regions, we can turn ON and OFF the motor repeatedly.
- It is also possible to regulate the speed of the motor from standstill to full speed by switching the transistor at variable frequencies. We can get the switching frequency from control device or IC like microcontroller.

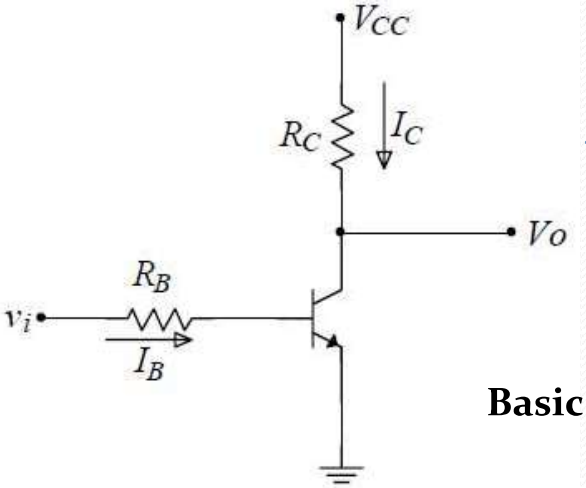
BJT applications

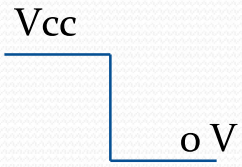


Control the speed of motor using Pulse Width Modulation
The duty cycle of input digital signal controls the DC level applied to the motor

BJT applications







Basic BJT inverter circuit

If the voltage v_i is zero (**low**) the transistor is in the cutoff region, the current $I_c = 0$ and the voltage $V_0 = V_{cc}$ (**high**).

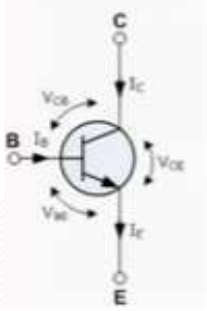
By contrast if the voltage v_i is **high**, say equal to V_{cc}, the transistor is driven into saturation and the output is equal to $V_{CE}(sat)$ which is **low**.

BJT Specs

Datasheet

MAXIMUM RATINGS

Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	–55 to +150	°C



FAIRCHILD
SEMICONDUCTOR TM

2N4123

TO-92

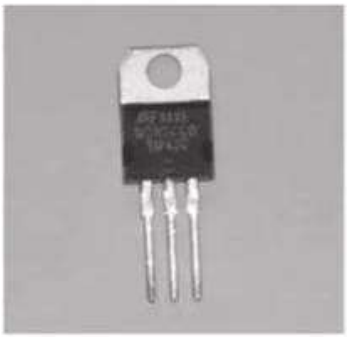
General Purpose
Transistor
NPN Silicon

$$P_D = I_C \times V_{CE}$$

BJT Specs

TRANSISTOR CASING AND TERMINAL IDENTIFICATION

low power



medium power

medium to high power

Why holes
To fix heat sink for cooling

6.2.1. Circuit Symbols and Conventions

Table 6.2 Summary of the BJT Current–Voltage Relationships in the Active Mode

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}.

$$i_C = \alpha i_E \qquad i_B = (1-\alpha) i_E = \frac{i_E}{\beta+1}$$

$$i_C = \beta i_B \qquad i_E = (\beta+1) i_B$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1}$$

V_T = thermal voltage $= \dfrac{kT}{q} \simeq 25$ mV at room temperature

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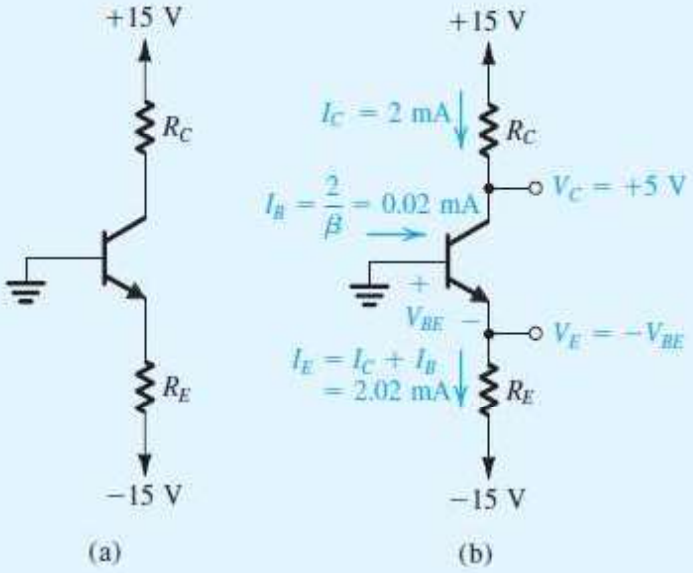
EXAMPLE 6.1

The transistor in the circuit of Fig (a) has $\beta = 100$ and exhibits a v_{BE} of 0.7 V at $i_C = 1$ mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +5 V appears at the collector.



EXAMPLE 6.1 - Sol

since we are required to design for $V_C = +5$ V, the CBJ will be reverse biased and the BJT will be operating in the active mode. To obtain a voltage $V_C = +5$ V, the voltage drop across R_C must be 15 – 5 = 10 V.

since $I_C = 2$ mA, the value of R_C should be selected according to

$$R_C = \frac{10 \text{ V}}{2 \text{ mA}} = 5 \text{ k}\Omega$$

Since $v_{BE} = 0.7$ V at $i_C = 1$ mA, the value of v_{BE} at $i_C = 2$ mA is

$$V_{BE} = 0.7 + V_T \ln\left(\frac{2}{1}\right) = 0.717 \text{ V}$$

Since the base is at 0 V, the emitter voltage should be

$$V_E = -0.717 \text{ V}$$

For $\beta = 100$, $\alpha = 100/101 = 0.99$. Thus the emitter current should be

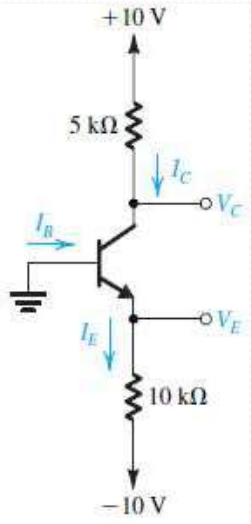
$$I_E = \frac{I_C}{\alpha} = \frac{2}{0.99} = 2.02 \text{ mA}$$

Now the value required for R_E can be determined from

$$R_E = \frac{V_E - (-15)}{I_E} = \frac{-0.717 + 15}{2.02} = 7.07 \text{ k}\Omega$$

EXAMPLE 6.2

In the circuit shown in the figure, the voltage at the emitter was measured and found to be –0.7 V. If β = 50, find I_E, I_B, I_C, and V_C.



Ans. 0.93 mA; 18.2 μA; 0.91 mA; +5.45 V

EXERCISE 6.2 - Sol

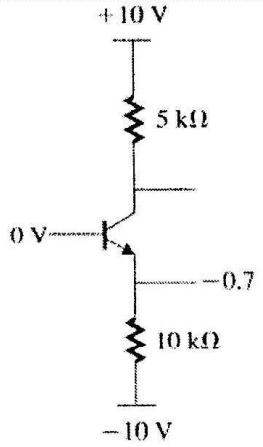


Fig 6.13

$\beta = 50, V_{BE} = 0.7$ V

$V_E = V_B - 0.7$ V

$= 0 - 0.7 = -0.7$ V

$$I_E = \frac{-0.7 + 10}{10\ \text{K}}$$

$= 0.93$ mA

$$I_C = \frac{50}{51} I_E = 0.91\ \text{mA}$$

$V_C = 10 - 0.91 \times 5$

$= 5.45$ V

$$I_B = \frac{I_C}{\beta} = \frac{0.91}{50}$$

$= 0.0182\ \mu\text{A}$

6.2.3. Dependence of i_C on Collector Voltage – The Early Effect

- When operated in active region, practical BJT's show some dependence of collector current on collector voltage.
- As such, i_C-v_{CB} characteristic is not "straight".

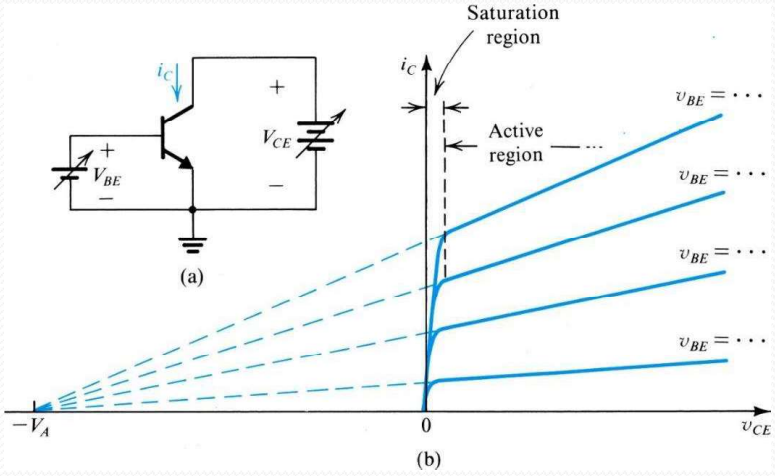


Figure 6.6 (a) Conceptual circuit for measuring the i_C–v_{CE} characteristics of the BJT. **(b)** The i_C–v_{CE} characteristics of a practical BJT.

6.2.3. Dependence of i_C on Collector Voltage – The Early Effect

$$r_o \equiv \left[\left.\frac{\partial i_C}{\partial v_{CE}}\right|_{v_{BE}=\text{constant}}\right]^{-1}$$

$$r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CE_Q}}{I_{C_Q}}$$

$$r_o \cong \frac{V_A}{I_{C_Q}}$$

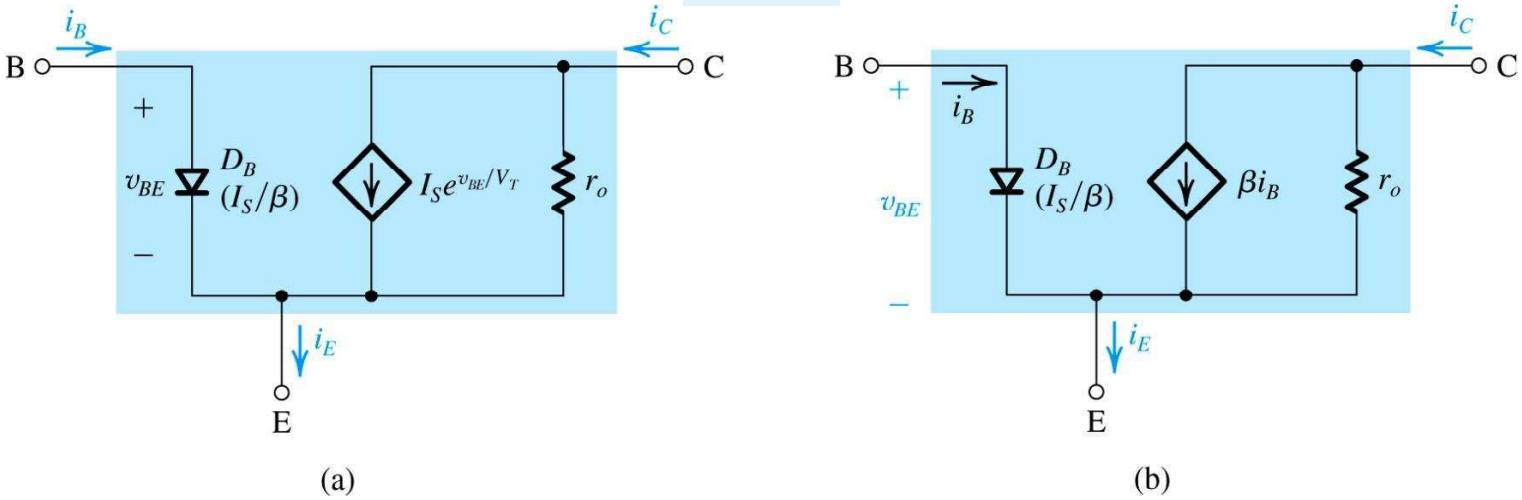


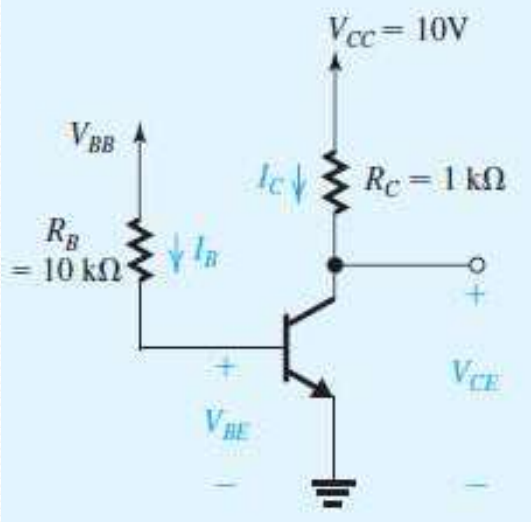
Figure 6.7: Large-signal equivalent-circuit models of an *npn* BJT operating in the active mode in the common-emitter configuration with the output resistance r_o included.

Example 6.3

For the circuit in Fig. , it is required to determine the value of the voltage V_{BB} that results in the transistor operating

(a) in the active mode with $V_{CE} = 5$ V
(b) at the edge of saturation
(c) deep in saturation with $\beta_{forced} = 10$

For simplicity, assume that V_{BE} remains constant at 0.7 V. The transistor β is specified to be 50.



Example 6.3 - Sol

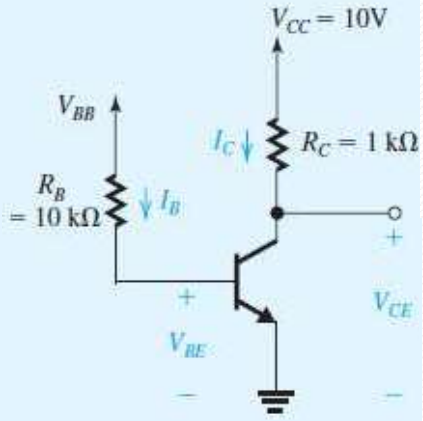
Solution

(a) To operate in the active mode with $V_{CE} = 5$ V,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$= \frac{10 - 5}{1\ \text{k}\Omega} = 5\ \text{mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{5}{50} = 0.1\ \text{mA}$$



Now the required value of V_{BB} can be found as follows:

$$V_{BB} = I_B R_B + V_{BE}$$

$$= 0.1 \times 10 + 0.7 = 1.7\ \text{V}$$

(b) Operation at the edge of saturation is obtained with $V_{CE} = 0.3$ V. Thus

$$I_C = \frac{10 - 0.3}{1} = 9.7\ \text{mA}$$

Since, at the edge of saturation, I_C and I_B are still related by β.

$$I_B = \frac{9.7}{50} = 0.194\ \text{mA}$$

Example 6.3 - Sol

The required value of V_{BB} can be determined as

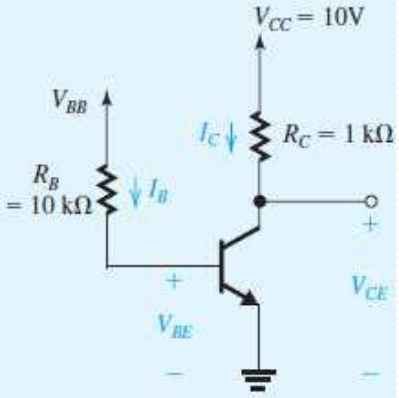
$$V_{BB} = 0.194 \times 10 + 0.7 = 2.64 \text{ V}$$

(c) To operate deep in saturation,

$$V_{CE} = V_{CEsat} \simeq 0.2 \text{ V}$$

Thus,

$$I_C = \frac{10 - 0.2}{1} = 9.8 \text{ mA}$$



We then use the value of forced β to determine the required value of I_B as

$$I_B = \frac{I_C}{\beta_{\text{forced}}} = \frac{9.8}{10} = 0.98 \text{ mA}$$

and the required V_{BB} can now be found as

$$V_{BB} = 0.98 \times 10 + 0.7 = 10.5 \text{ V}$$

Observe that once the transistor is in saturation, increasing V_{BB} and thus I_B results in negligible change in I_C since V_{CEsat} will change only slightly. Thus I_C is said to *saturate*, which is the origin of the name "saturation mode of operation."

EXAMPLE 6.4

For the circuit in Fig 6.8 , let V_{BB} be set to the value obtained in Example 6.3, part (a), namely, $V_{BB} = 1.7$ V. Verify that the transistor is indeed operating in the active mode. Now, while keeping V_{BB} constant, find that value to which R_C should be increased in order to obtain (a) operation at the edge of saturation, and (b) operation deep in saturation with $\beta_{\text{forced}} = 10$.

For $V_{BB} = 1.7$ V

$$I_B = \frac{1.7 - 0.7}{10} = 0.1 \text{ mA}$$

$$I_C = \beta I_B$$

$$= 50 \times 0.1 = 5 \text{ mA}$$

$$V_C = 10 - 5 \times 1 \text{ k}\Omega$$

$$= +5 \text{ V} > V_{BE} \text{ (so Active)}$$

(a) edge of saturation $V_{CE} = 0.3$ V

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10 - 0.3}{5} = 1.94 \text{ k}\Omega$$

(b) deep saturation $v_{CE} = 0.2$ V

$$I_B = 0.1 \text{ mA (unchanged)}$$

$$I_C = \beta_{Forced} I_B = 10 \times 0.1 = 1 \text{ mA}$$

$$R_C = \frac{10 - 0.2}{1 \text{ mA}} = 9.8 \text{ k}\Omega$$

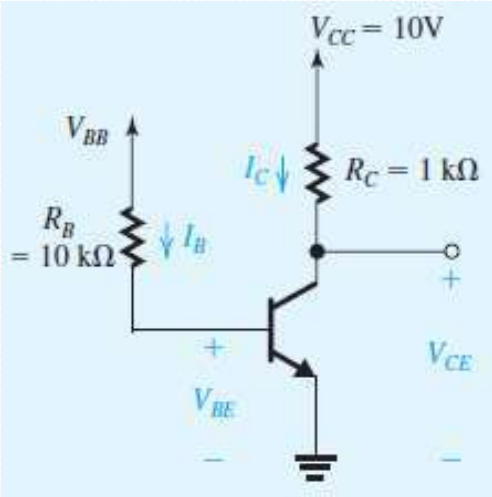


Figure 6.8

Summary

- Depending on the bias condition on its two junctions, the BJT can operate in one of three possible modes:
  - **cut-off** (both junctions reverse biased)
  - **active** (the EBJ forward-biased and CBJ reversed)
  - **saturation** (both junctions forward biased)
- For amplifier applications, the BJT is operated in the active mode. Switching applications make use of the cutoff and saturation modes.
- A BJT operating in the active mode provides a collector current $i_C = I_S \mathbf{exp}\{v_{BE}/V_T\}$. The base current $i_B = i_C/\beta$, and emitter current $i_E = i_C + i_B$.

Summary

- To ensure operation in the active mode, the collector voltage of an *npn*-transistor must be kept higher than approximately $0.4V$ below the base voltage. For a *pnp*-transistor, the collector voltage must be lower than approximately $0.4V$ above the base voltage. Otherwise, the CBJ becomes forward-biased and the transistor will enter saturation.
- At a constant collector current, the magnitude of the base emitter voltage decreases by about $2mV$ for every $1^{O}C$ rise in temperature.
- The BJT will be at the edge of saturation when $|v_{CE}|$ is reduced to about $0.3V$.

Summary

- In the active mode, i_C shows a slight dependence on v_{CE}. This phenomenon, known as the Early Effect, is modeled by ascribing a finite output resistance to the BJT: $r_o = |V_A|/I'_C$ where V_A is the Early Voltage and I'_C is the dc collector current without the Early Effect taken into account.
- The dc analysis of transistor circuits is generally simplified by assuming $|V_{BE}| = 0.7V$.

BJT Circuits at DC

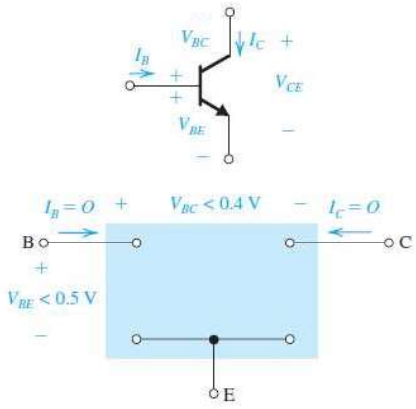
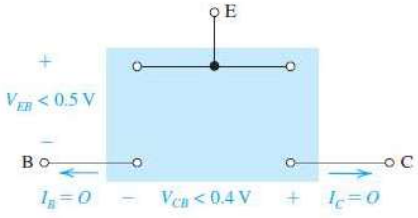
in analyzing a circuit the first question that one must answer is: *In which mode is the transistor operating*?

1. quick check of the terminal voltages.
2. Assume that the transistor is operating in the active mode, and determine the various voltages and currents that correspond.

- Then check for consistency of the results with the assumption of active-mode operation ($v_{CB} > -0.4$ volt);
- If the answer is no, assume saturation-mode then test
- compute the ratio I_C/I_B and to verify that it is lower than the transistor β (i.e., $\beta_{forced} < \beta$).

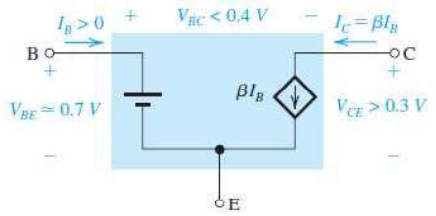
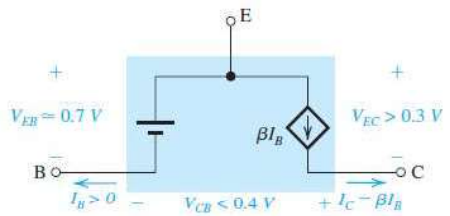
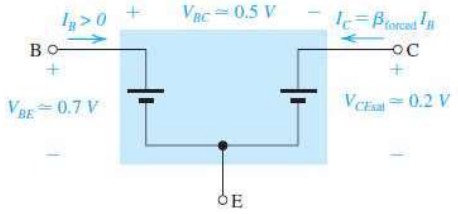
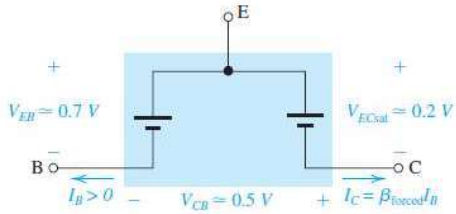
BJT Circuits at DC

Table 6.3 Conditions and Models for the Operation of the BJT in Various Modes

	npn	*pnp*
Cutoff EJB: Reverse Biased CBJ: Reverse Biased		

BJT Circuits at DC

Table 6.3 Conditions and Models for the Operation of the BJT in Various Modes

	npn	*pnp*
Active EBJ: Forward Biased CBJ: Reverse Biased		
Saturation EBJ: Forward Biased CBJ: Forward Biased		

Example 6.5

Consider the circuit shown in Fig. 6.9(a), which is redrawn in Fig. 6.9(b) to remind the reader of the convention employed throughout this book for indicating connections to dc sources. We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that β is specified to be 100.

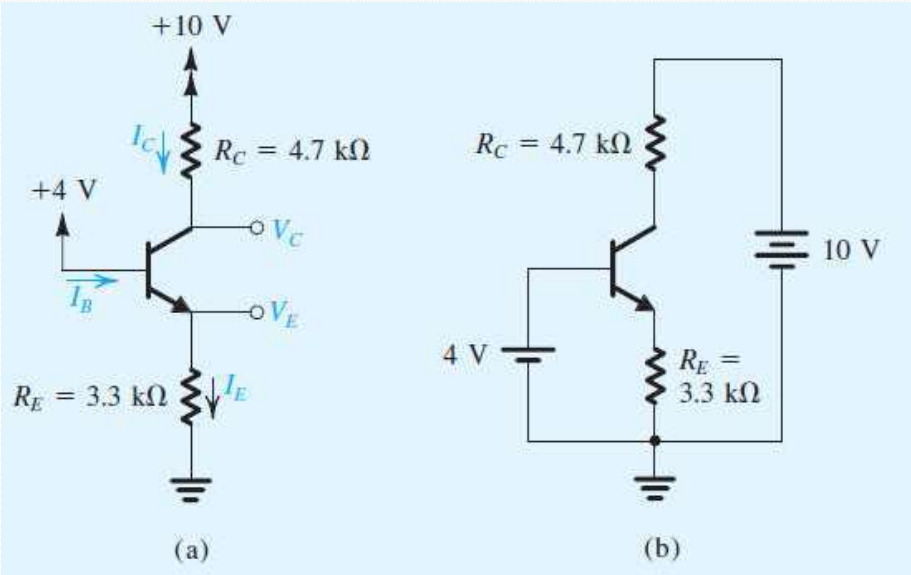
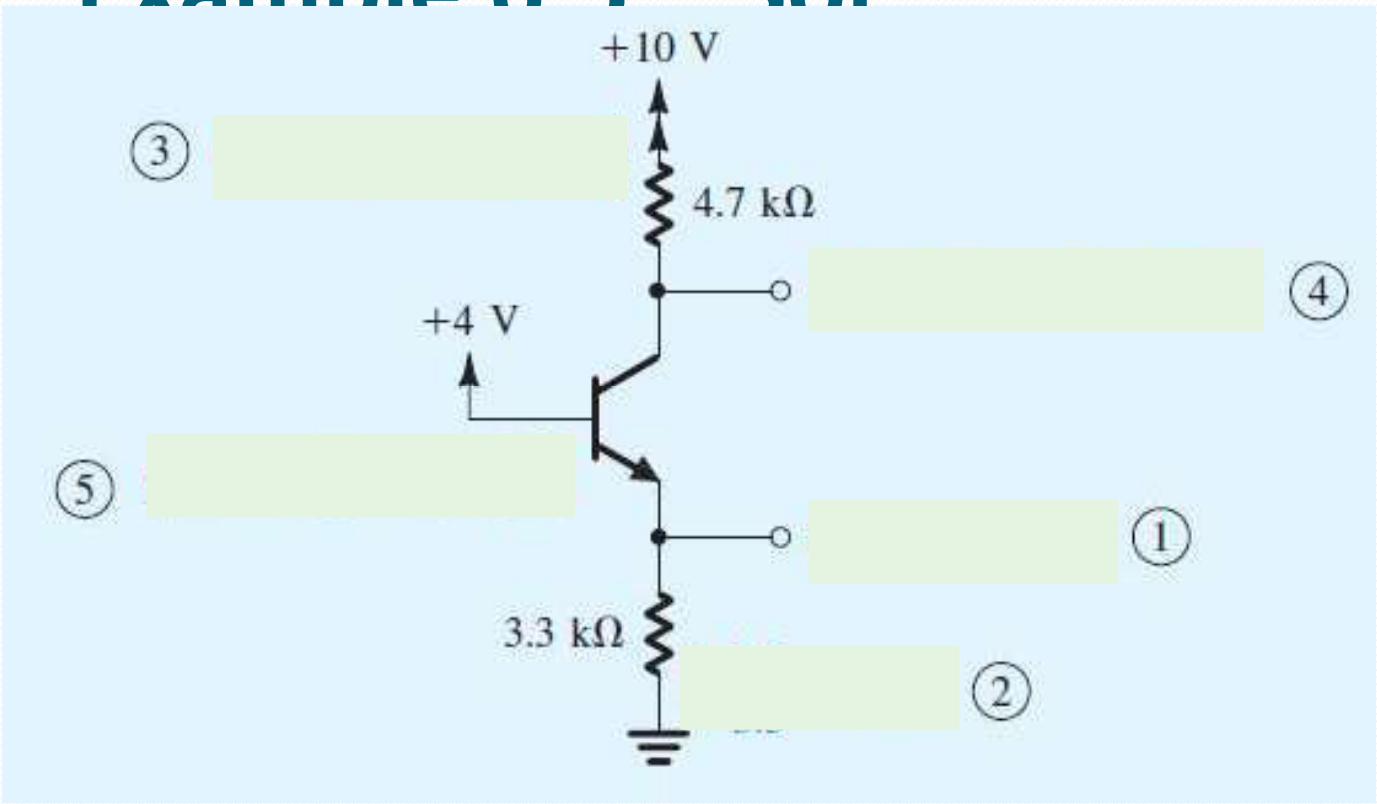


Figure 6.9

Example 6.5 – Sol



Example 6.6

We wish to analyze the circuit of Fig. 6.10 to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 1 except that the voltage at the base is now +6 V. Assume that the transistor β is specified to be *at least* 50.

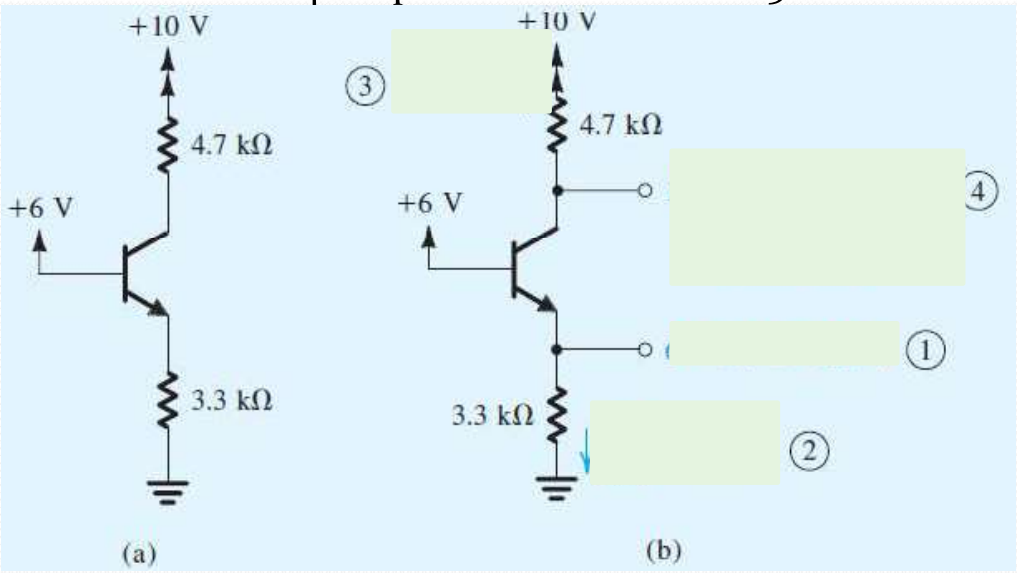
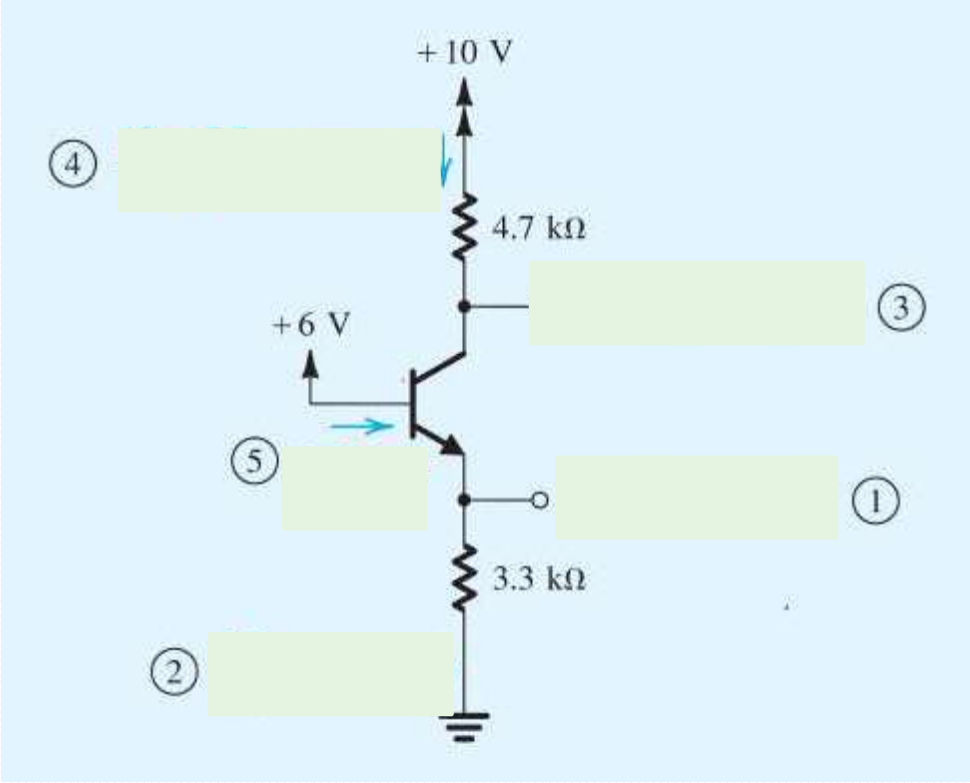


Figure 6.10 Analysis of the circuit for Example 6.7.

Example 6.6 – Sol.

Active mode assumption is not correct because $V_C < V_B$



Example 6.6 – Sol

$$V_C = V_E + V_{CEsat} \simeq +5.3 + 0.2 = +5.5\ \text{V}$$

from which we can determine I_C as

$$I_C = \frac{+10 - 5.5}{4.7} = 0.96\ \text{mA}$$

and I_B can now be found as

$$I_B = I_E - I_C = 1.6 - 0.96 = 0.64\ \text{mA}$$

Thus the transistor is operating at a forced β of

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{0.96}{0.64} = 1.5$$

Since β_{forced} is less than the *minimum* specified value of β, the transistor is indeed saturated. We should emphasize here that in testing for saturation the minimum value of β should be used. By the same token, if we are designing a circuit in which a transistor is to be saturated, the design should be based on the minimum specified β.

Example 6.7

We want to analyze the circuit of Fig. 6.11 (a) to determine the voltages at all nodes and the currents through all branches.

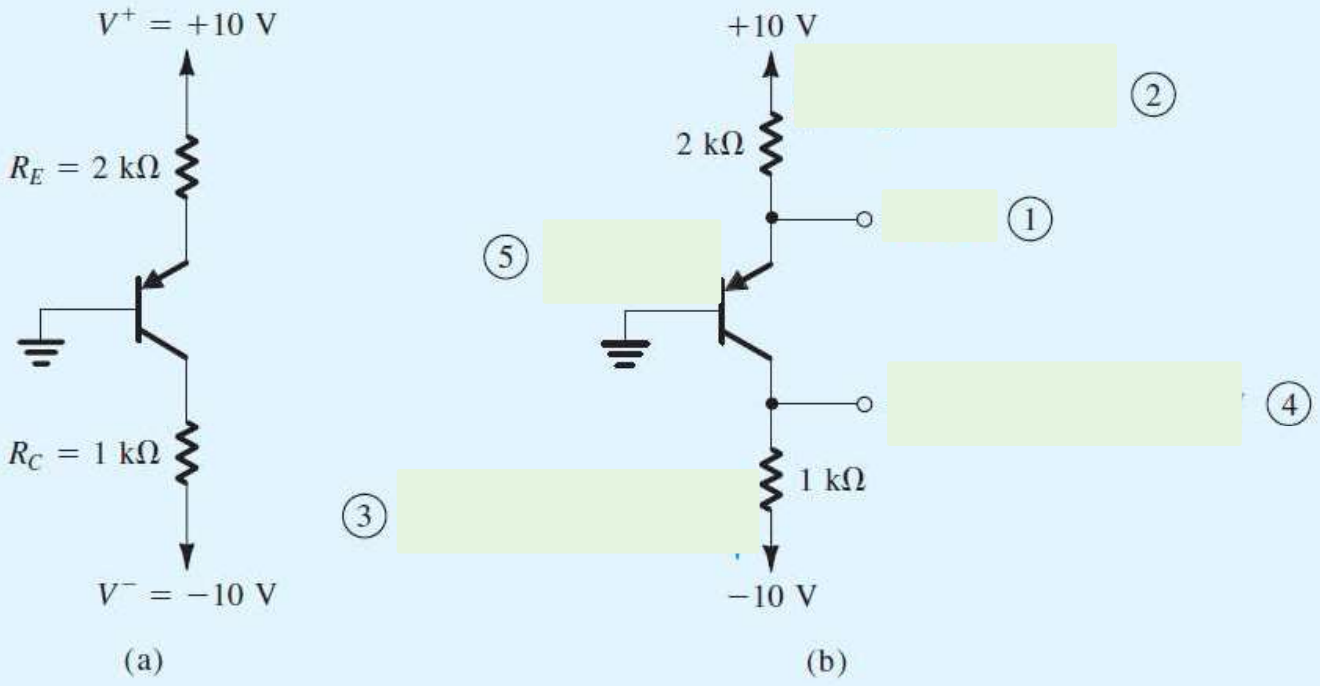


Figure 6.11 **(a)** circuit; **(b)** analysis, with the steps indicated by circled numbers.

Example 6.8

We want to analyze the circuit, shown in the figure below, to determine the voltages at all nodes and the currents through all branches. Assume β = 100.

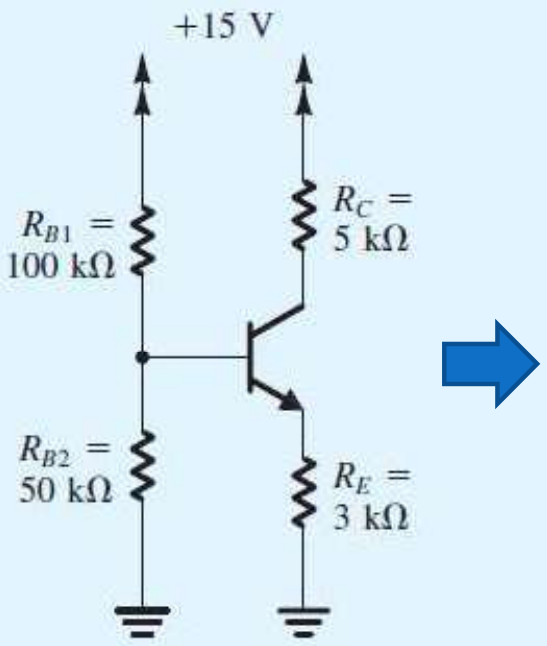


Figure 6.12 (a)

Example 6.8

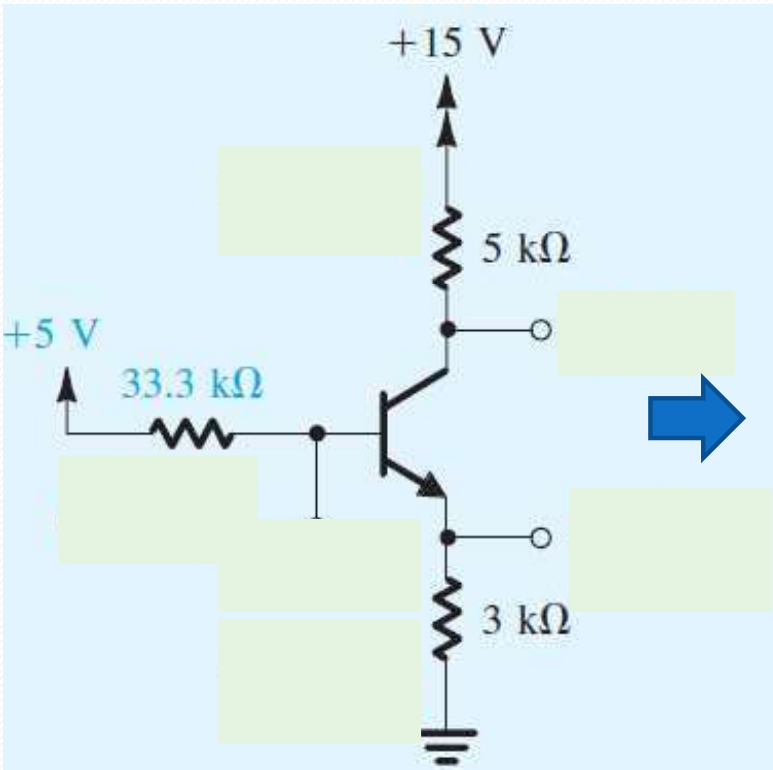
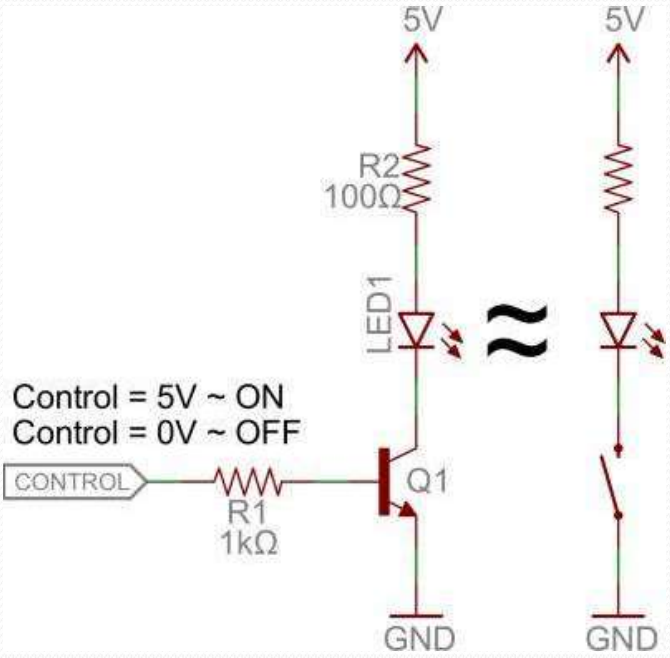
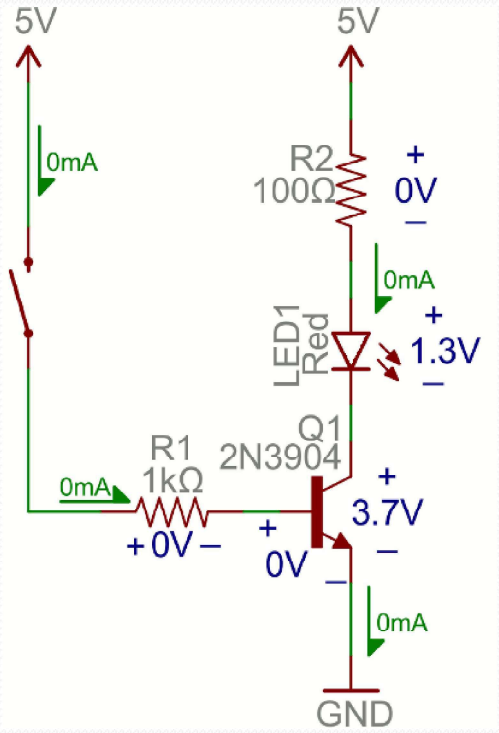


Figure 6.12 (c)

Applications

Transistor Switch





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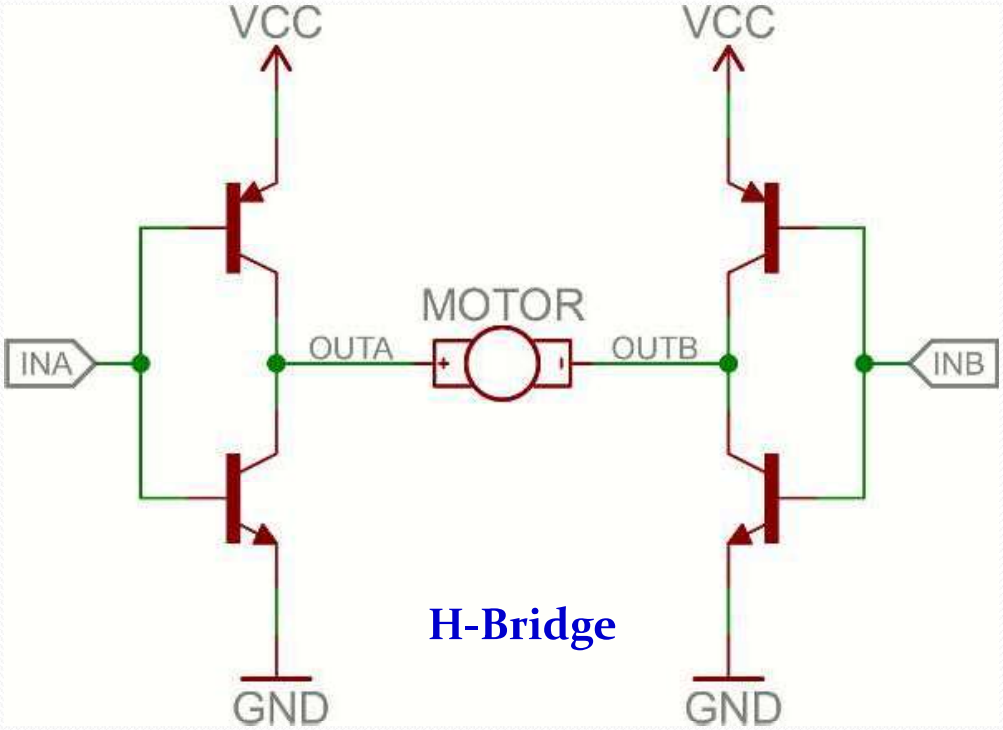
Applications

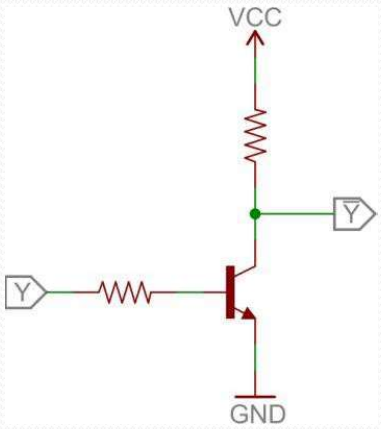
An H-bridge is a transistor-based circuit capable of **driving motors both clockwise and counter-clockwise**.



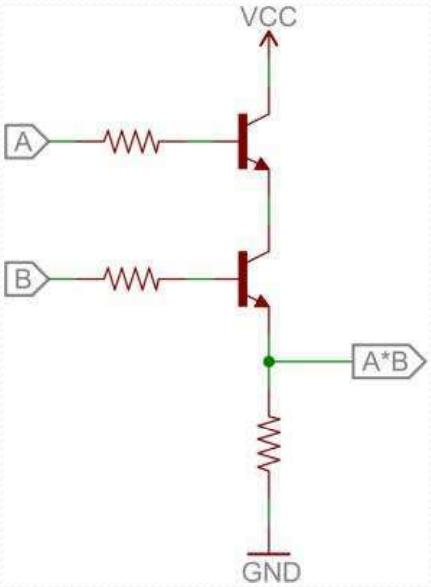
H-Bridge

Applications

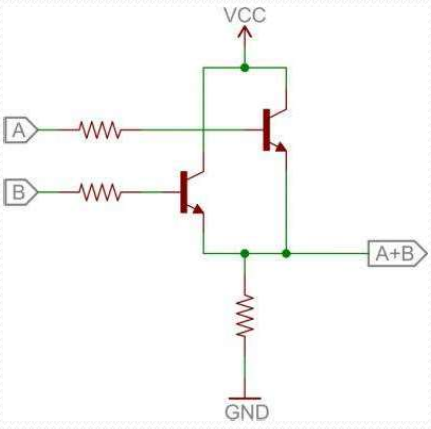
Digital Logic



Not Gate



AND Gate



OR Gate

Design Examples

Relay Driver

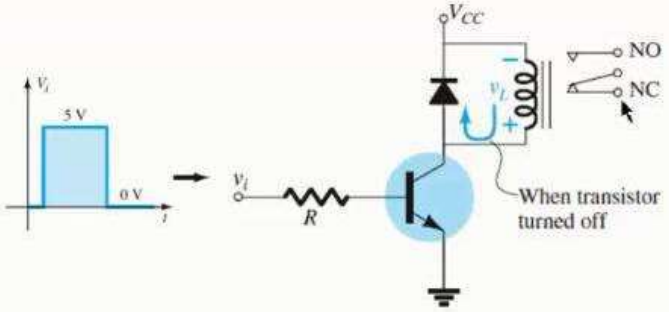
Ex:

Relay coil = 6 v, 100 Ohm

High input level = 5 V

maximum source current 20 mA

Design transistor relay driver



At off: $V_{CE(max)}$ For transistor >= 1.5 * 6 = 9 V → $V_{CE(max)}$ For transistor >= 9 V

$I_{C(sat)} = V_{CC} / R_C = 6 / 100 = 60$ mA → $I_{C(max)}$ For transistor = 1.5 * 60 = 90 mA → $I_{C(max)}$ For transistor >= 90 mA

To saturate the transistor with the lowest β, we need to provide a base current at least

$I_B = I_{C(sat)} / B_{min} = 60$ mA / 35 = 1.7 mA

$I_{B(sat)} = (5 : 10) * I_B$ → $I_{B(sat)} = 5 * I_B = 5 * 1.7 = 8.5$ mA < $I_{source(max)}$

I_B for transistor >= 1.5 * $I_{B(sat)}$ = 1.5 * 8.5 mA = 12.8mA → I_B for transistor >= 12.8 mA

$R_B = (V_i - V_{BE}) / I_{B(sat)} = (5 - 0.7) / 0.0085 = 506$ Ohm → (470, 510 Ohm --> E24 >< 487, 511 Ohm --> E48)

$P_{RB} = (V_i - V_{BE}) * I_B = (5 - 0.7) * 8.5$mA = 37 mWatt → 37 mW * 1.5 = 55.5 mW

Design Examples

I_{CBO}	collector cut-off current 2N2222	$I_E = 0$; $V_{CB} = 50$ V	–	10	nA
		$I_E = 0$; $V_{CB} = 50$ V; $T_{amb} = 150$ °C	–	10	µA
I_{CBO}	collector cut-off current 2N2222A	$I_E = 0$; $V_{CB} = 60$ V	–	10	nA
		$I_E = 0$; $V_{CB} = 60$ V; $T_{amb} = 150$ °C	–	10	µA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = 3$ V	–	10	nA
h_{FE}	DC current gain	$I_C = 0.1$ mA; $V_{CE} = 10$ V	35	–	
		$I_C = 1$ mA; $V_{CE} = 10$ V	50	–	
		$I_C = 10$ mA; $V_{CE} = 10$ V	75	–	
		$I_C = 150$ mA; $V_{CE} = 1$ V; note 1	50	–	
		$I_C = 150$ mA; $V_{CE} = 10$ V; note 1	100	300	
h_{FE}	DC current gain 2N2222A	$I_C = 10$ mA; $V_{CE} = 10$ V; $T_{amb} = -55$ °C	35	–	

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Design Examples

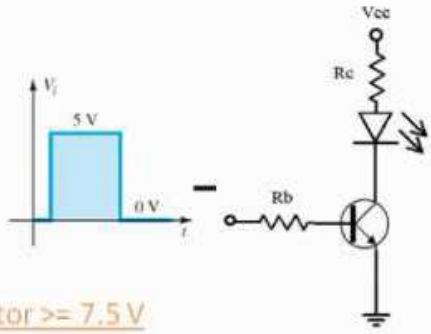
Ex:

Led Driver

Red Led= 2V, 20 mA (max) , Vcc = 5 V

High input level = 5 V , maximum source current 10 mA

Design transistor led driver



At off: $V_{CE(max)}$ For transistor >= 1.5 * 5 = 7.5 V → $V_{CE(max)}$ For transistor >= 7.5 V

$R_C = (V_{CC} - V_{LED}) / I_{LED} = (5 - 2) / 15mA = 200$ Ohm

$P_{LED} = V_{LED} * I_{LED} = 2 * 15$ mA = 30 mWatt → 30 mW * 1.5 = 45mW

$P_{RC} = V_{RC} * I_{RC} = (5 - 2) * 15$ mA = 45 mWatt → 45 mW * 1.5 = 67.5mW

$I_{C(sat)} = 15mA$ → $I_{C(max)}$ For transistor = 1.5 * 15 = 22.5 mA → $I_{C(max)}$ For transistor >= 30 mA

$I_B = I_{C(sat)} / B_{min} = 15$ mA / 35 = 0.43 mA

$I_{B(sat)} = (5 : 10) * I_B$ → $I_{B(sat)} = 5 * I_B = 5 * 0.43 = 2.15$ mA $< I_{source(max)}$

I_B for transistor >= 1.5 * $I_{B(sat)}$ = 1.5 * 2.15 mA = 3.225mA → I_B for transistor >= 3.224 mA

$R_B = (V_i - V_{BE}) / I_{B(sat)} = (5 - 0.7) / 2.15$ mA = 2000 Ohm

$P_{RB} = (V_i - V_{BE}) * I_B = (5 - 0.7) * 2.15$mA = 9.245 mWatt → 9.245mW * 1.5 = 14 mW

UNIT-IV

BIASING OF BJTs

Load line and mode of operations
Operating point, Bias stability
Fixed Bias, Self bias
Stabilization against variation in Ico, $V_{BE,}$
Bias compensation
Thermal runaway, condition for thermal stability

Prepared
by
Mr. M.A Vijay Kamalnath,
Asst.Prof, Dept.of ECE,
RGMCET, Nandyal.

Transistor Biasing

The basic function of transistor is amplification. The process of raising the strength of weak signal without any change in its general shape is referred as faithful amplification. For faithful amplification it is essential that:-

1. Emitter-Base junction is forward biased
2. Collector- Base junction is reversed biased
3. Proper zero signal collector current

The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is called transistor biasing.

WHY BIASING?

- If the transistor is not biased properly, it would work inefficiently and produce distortion in output signal.

HOW A TRANSISTOR CAN BE BIASED?

- A transistor is biased either with the help of battery or associating a circuit with the transistor.
- The later method is more efficient and is frequently used. The circuit used for transistor biasing is called the biasing circuit.

BIAS STABILITY

❖ Through proper biasing, a desired quiescent operating point of the transistor amplifier in the active region (linear region) of the characteristics is obtained. It is desired that once selected the operating point should remain stable. The maintenance of operating point stable is called Stabilisation.

❖ The selection of a proper quiescent point generally depends on the following factors:

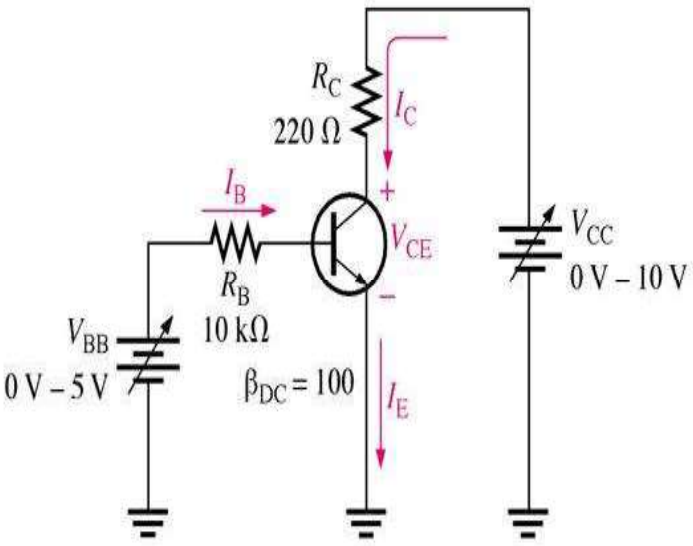
(a) The amplitude of the signal to be handled by the amplifier and distortion level in signal

(b) The load to which the amplifier is to work for a corresponding supply voltage

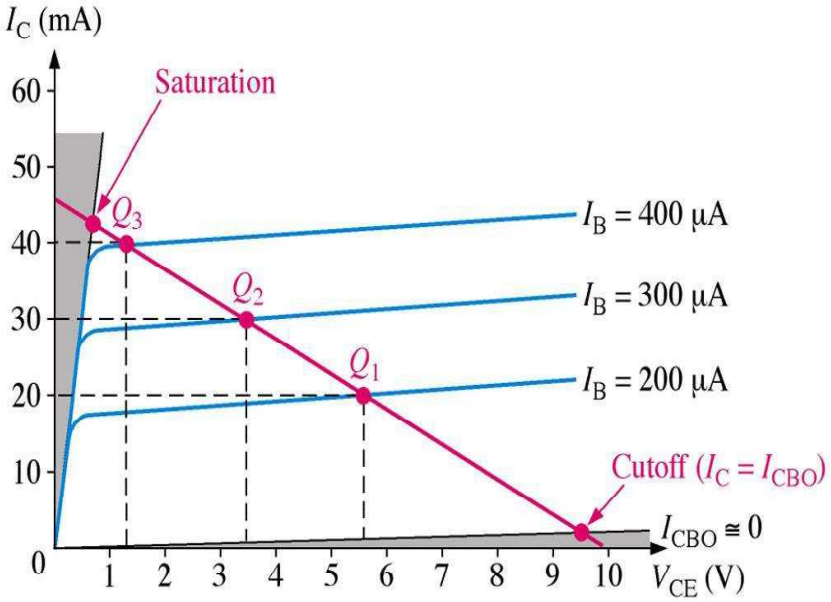
❖ The operating point of a transistor amplifier shifts mainly with changes in temperature, since the transistor parameters — *β, I_{CO} and V_{BE} (where the symbols carry their usual meaning)—are functions of* temperature.

The DC Operating Point

For a transistor circuit to amplify it must be properly biased with dc voltages. The dc operating point between saturation and cutoff is called the **Q-point.** The goal is to set the Q-point such that that it does not go into saturation or cutoff when an a ac signal is applied.



(a) DC biased circuit



Requirements of biasing network

- Ensuring proper zero signal collector current.
- Ensuring V_{CE} not falling below 0.5V for Ge transistor and 1V for Silicon transistor at any instant.
- Ensuring Stabilization of operating point. (zero signal I_C and V_{CE})

The Thermal Stability of Operating Point (S_{Ico})

❖**Stability Factor *S*:-** The stability factor *S, as the change of collector current with respect to the reverse saturation* current, keeping β *and VBE constant. This can be written as:*

The Thermal Stability Factor : S_{Ico}

$$S_{Ico} = \left.\frac{\partial I_c}{\partial I_{co}}\right|_{V_{be},\ \beta}$$

This equation signifies that I_c Changes S_{Ico} times as fast as I_{co}

Differentiating the equation of Collector Current $I_C = (1+\beta)I_{co} + \beta I_b$ & rearranging the terms we can write

$$S_{Ico} = \frac{1+\beta}{1-\beta\,(\partial I_b/\partial I_C)}$$

It may be noted that Lower is the value of S_{Ico} better is the stability

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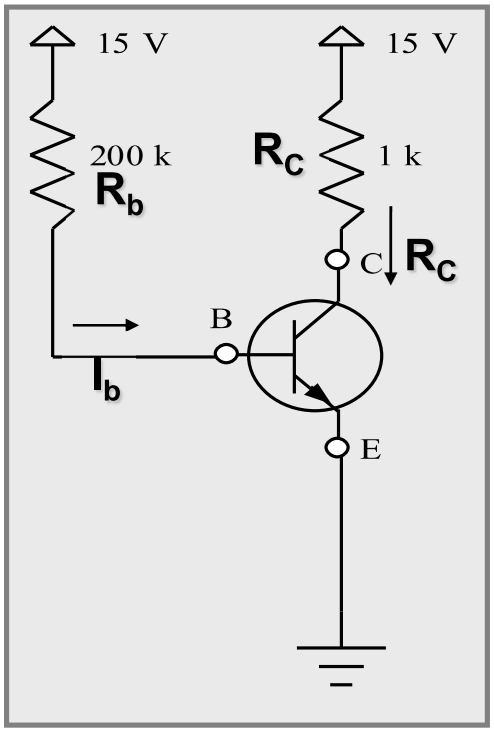
Various Biasing Circuits

- **Fixed Bias Circuit**
- **Fixed Bias with Emitter Resistor**
- **Collector to Base Bias Circuit**
- **Potential Divider Bias Circuit**

The Fixed Bias Circuit



The Thermal Stability Factor : S_{Ico}

$$S_{Ico} = \frac{\partial I_c}{\partial I_{co}}\Bigg|_{V_{be},\ \beta}$$

General Equation of S_{Ico} Comes out to be

$$S_{Ico} = \frac{1 + \beta}{1 - \beta\ (\partial I_b / \partial I_C)}$$

Applying KVL through Base Circuit we can write, $I_b R_b + V_{be} = V_{cc}$

Diff w. r. t. I_C, we get $(\partial I_b / \partial I_c) = 0$

$S_{Ico} = (1+\beta)$ is very large

Indicating high un-stability

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

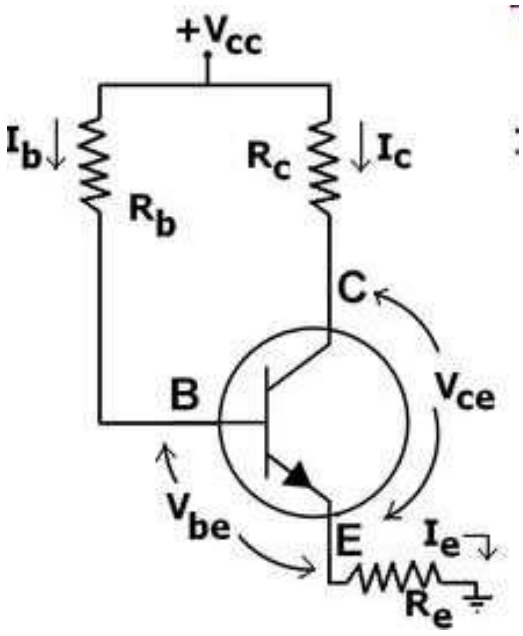
- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.
- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

Usage:

- Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where transistor is used as a switch. However, one application of fixed bias is to achieve crude automatic gain control in the transistor by feeding the base resistor from a DC signal derived from the AC output of a later stage.

Fixed bias with emitter resistor

The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point.



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Merits:

• The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits:

• As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.

➢ If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.

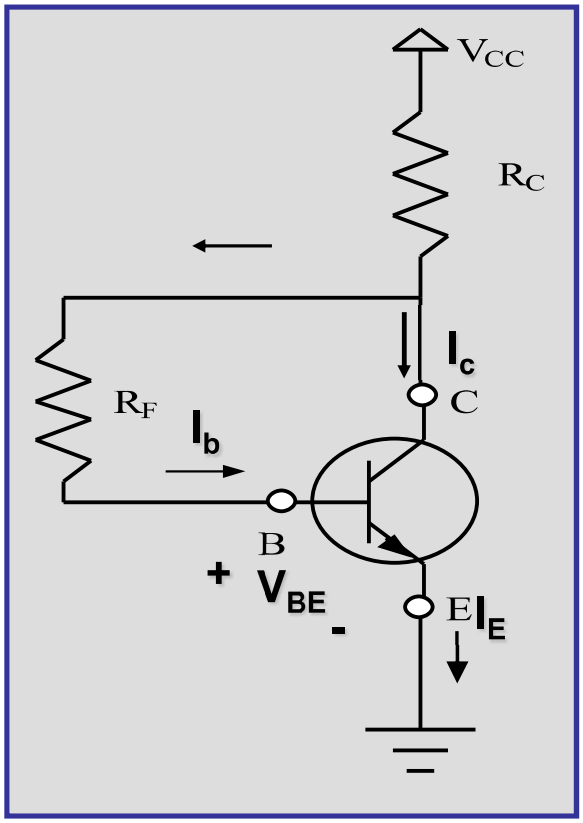
➢ If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.

• In addition to the above, R_E causes ac feedback which reduces the voltage gain of the amplifier.

Usage:

The feedback also increases the input impedance of the amplifier when seen from the base, which can be advantageous. Due to the above disadvantages, this type of biasing circuit is used only with careful consideration of the trade-offs involved.

The Collector to Base Bias Circuit



This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_F is connected to the collector instead of connecting it to the DC source V_{CC}. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

Applying KVL through base circuit

we can write $(I_b + I_C) R_C + I_b R_f + V_{be} = V_{cc}$

Diff. w. r. t. I_C we get

$$(\partial I_b / \partial I_c) = - R_C / (R_f + R_C)$$

Therefore, $S_{Ico} = \dfrac{(1+\beta)}{1+[\beta R_C/(R_C+R_f)]}$

Which is less than (1+β), signifying better thermal stability

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

• As β -value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_C fairly large or making R_f very low.

- If R_C is large, a high V_{CC} is necessary, which increases cost as well as precautions necessary while handling.
- If R_f is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_f causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

The Potential Divider Bias Circuit

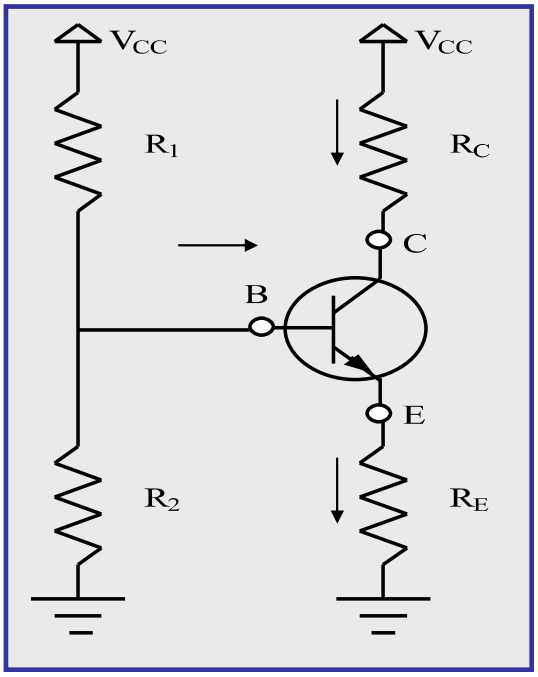
- This is the most commonly used arrangement for biasing as it provide good bias stability. In this arrangement the emitter resistance 'R_E' provides stabilization.

- The resistance 'R_E' cause a voltage drop in a direction so as to reverse bias the emitter junction. Since the emitter-base junction is to be forward biased, the base voltage is obtained from R_1-R_2 network.

- The net forward bias across the emitter base junction is equal to V_B- dc voltage drop across 'R_E'. The base voltage is set by Vcc and R_1 and R_2. The dc bias circuit is independent of transistor current gain.

- In case of amplifier, to avoid the loss of ac signal, a capacitor of large capacitance is connected across R_E. The capacitor offers a very small reactance to ac signal and so it passes through the condenser.

The Potential Divider Bias Circuit



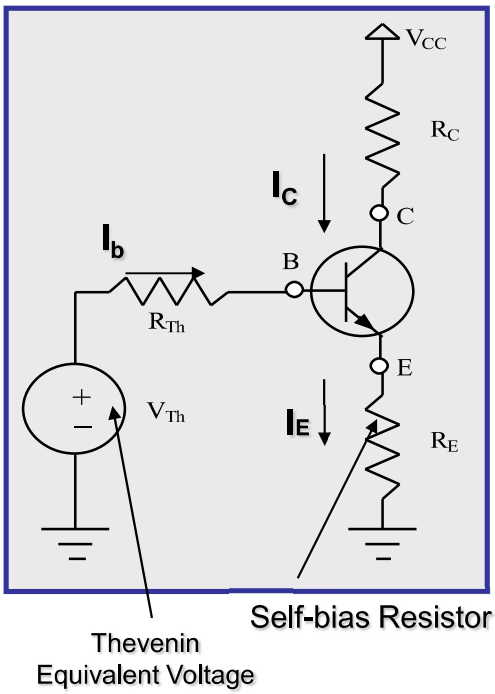
To find the stability of this circuit we have to convert this circuit into its Thevenin's Equivalent circuit

$$R_{th} = \frac{R_1 * R_2}{R_1 + R_2} \quad \& \quad V_{th} = \frac{Vcc\ R_2}{R_1 + R_2}$$

19

The Potential Divider Bias Circuit

Thevenin Equivalent Ckt



Applying KVL through input base circuit

we can write $I_b R_{Th} + I_E R_E + V_{be} = V_{Th}$

Therefore, $I_b R_{Th} + (I_C + I_b) R_E + V_{BE} = V_{Th}$

Diff. w. r. t. I_C & rearranging we get

$(\partial I_b / \partial I_c) = - R_E / (R_{Th} + R_E)$

Therefore, $$S_{Ico} = \frac{1+\beta}{1+\left[\beta \frac{R_E}{R_E + R_{Th}}\right]}$$

This shows that $S_{I_{co}}$ is inversely proportional to R_E and It is less than (1+β), signifying better thermal stability

Merits:

- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making R1||R2 very low.
  - If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
  - If R1 || R2 is low, either R1 is low, or R2 is low, or both are low. A low R1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R2 lowers Vbe, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
  - AC as well as DC feedback is caused by RE, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage:

The circuit's stability and merits as above make it widely used for linear circuits.

Summary

- The Q-point is the best point for operation of a transistor for a given collector current.
- The purpose of biasing is to establish a stable operating point (Q-point).
- The linear region of a transistor is the region of operation within saturation and cutoff.
- Out of all the biasing circuits, potential divider bias circuit provides highest stability to operating point.

UNIT-V&VI

JUNCTION FIELD EFFECT TRANSISTOR

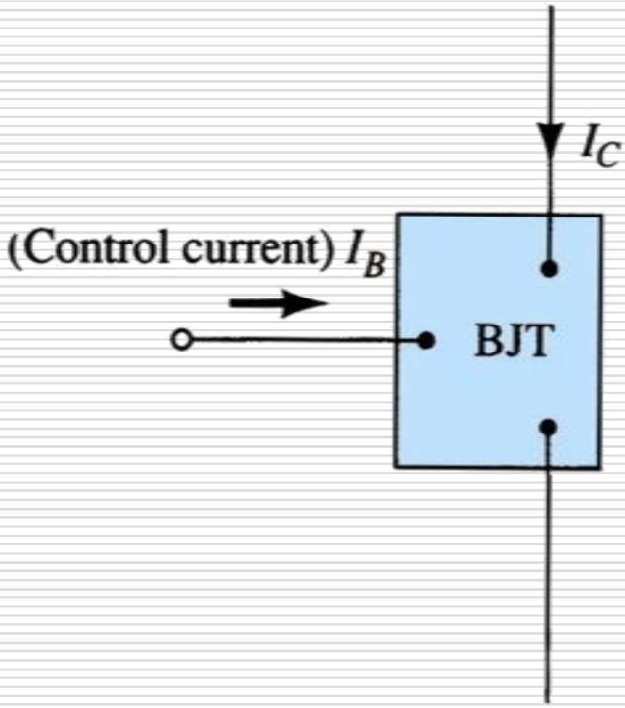
- Introduction, structure
- MOSFET current equation and V-I characteristics
- n-channel MOSFET: Enhancement mode and depletion mode
- p-channel MOSFET: Enhancement mode and depletion mode
- MOSFET Symbols and conversions
- Complementary MOSFETs-Structure, V-I characteristics, symbols and conversions.
- Different configurations using MOSFETs
- Load line and modes of operation
- Different biasing circuits(Self-bias, voltage bias) using MOSFETs
- DC analysis of n-channel MOSFETs (both enhancement & depletion modes)
- Problem solving
- Applications of MOSFETS as switch and small signal amplifiers

Prepared
by
Mr. M.A Vijay Kamalnath,
Asst.Prof, Dept.of ECE,
RGMCET, Nandyal.

Introduction (FET)

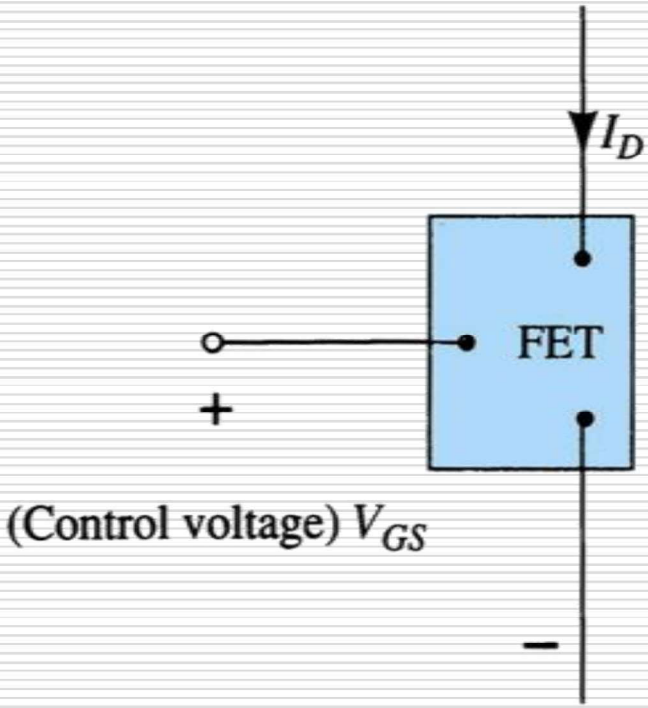
- Field-effect transistor (FET) are important devices such as BJTs
- Also used as amplifier and logic switches
- Types of FET:
  - MOSFET (metal-oxide-semiconductor field-effect transistor)
  - Depletion-mode MOSFET
  - JFET (junction field-effect transistor)
- What is the difference between JFET and MOSFET?

Current-controlled amplifiers



(a)

Voltage-controlled amplifiers



(b)

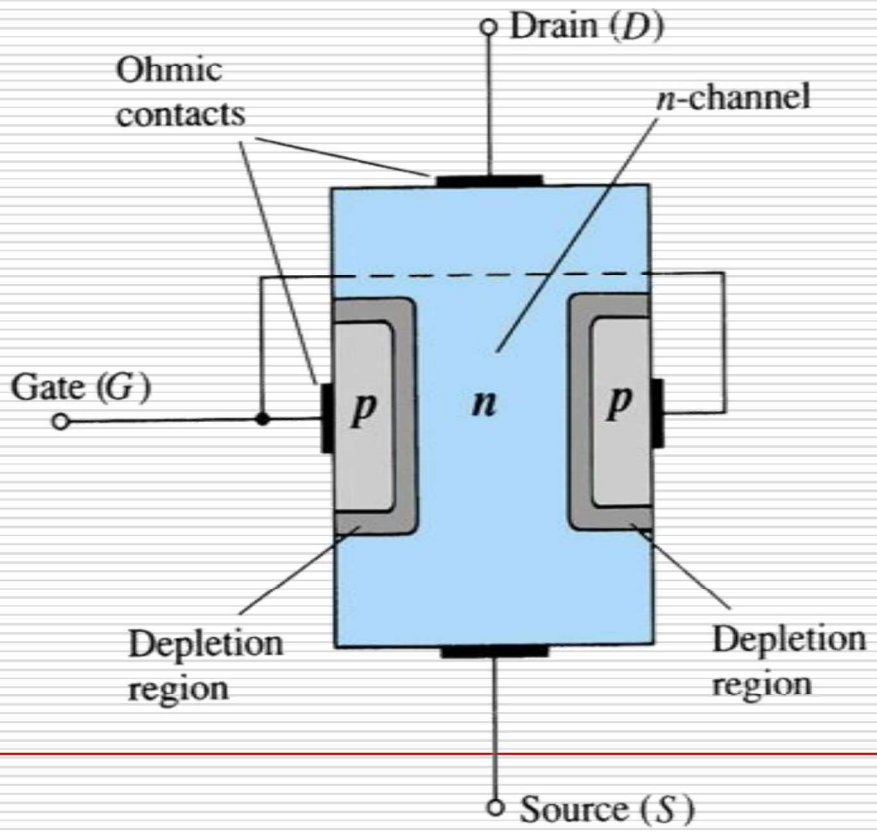
Introduction.. (Advantages of FET)

- High input impedance (MΩ) (Linear AC amplifier system)
- Temperature stable than BJT
- Smaller than BJT
- Can be fabricated with fewer processing
- BJT is bipolar – conduction both hole and electron
- FET is unipolar – uses only one type of current carrier
- ~~Less noise compare to BJT~~
- Usually use as logic switch

Disadvantages of FET

- Easy to damage compare to BJT
- ???

Junction field-effect transistor (JFET)



Junction field-effect transistor..

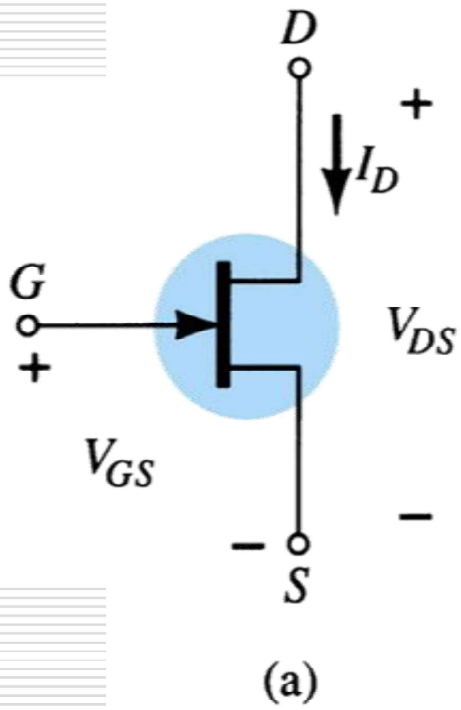
- There are 2 types of JFET
  - n-channel JFET
  - p-channel JFET

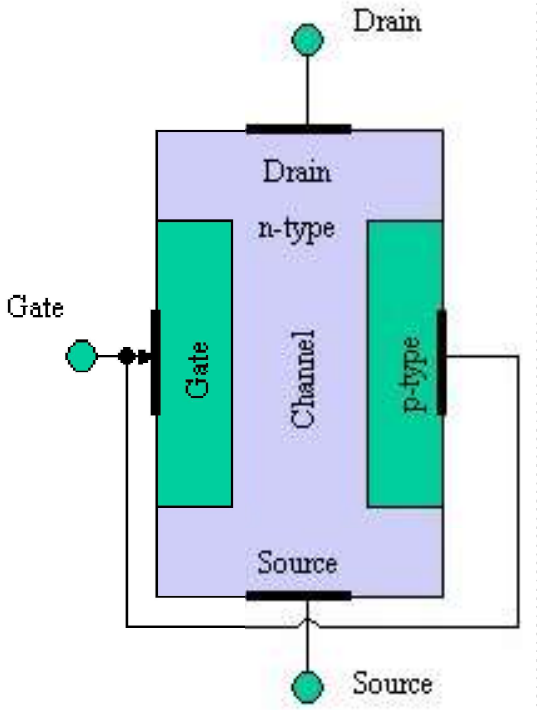
- Three Terminal
  - Drain – D (*Saliran*)
  - Gate -G (*Get*)
  - Source – S (*Punca*)

N-channel JFET

- N channel JFET:
  - Major structure is n-type material (channel) between embedded p-type material to form 2 p-n junction.
  - In the normal operation of an n-channel device, the Drain (D) is positive with respect to the Source (S). Current flows into the Drain (D), through the channel, and out of the Source (S)
  - Because the resistance of the channel depends on the gate-to-source voltage (V_{GS}), the drain current (I_D) is controlled by that voltage

N-channel JFET..

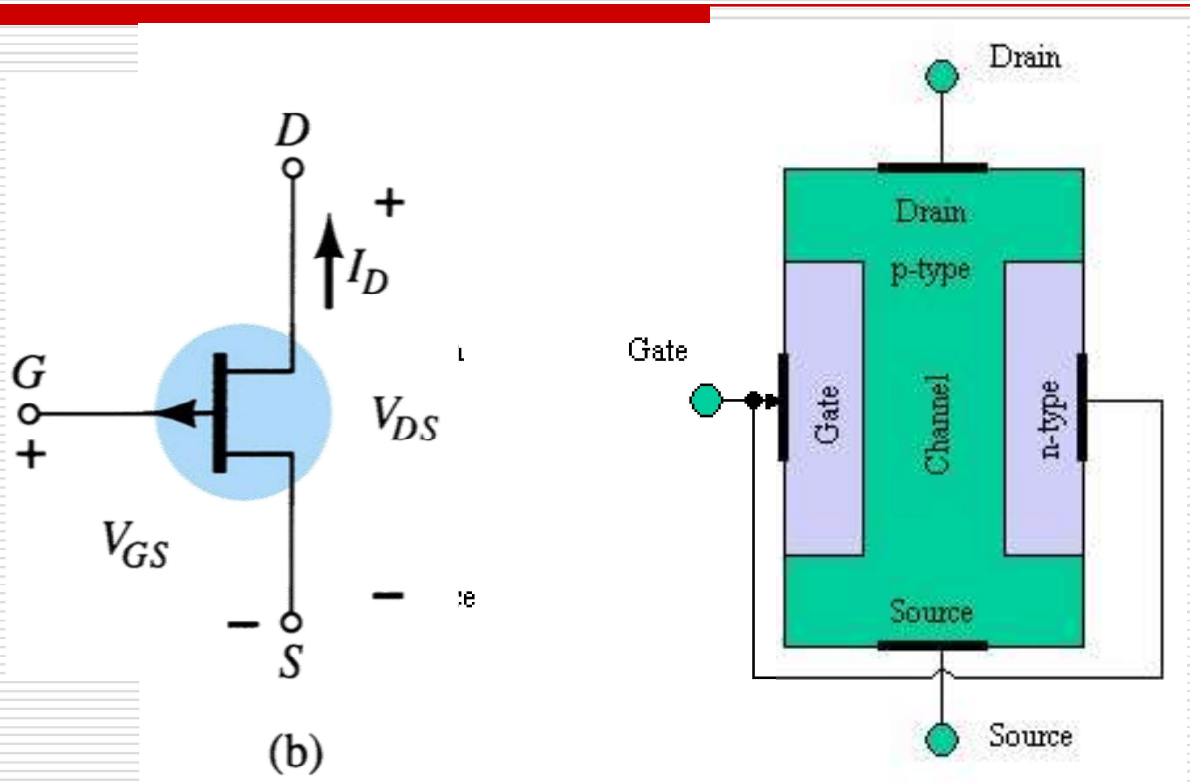




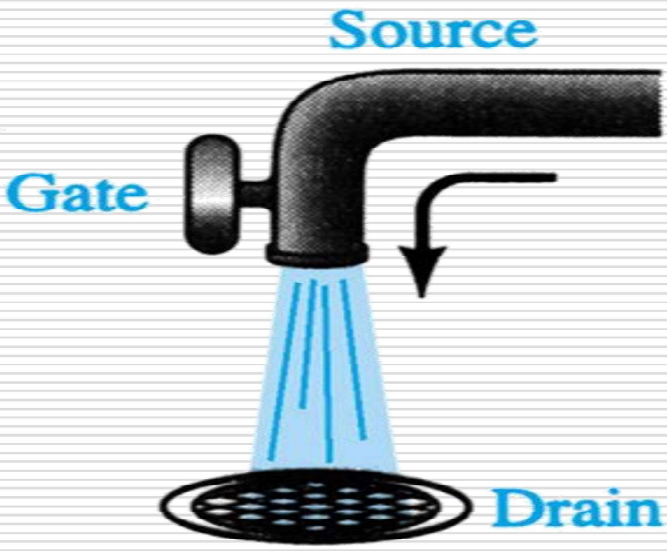
P-channel JFET

- P channel JFET:
  - Major structure is p-type material (channel) between embedded n-type material to form 2 p-n junction.
  - Current flow : from Source (S) to Drain (D)
  - Holes injected to Source (S) through p-type channel and flowed to Drain (D)

P-channel JFET..



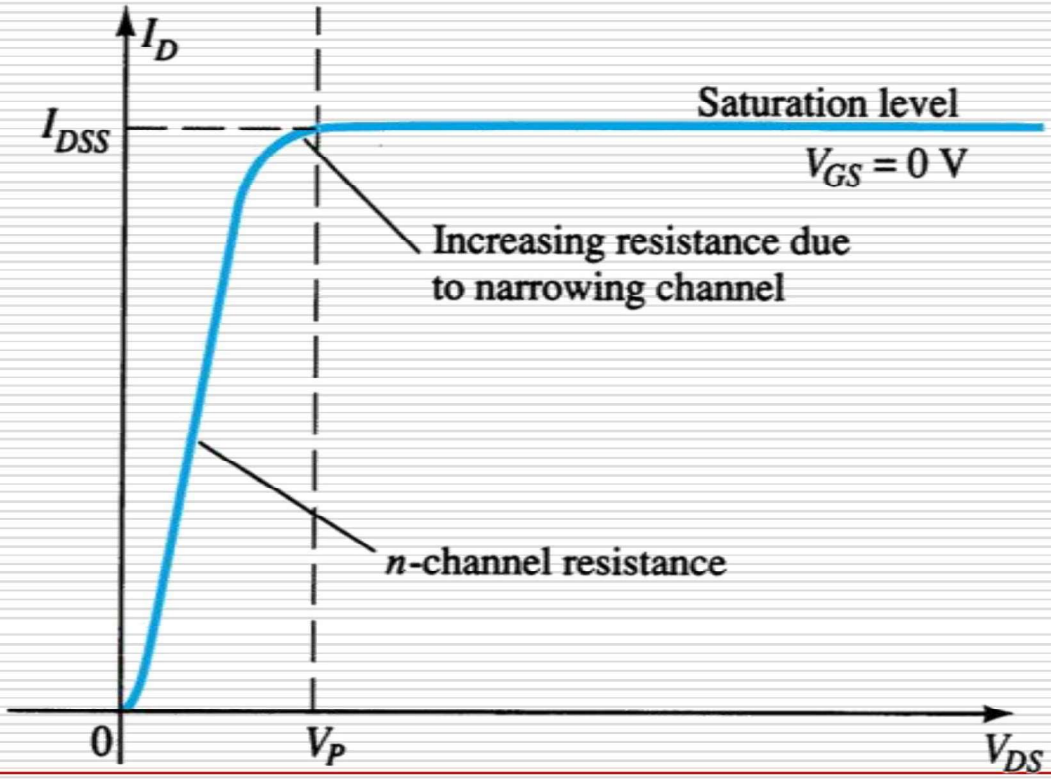
Water analogy for the JFET control mechanism



JFET Characteristic Curve

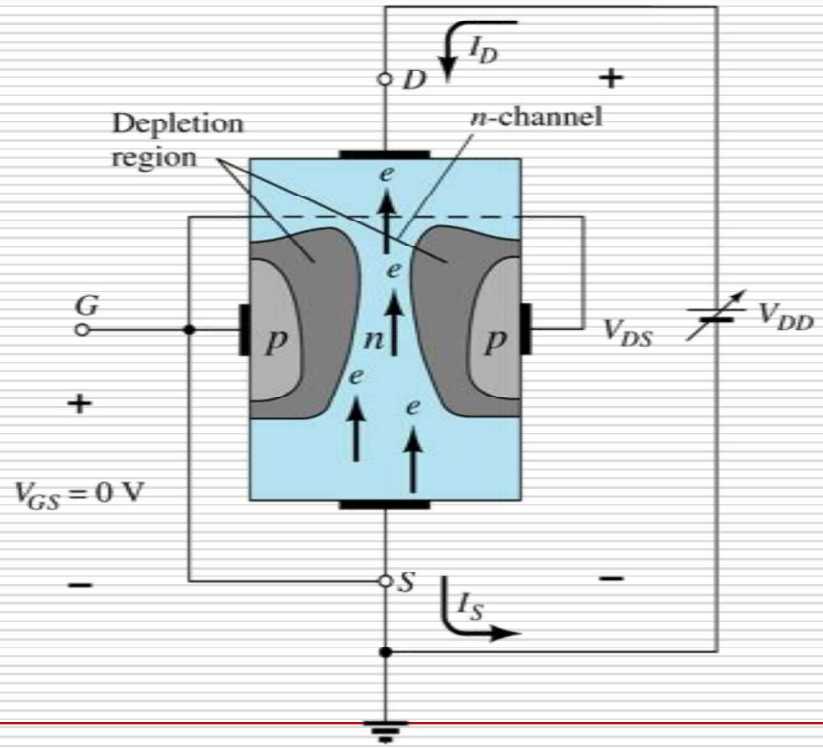
- To start, suppose $V_{GS}=0$
- Then, when V_{DS} is increased, I_D increases. Therefore, I_D is proportional to V_{DS} for small values of V_{DS}
- For larger value of V_{DS}, as V_{DS} increases, the depletion layer become wider, causing the resistance of channel increases.
- After the pinch-off voltage (V_p) is reached, the I_D becomes nearly constant (called as I_D maximum, I_{DSS}-Drain to Source current with Gate Shorted)

I_D versus V_{DS} for V_{GS} = 0 V.



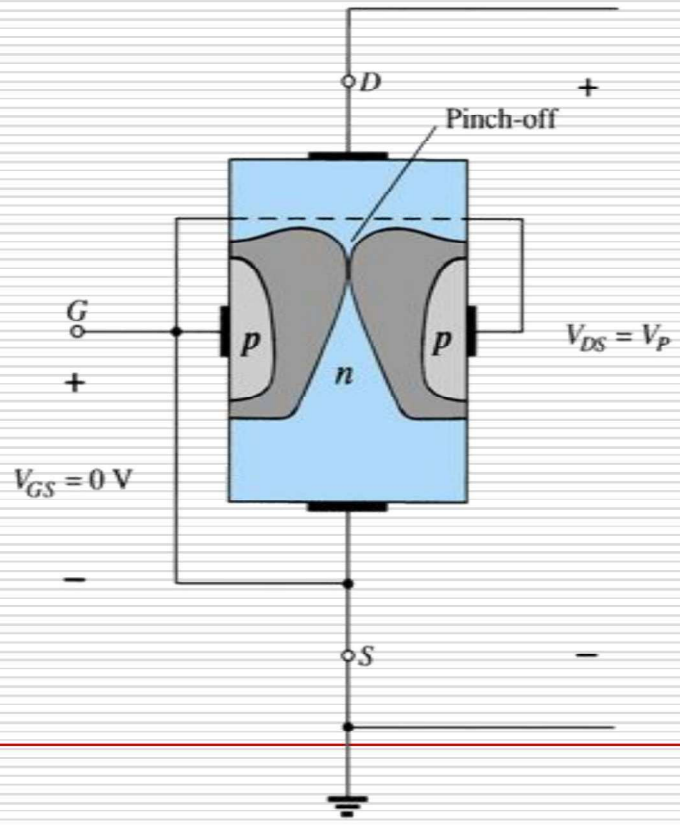
JFET Characteristic Curve

JFET for V_{GS} = 0 V and 0<V_{DS}<|V_p|

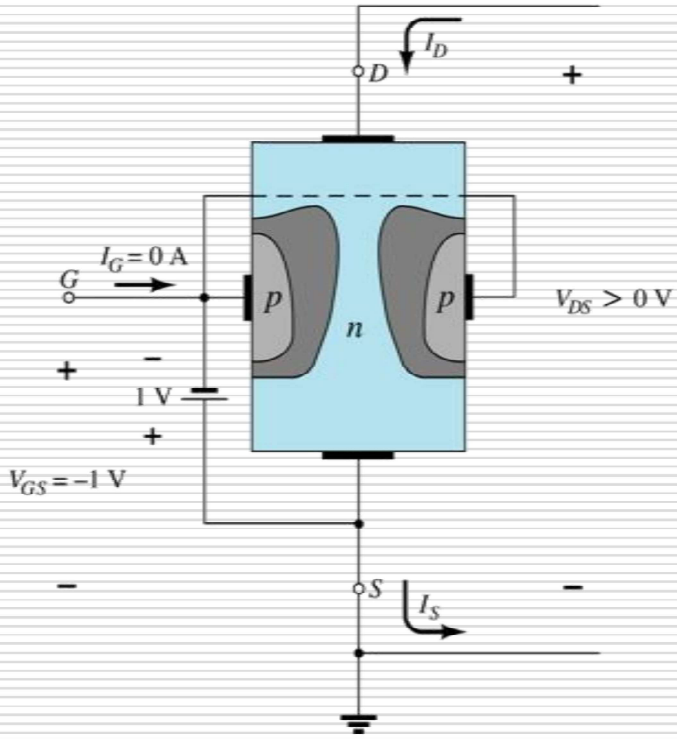


Channel becomes narrower as V_{DS} is increased

Pinch-off (V_{GS} = 0 V, $V_{DS} = V_P$).



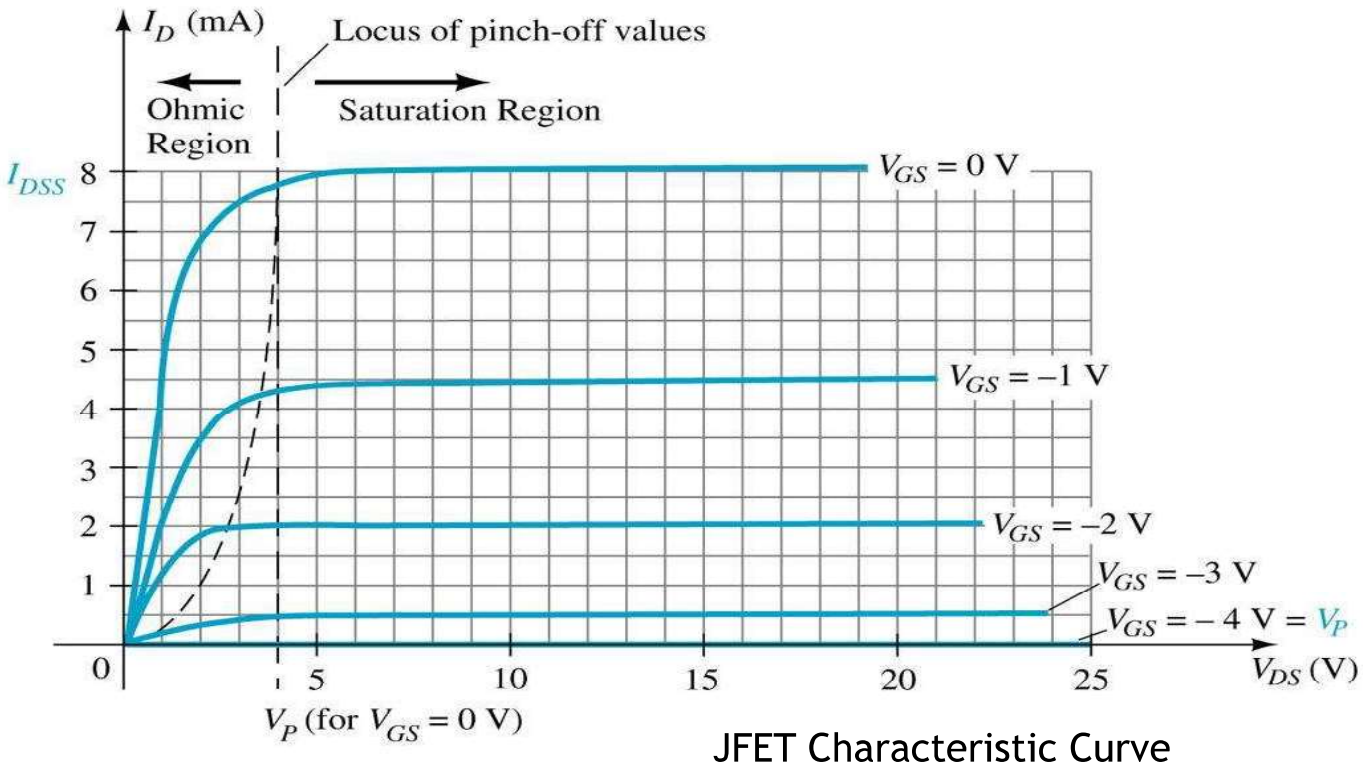
Application of a negative voltage to the gate of a JFET.



JFET Characteristic Curve..

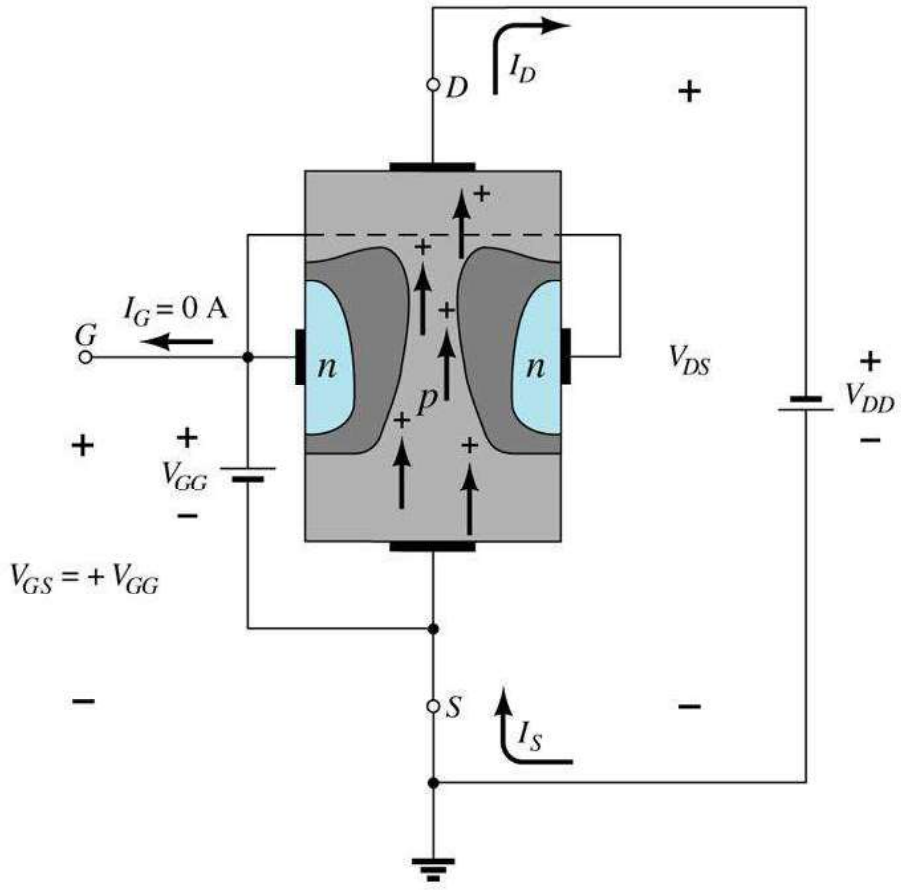
- For negative values of V_{GS}, the gate-to-channel junction is reverse biased even with $V_{DS}=0$
- Thus, the initial channel resistance is higher (in which the initial slope of the curves is smaller for values of V_{GS} closer to the pinch-off voltage (V_P)
- The resistance value is under the control of V_{GS}
- If V_{GS} is less than pinch-off voltage, the resistance becomes an open-circuit ;therefore the device is in cutoff ($V_{GS}=V_{GS(off)}$)
- The region where I_D constant – The saturation/pinch-off region
- The region where I_D depends on V_{DS} is called the linear/triode/ohmic region

n-Channel JFET characteristics curve with I_{DSS} = 8 mA and V_P = -4 V.

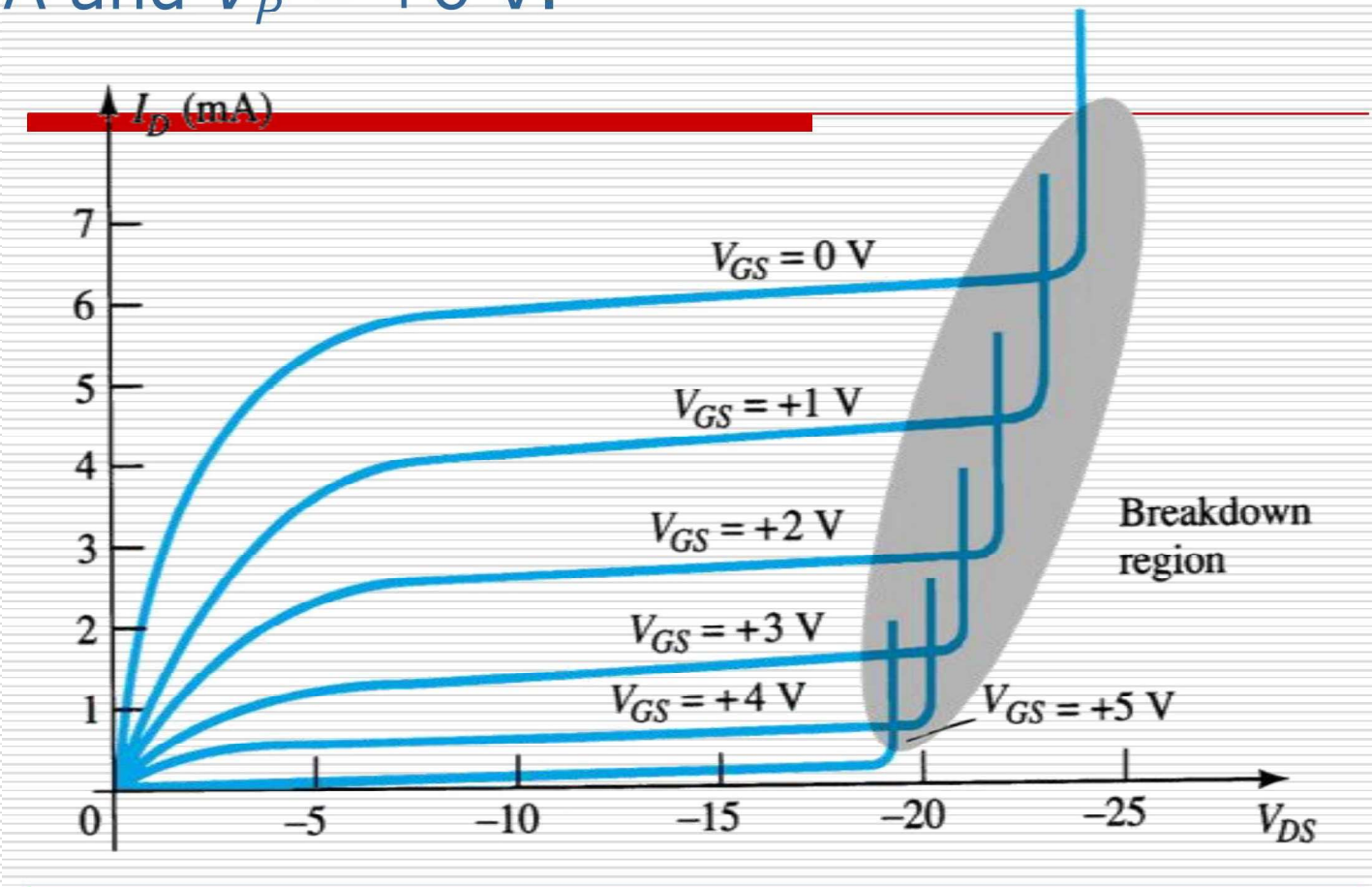


JFET Characteristic Curve

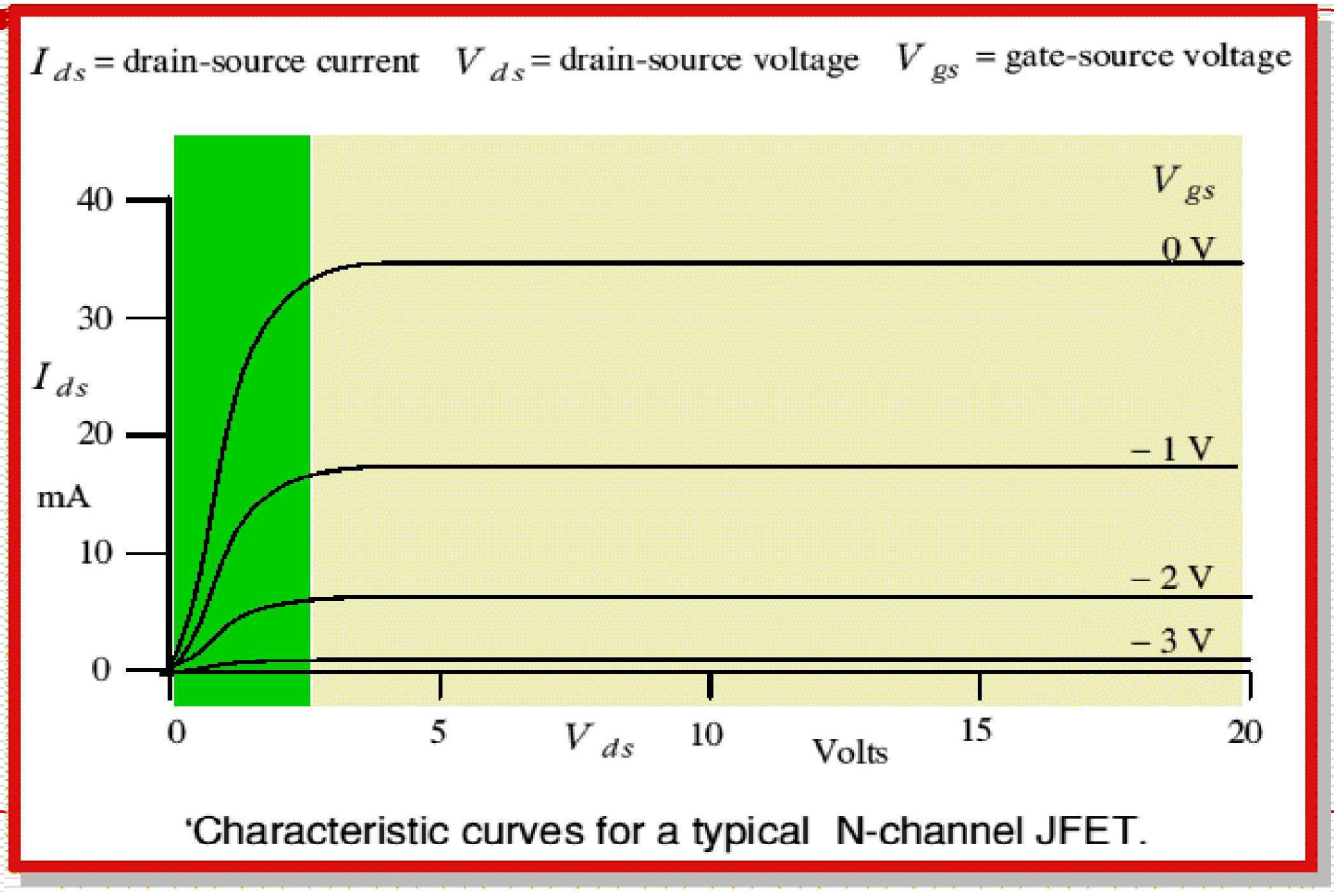
p-Channel JFET



p-Channel JFET characteristics with I_{DSS} = 6 mA and V_P = +6 V.

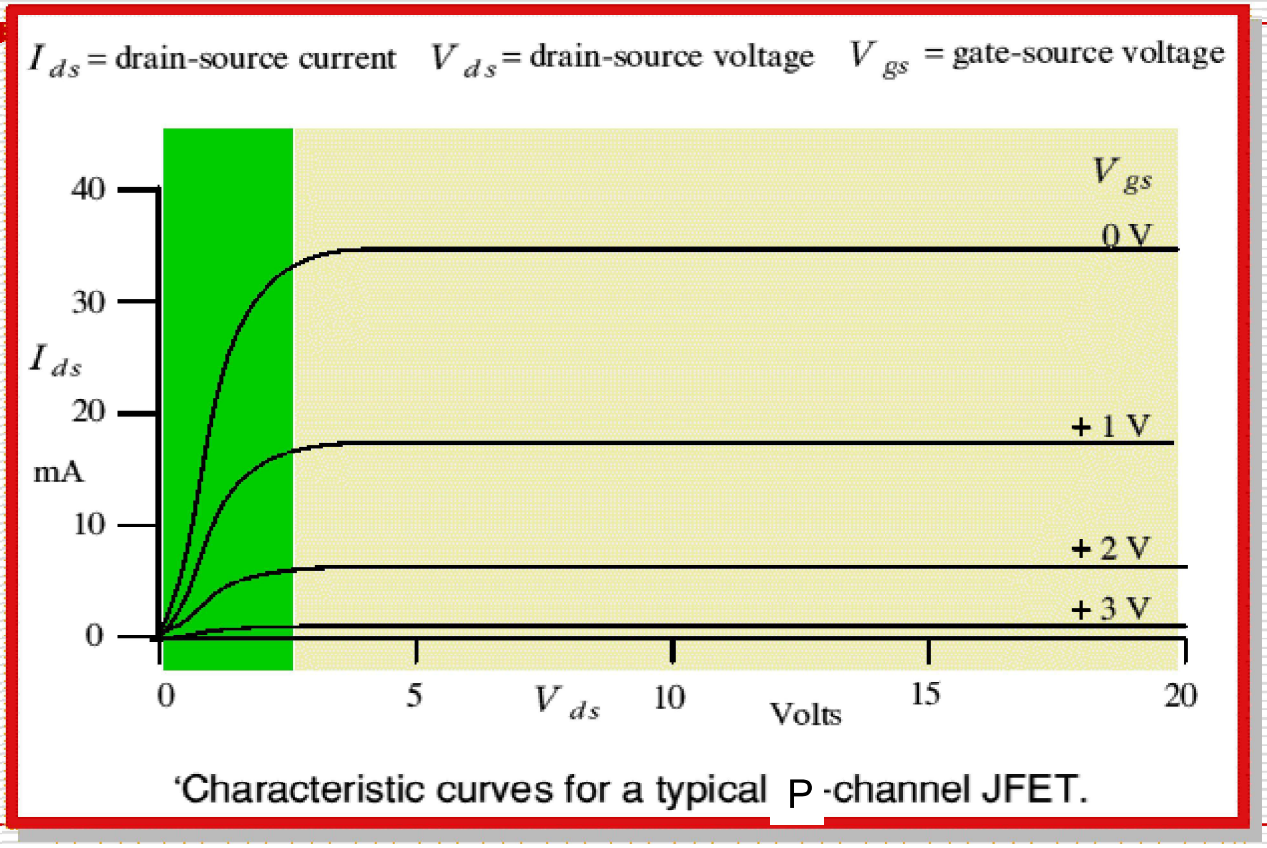


Characteristics for n-channel JFET



'Characteristic curves for a typical N-channel JFET.

Characteristics for p-channel JFET



'Characteristic curves for a typical P -channel JFET.

Operation of n-channel JFET

- JFET is biased with two voltage sources:
  - V_{DD}
  - V_{GG}
- ***V_{DD}*** generate voltage bias between Drain (D) and Source (S) – V_{DS}
- ***V_{DD}*** causes drain current, I_D flows from Drain (D) to Source (S)
- ***V_{GG}*** generate voltage bias between Gate (G) and Source (S) with negative polarity source is connected to the Gate Junction (G) – reverse-biases the gate; therefore gate current, $I_G = 0$.
- ***V_{GG}*** is to produce depletion region in N channel so that it can control the amount of drain current, I_D that flows through the channel

Transfer Characteristics

The input-output transfer characteristic of the JFET is not as straight forward as it is for the BJT. In BJT:

$$I_C = \beta I_B$$

which β is defined as the relationship between I_B (input current) and I_C (output current).

Transfer Characteristics..

In JFET, the relationship between V_{GS} (input voltage) and I_D (output current) is used to define the transfer characteristics. It is called as Shockley's Equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad V_P = V_{GS\ (OFF)}$$

The relationship is more complicated (and not linear)

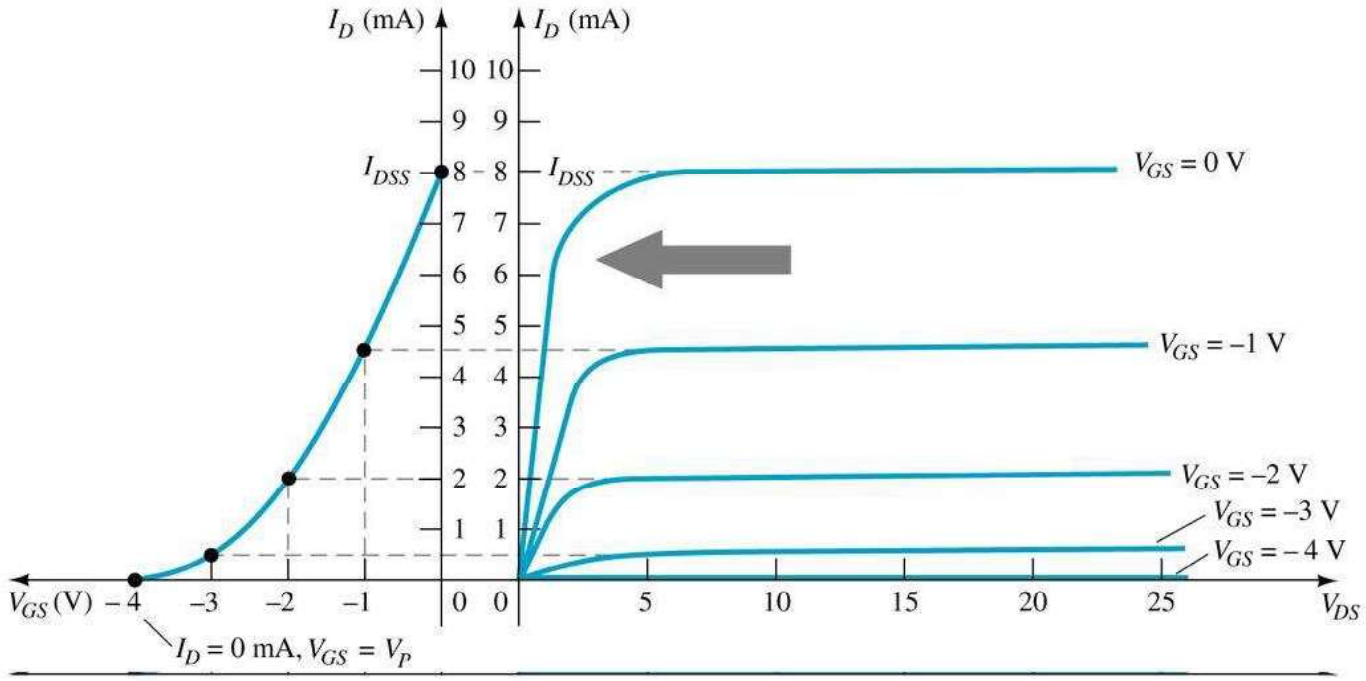
As a result, FET's are often referred to a square law devices

Transfer Characteristics…

- Defined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad V_P = V_{GS(off)}$$

- Relationship between I_D and V_{GS}.
- Obtaining transfer characteristic curve axis point from Shockley:
  - When V_{GS} = 0 V, $I_D = I_{DSS}$
  - When $V_{GS} = V_{GS(off)}$ or V_p, I_D = 0 mA



JFET Transfer Characteristic Curve JFET Characteristic Curve

Exercise 1

Sketch the transfer defined by

I_{DSS} = 12 mA dan $V_{GS(off)}$ = - 6

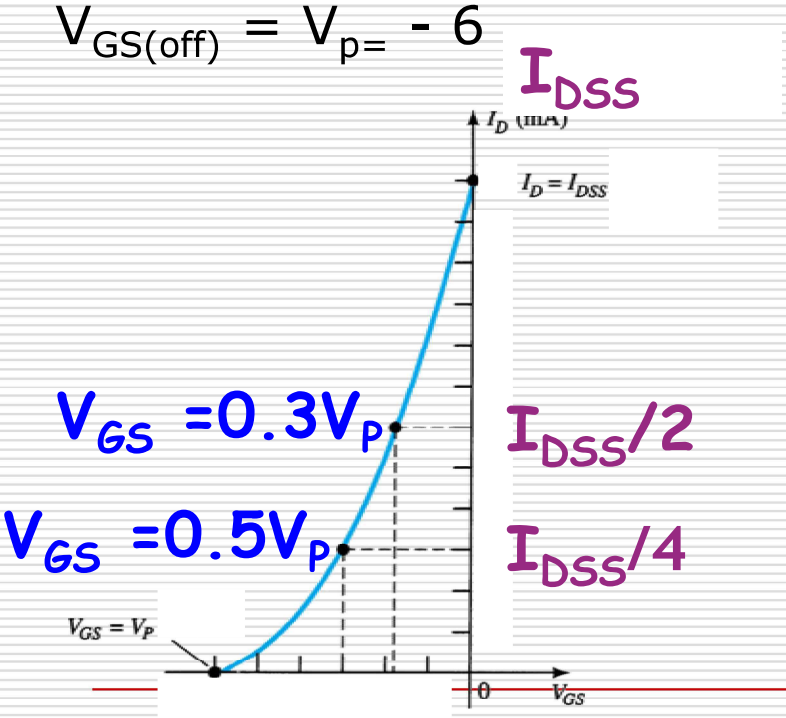
V_{GS}	I_D
0	I_{DSS}
0.3Vp	$I_{DSS}/2$
0.5Vp	$I_{DSS}/4$
Vp	0 mA

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Exercise 1

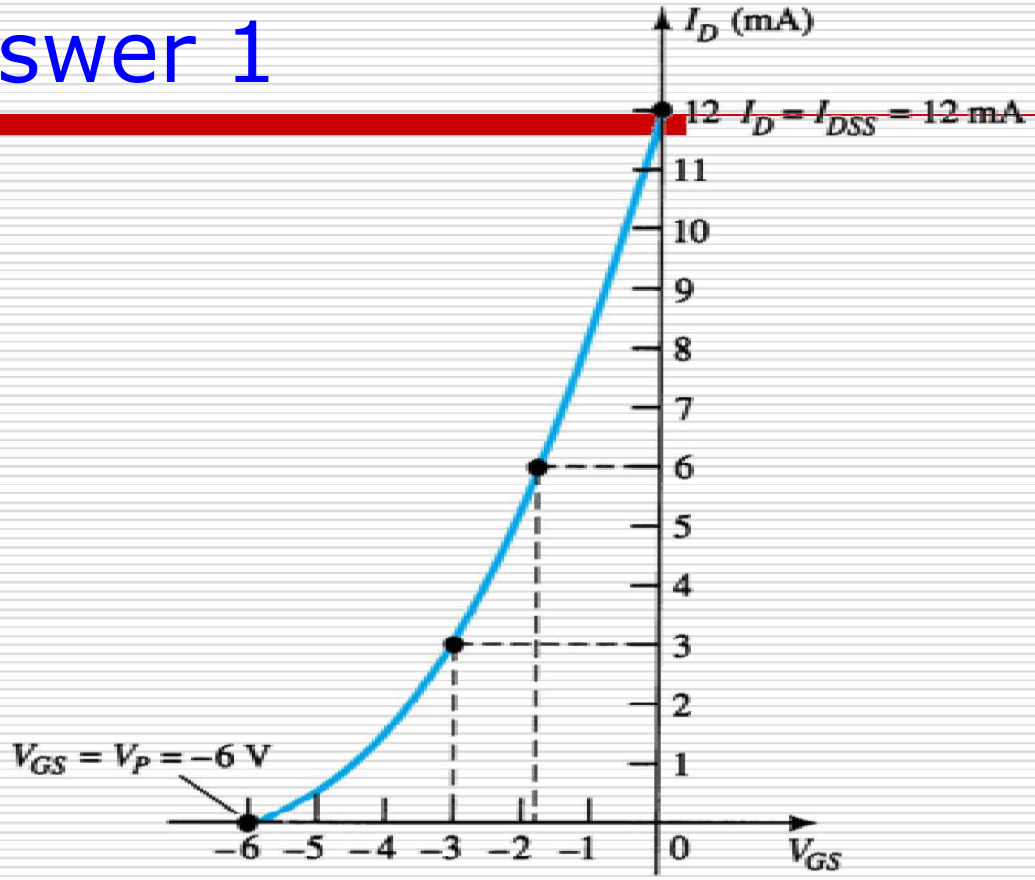
Sketch the transfer defined by I_{DSS} = 12 mA dan $V_{GS(off)} = V_{p=} - 6$



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

Answer 1



Exercise 2

Sketch the transfer defined by

I_{DSS} = 4 mA dan $V_{GS(off)}$ = 3 V

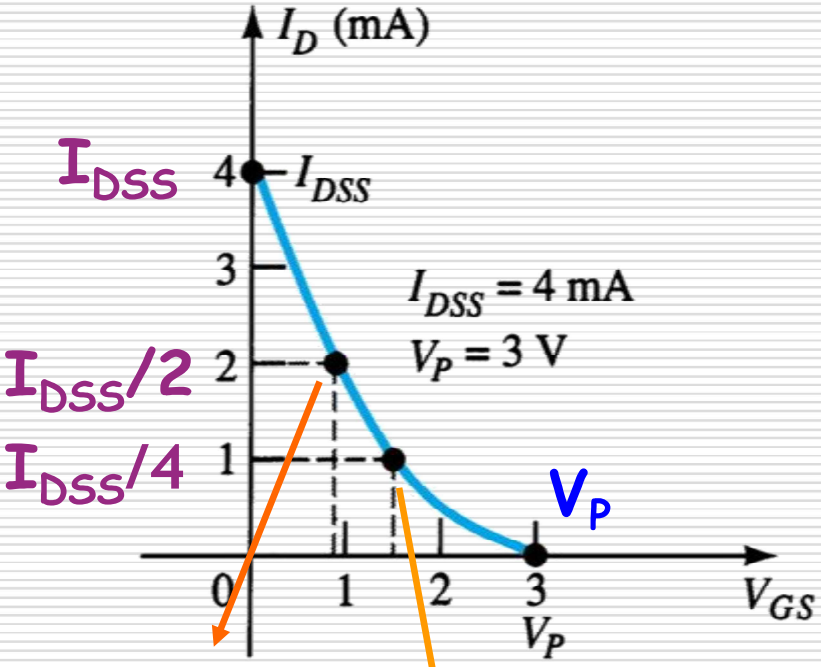
V_{GS}	I_D
0	I_{DSS}
0.3Vp	$I_{DSS}/2$
0.5Vp	$I_{DSS}/4$
Vp	0 mA

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Exercise 2

Sketch the transfer defined by
I_{DSS} = 4 mA dan $V_{GS(off)}$ = 3V



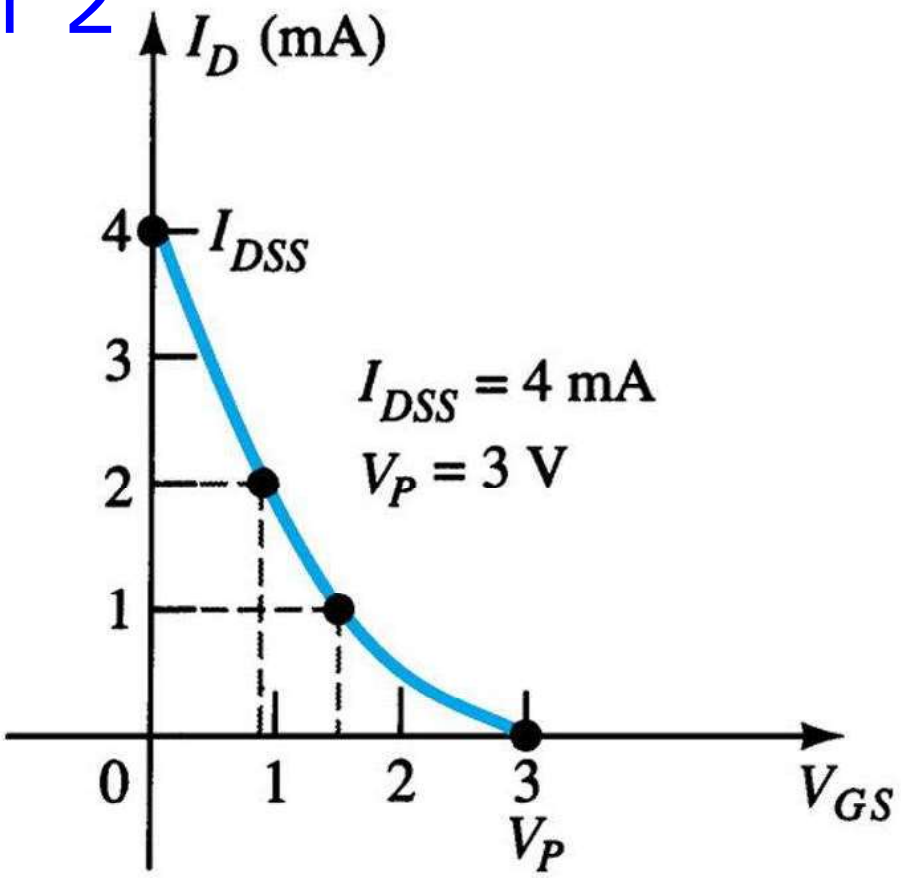
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

V_{GS} =0.3V_P

V_{GS} =0.5V_P

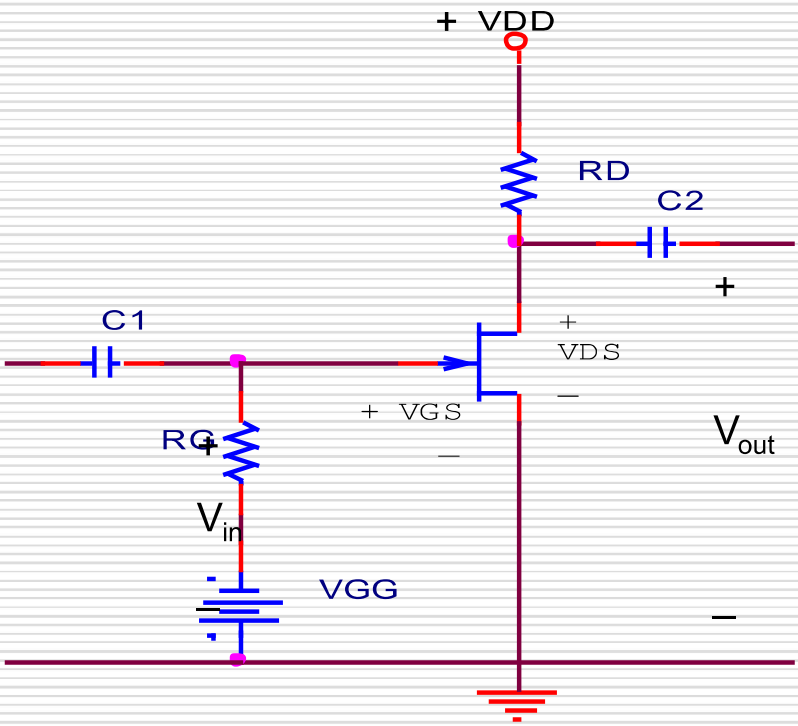
Answer 2



DC JFET Biasing

- Just as we learned that the BJT must be biased for proper operation, the JFET also must be biased for operation point (I_D, V_{GS}, V_{DS})
- In most cases the ideal Q-point will be at the middle of the transfer characteristic curve, which is about half of the I_{DSS}.
- 3 types of DC JFET biasing configurations :
  - Fixed-bias
  - Self-bias
  - Voltage-Divider Bias

Fixed-bias

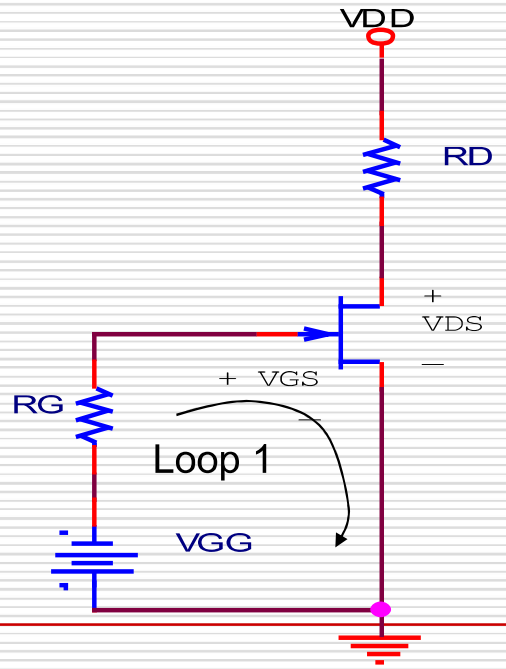


Fixed-bias

- Use two voltage sources: V_{GG}, V_{DD}
- V_{GG} is reverse-biased at the Gate – Source (G-S) terminal, thus no current flows through R_G (I_G = 0).

Fixed-bias..

- DC analysis
  - All capacitors replaced with open-circuit



Fixed-bias…

1. Input Loop

- By using KVL at loop 1:

$$V_{GG} + V_{GS} = 0$$
$$V_{GS} = - V_{GG}$$

  - For graphical solution, use $\mathbf{V_{GS} = - V_{GG}}$ to draw the load line
  - For mathematical solution, replace $\mathbf{V_{GS} = -V_{GG}}$ in Shockley's Eq. ,therefore:

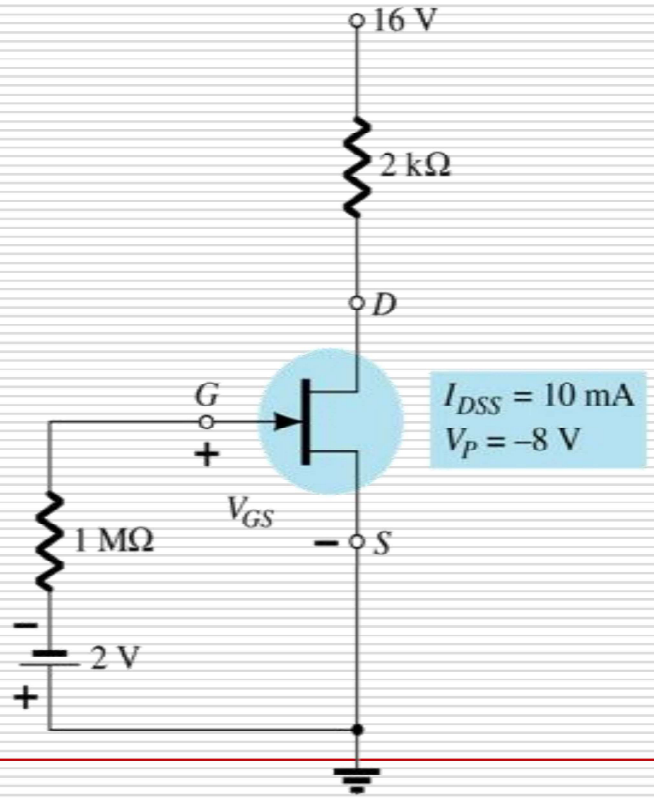
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = I_{DSS}\left(1 + \frac{V_{GG}}{V_{GS(off)}}\right)^2$$

2. Output loop

$$- V_{DD} + I_D R_D + V_{DS} = 0$$
$$V_{DS} = V_{DD} - I_D R_D$$

3. Then, plot transfer characteristic curve by using Shockley's Equation

Example : Fixed-bias



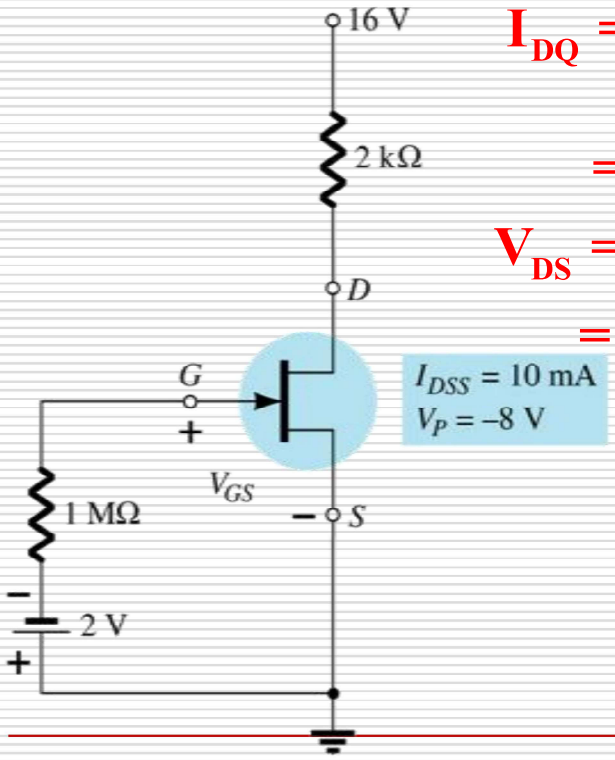
Determine the following network:

1. V_{GSQ}
2. I_{DQ}
3. V_D
4. V_G
5. V_S

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Mathematical Solutions

$$V_{GSQ} = -V_{GG} = -2$$



$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{mA}\left(1 - \frac{-2}{-8}\right)^2$$

$$= 10\text{mA}(0.75)^2 = 5.625\text{mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 16 - (5.625\text{mA})(2\text{k}\Omega)$$

$$= 16\text{V} - 11.25\text{V} = 4.75\text{V}$$

$$V_D = V_{DS} = 4.75\text{V}$$

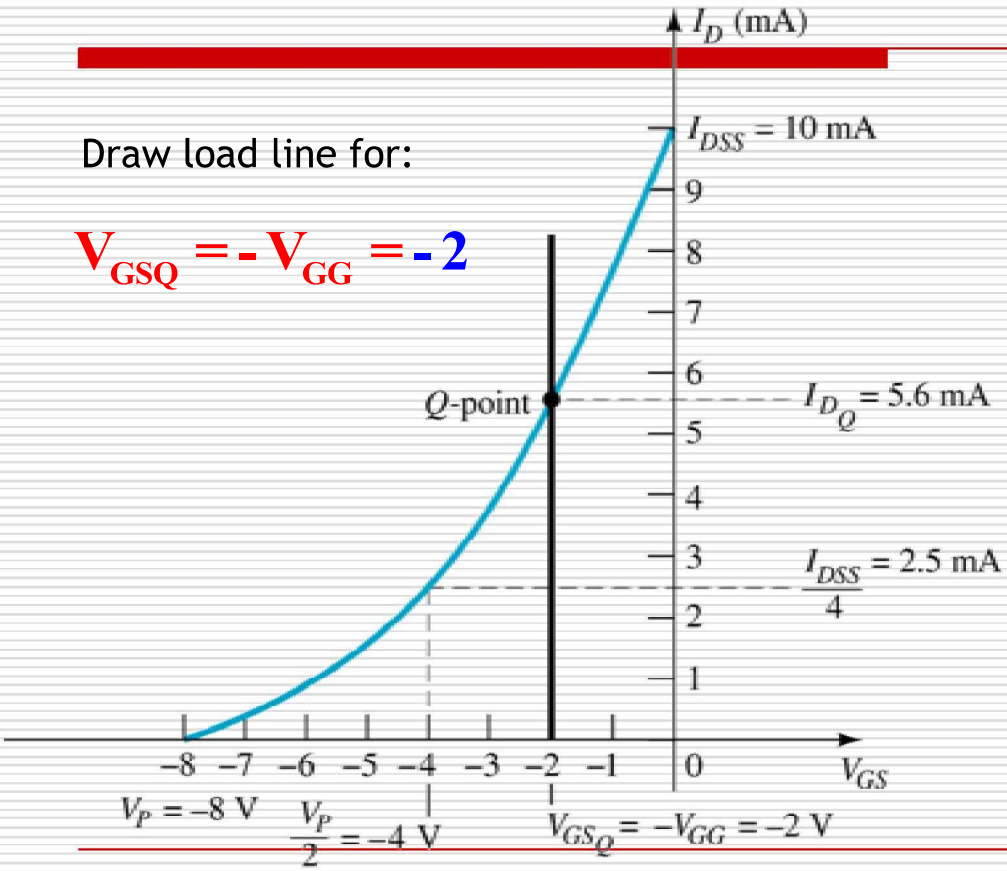
$$V_G = V_{GS} = -2\text{V}$$

$$V_S = 0\text{V}$$

Graphical solution for the network

Draw load line for:

$V_{GSQ} = -V_{GG} = -2$



$I_{DQ} = 5.6$ mA

$V_{DS} = 4.75V$

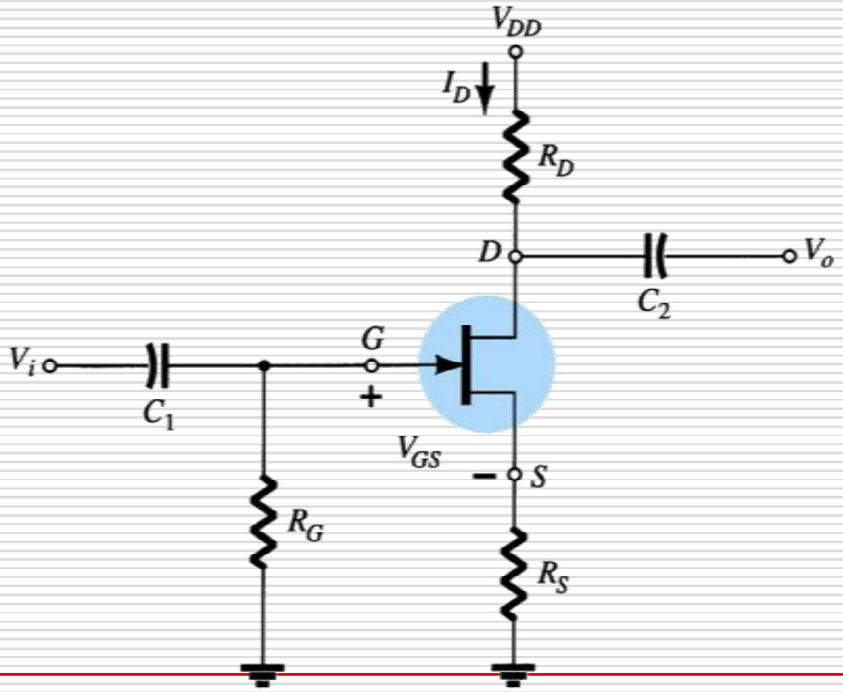
$V_D = 4.75V$

$V_G = -2V$

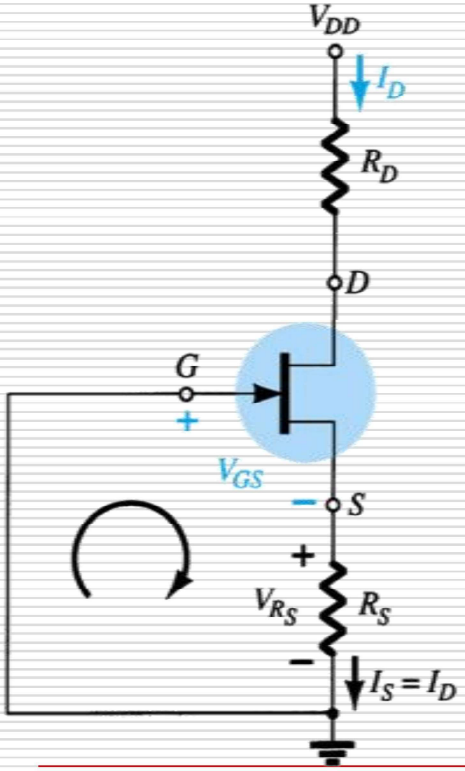
$V_S = 0V$

Self-bias

- Using only one voltage source



DC analysis of the self-bias configuration.



Since $I_G \approx 0A$, $V_{RG} = I_G R_G$

thus $V_{RG} = 0A$,

$$V_{RS} = I_D R_S$$

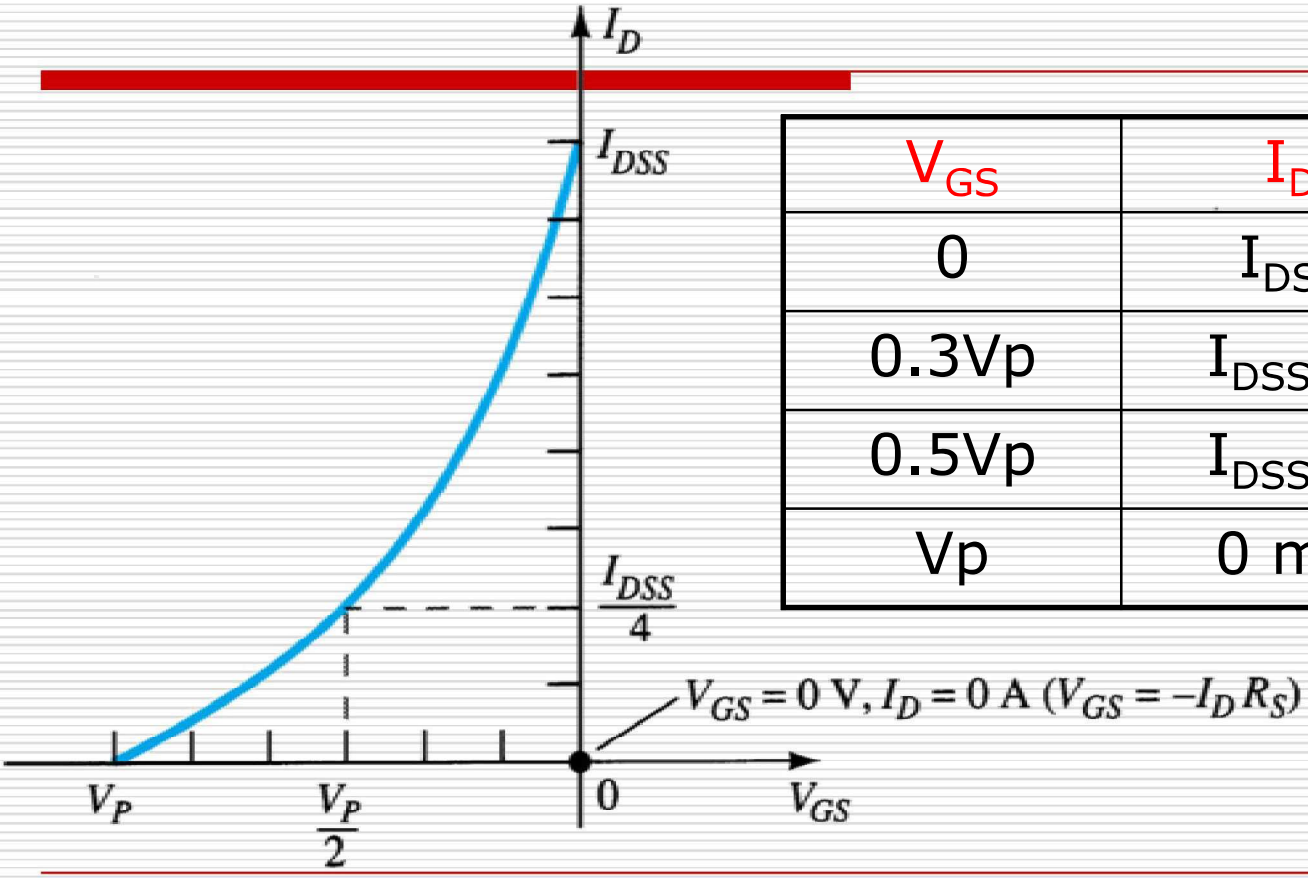
$$V_{GS} + V_{RS} = 0$$

$$V_{GS} = -V_{RS}$$

$$= -I_D R_S$$

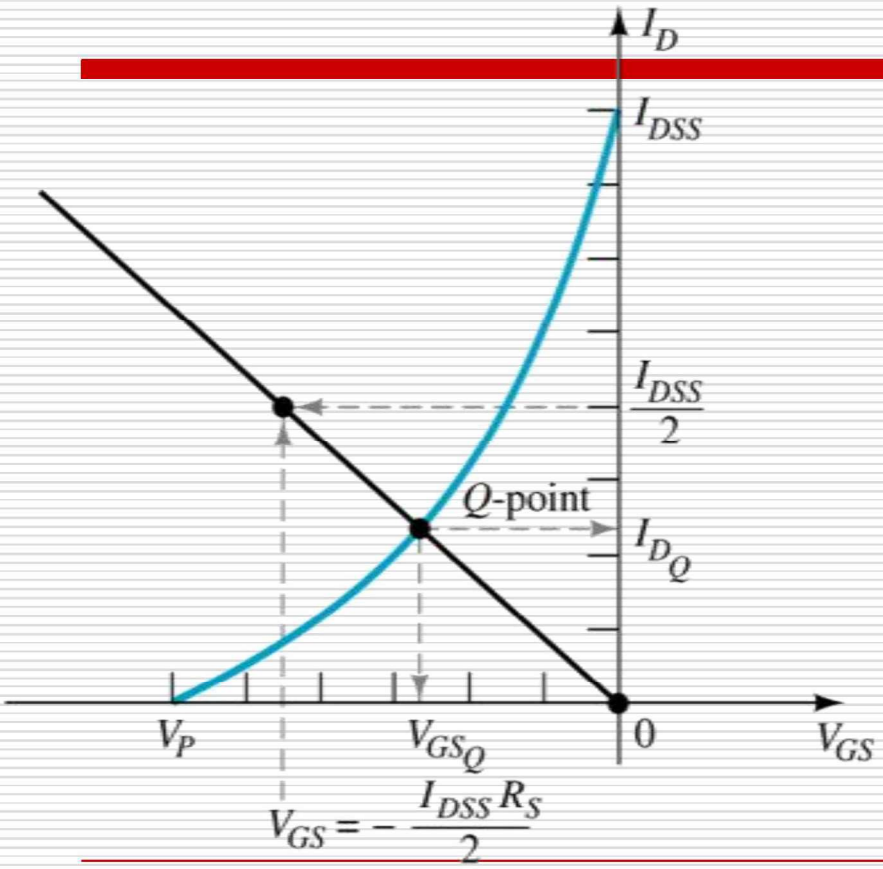
Q point for V_{GS}

Graphical Solutions:
Defining a point on the self-bias line.



V_{GS}	I_D
0	I_{DSS}
0.3Vp	$I_{DSS}/2$
0.5Vp	$I_{DSS}/4$
Vp	0 mA

Graphical Solutions:
Sketching the self-bias line.



$$I_D = I_{DSS}/2$$

$$V_{GS} = -I_D R_S$$

$$= -\frac{I_{DSS} R_S}{2}$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

$$V_S = I_D R_S$$

Mathematical Solutions:

- Replace $V_{GS} = -I_D R_S$ in the Shockley's Equation:

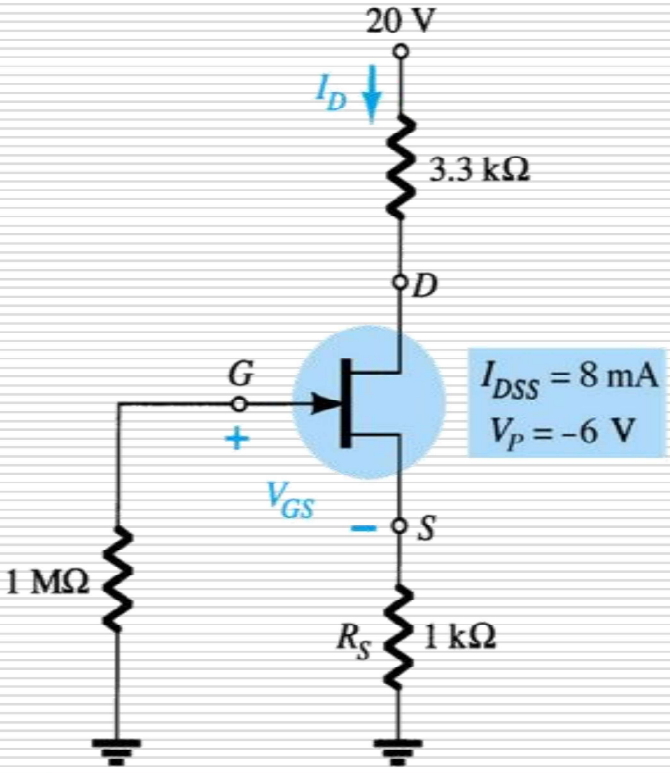
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad V_P = V_{GS(off)}$$

$$therefore;$$

$$I_D = I_{DSS}\left(1 - \frac{(-I_D R_S)}{V_P}\right)^2$$

- By using, quadratic equation and formula, choose value of I_D that relevant within the range (0 to I_{DSS}): nearly to $I_{DSS}/2$
- Find V_{GS} by using $V_{GS} = -I_D R_S$;also choose V_{GS} that within the range (0 to v_P)

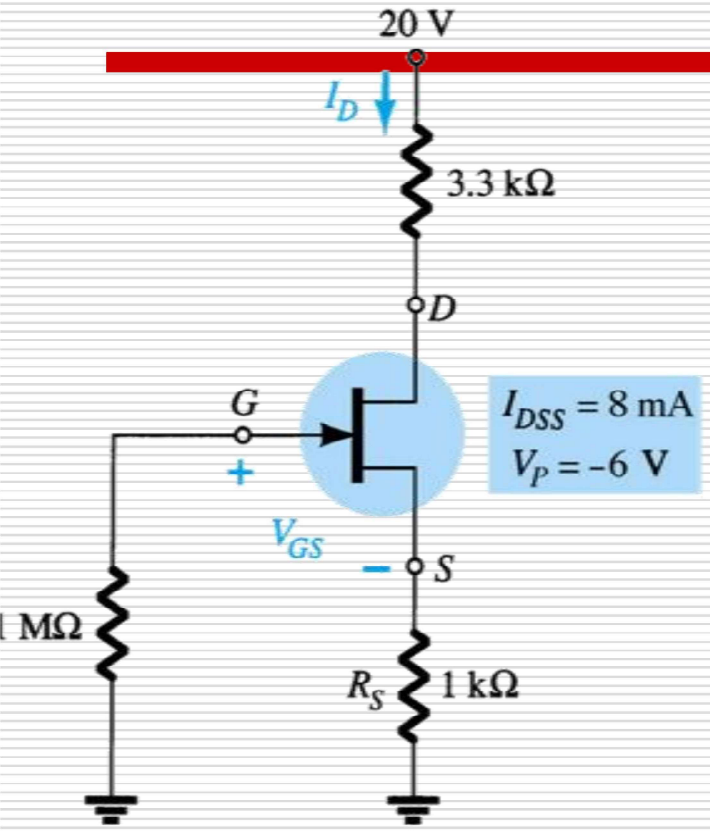
Example : Self-bias configuration



Determine the following for the network

1. V_{GSQ}
2. I_{DQ}
3. V_D
4. V_G
5. Vs

Graphical Solutions:



$$V_{GS} = -I_D R_s$$

When $I_D = 4mA$,

$$V_{GS} = -I_D R_s$$

$$= -(4mA)(1k\Omega) = -4V$$

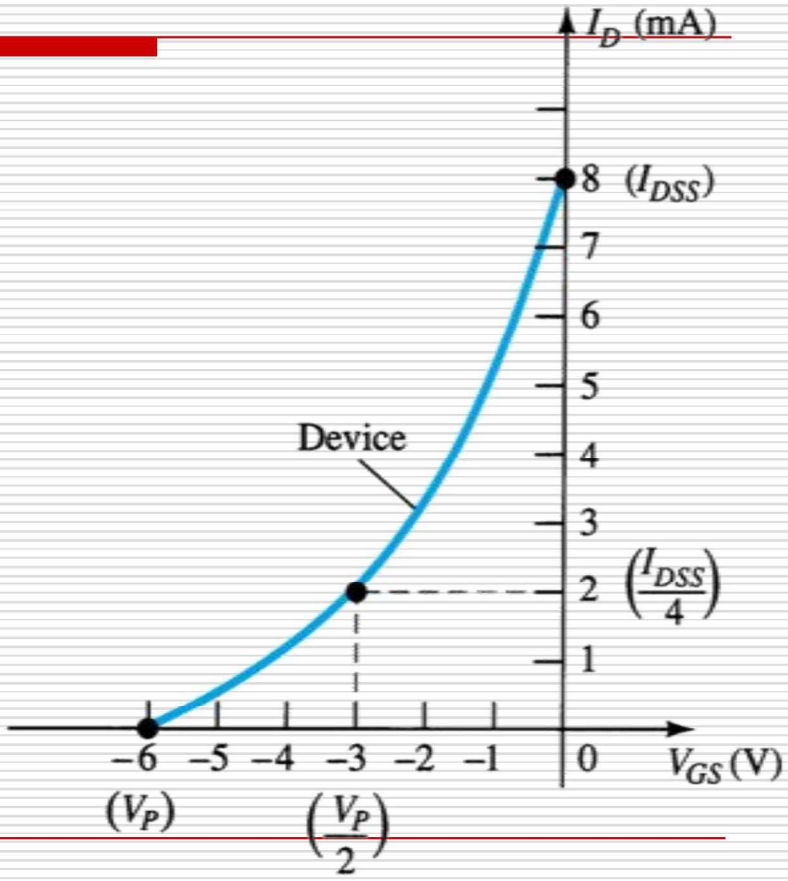
When $I_D = 8mA$, $V_{GS} = -I_D R_s$

$$V_{GS} = -I_D R_s$$

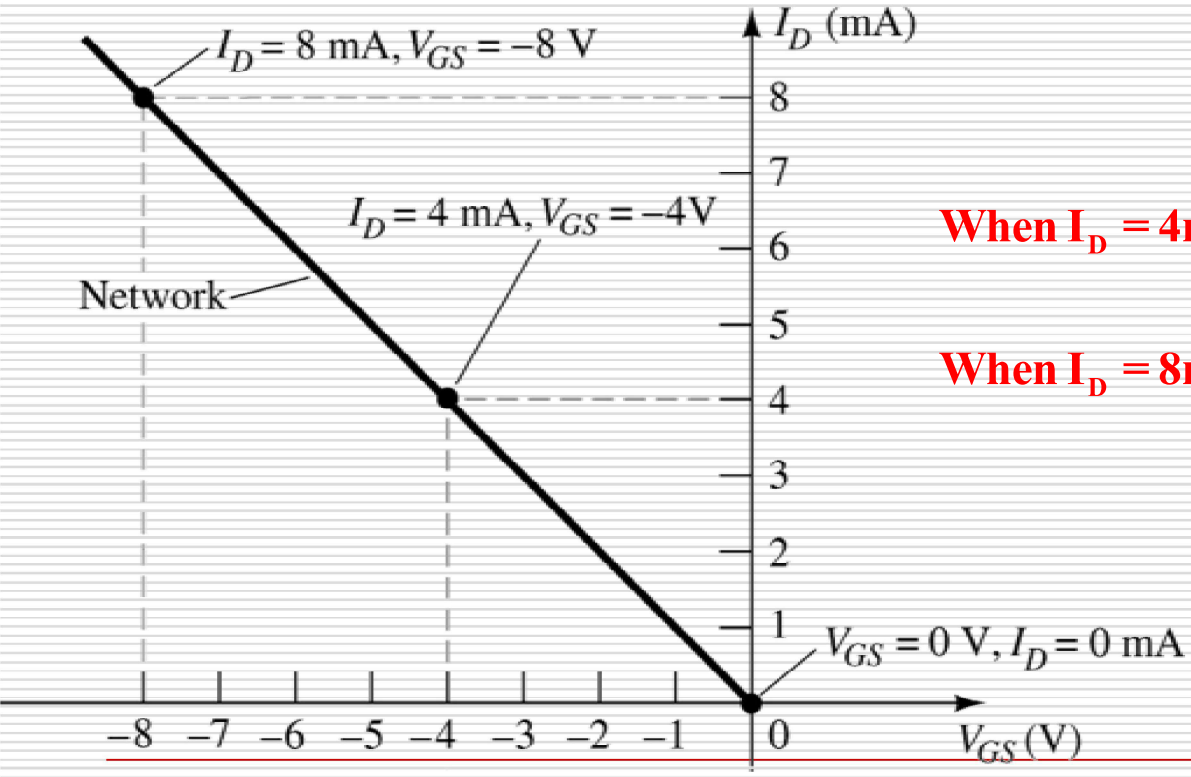
$$= -8 \quad mA \quad (1k\Omega) = -8V$$

Sketching the transfer characteristics curve

Vgs	I_D
0	I_{DSS}
0.3Vp	$I_{DSS}/2$
0.5Vp	$I_{DSS}/4$
Vp	0 mA



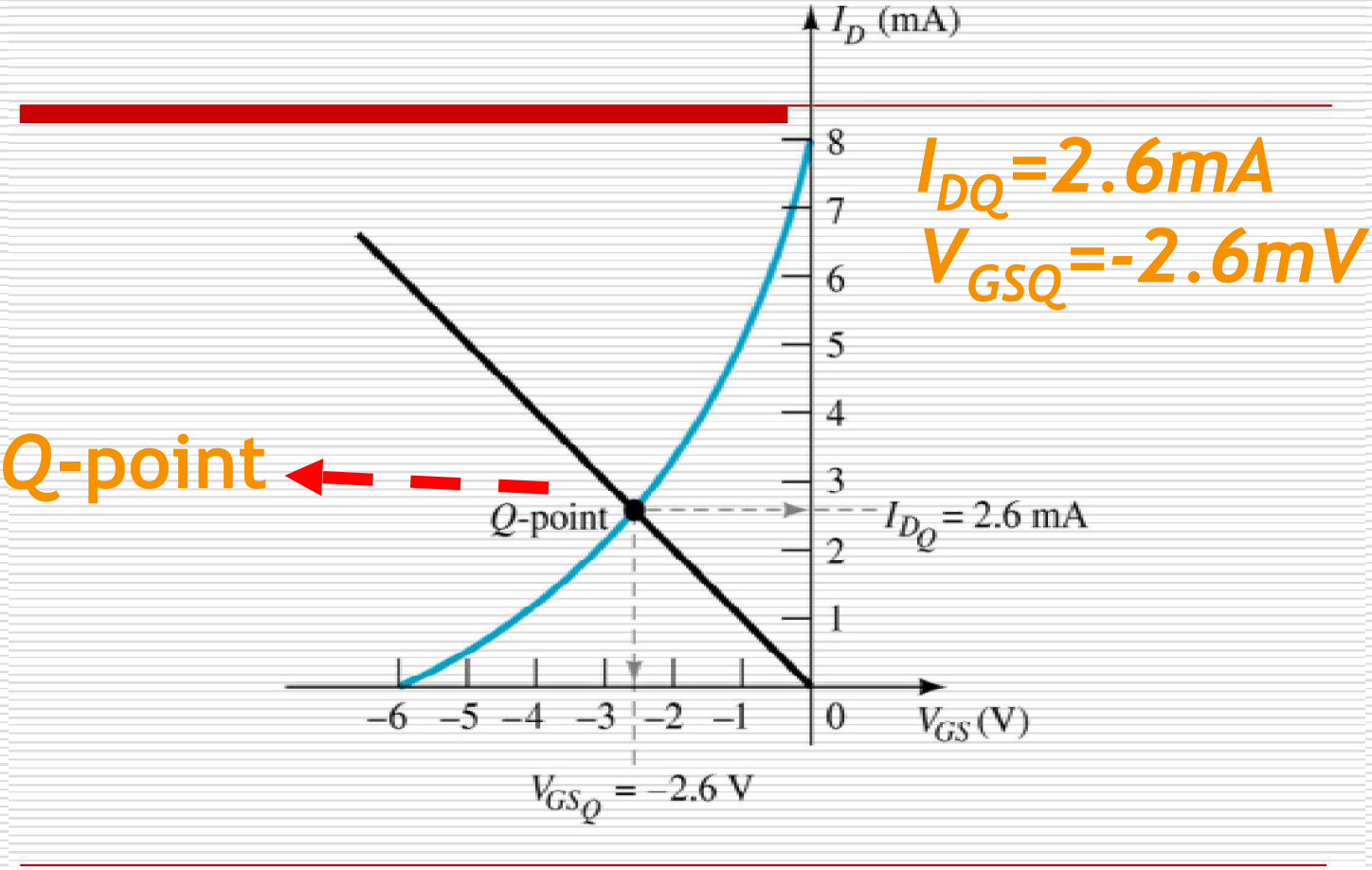
Sketching the self-bias line



When $I_D = 4$mA, $V_{GS} = -4$V

When $I_D = 8$mA, $V_{GS} = -8$V

Graphical Solutions: Determining the *Q*-point



Mathematical Solutions

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \qquad recall \quad V_{GS} = -I_D R_S$$

$$= I_{DSS}\left(1-\frac{(-I_D R_S)}{V_P}\right)^2$$

$$I_D = 8m\left(1+\frac{I_D(1k)}{-6}\right)^2 = 8m\left(\frac{-6+I_D(1k)}{-6}\right)^2$$

$$= \frac{8m}{36}\left(36-6kI_D-6kI_D+1MI_D{}^2\right)$$

$$36I_D = 0.288-96I_D+8kI_D{}^2$$

$$8kI_D{}^2-132I_D+0.288=0$$

$$I_{D_1} = 13.9mA \qquad I_{D_{21}} = 2.588mA$$

$$V_{GS} = -I_D R_S \qquad V_{GS} = -I_D R_S$$

$$= -13.9mA(1k) \qquad = -2.588mA(1k)$$

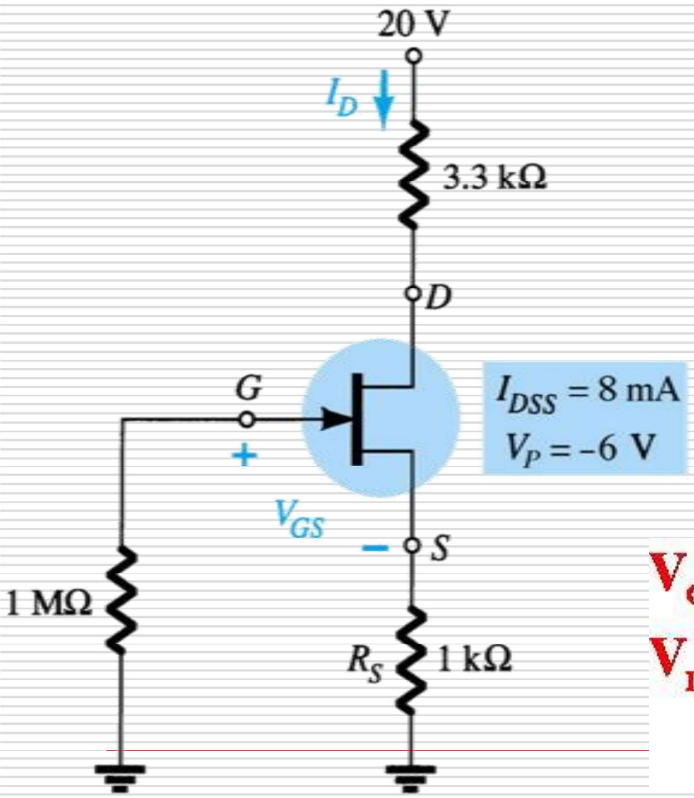
$$= -13.9V \qquad = -2.6V$$

$$therefore;\ choose\ I_D = 2.588mA\ \ and\ \ V_{GS} = -2.6V$$

Solutions

$V_{GSQ} = -2.6V$

$I_{DQ} = 2.6mA$



$I_D = I_S$

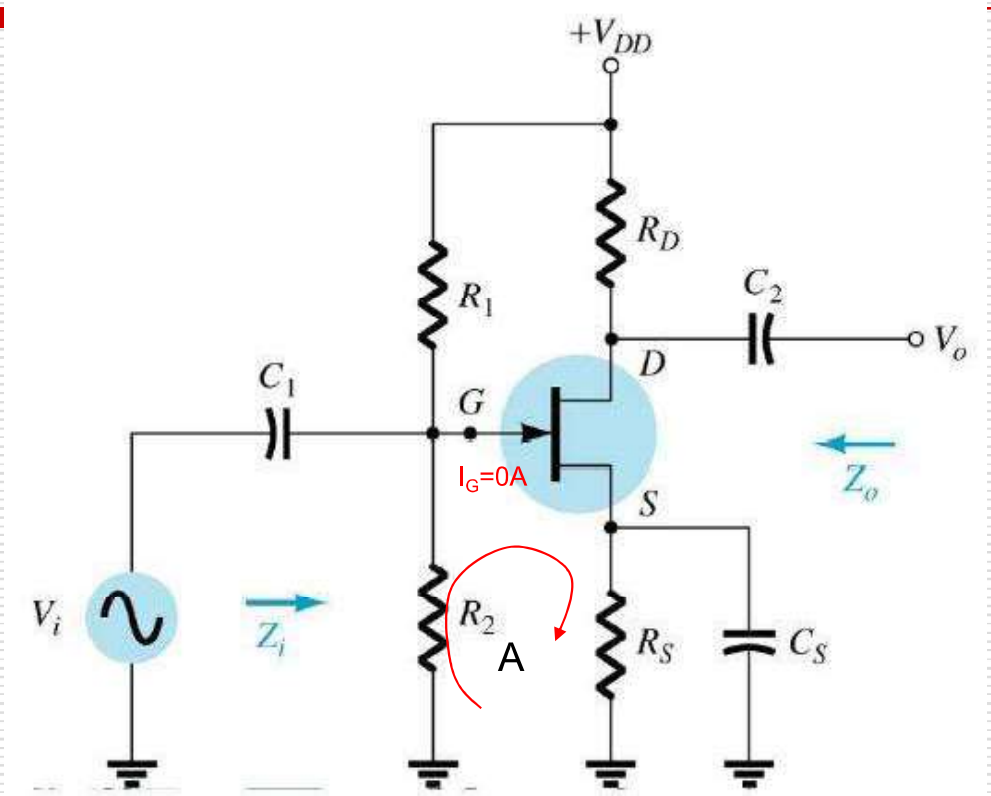
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 20V - 2.6mA(4.3k\Omega)$$
$$= 8.82V$$

$$V_s = I_s R_s = (2.6mA)(1k\Omega)$$
$$= 2.6V$$

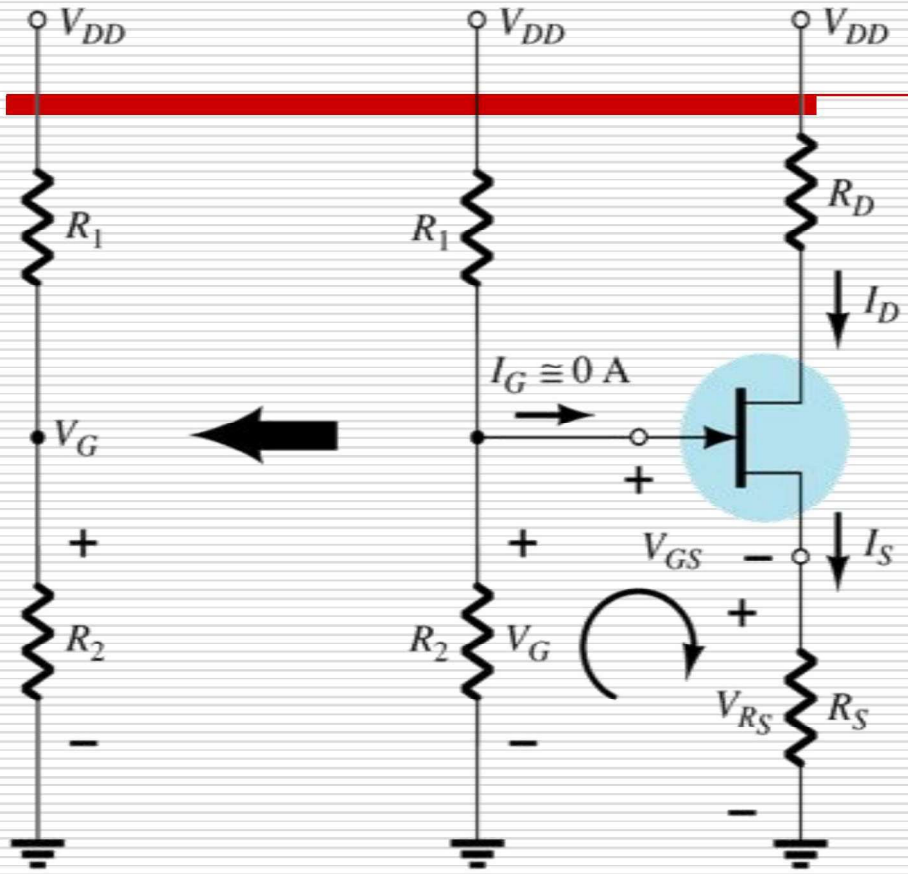
$$V_G = V_{GS} + V_s = 0V$$

$$V_D = V_{DS} + V_s \text{ or } V_D = V_{DD} - I_D R_D$$
$$= V_{DS} + V_s = 8.82V + 2.6V = 11.42V$$

Voltage-divider bias



Redrawn network



$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

Sketching the network equation for the voltage-divider configuration.

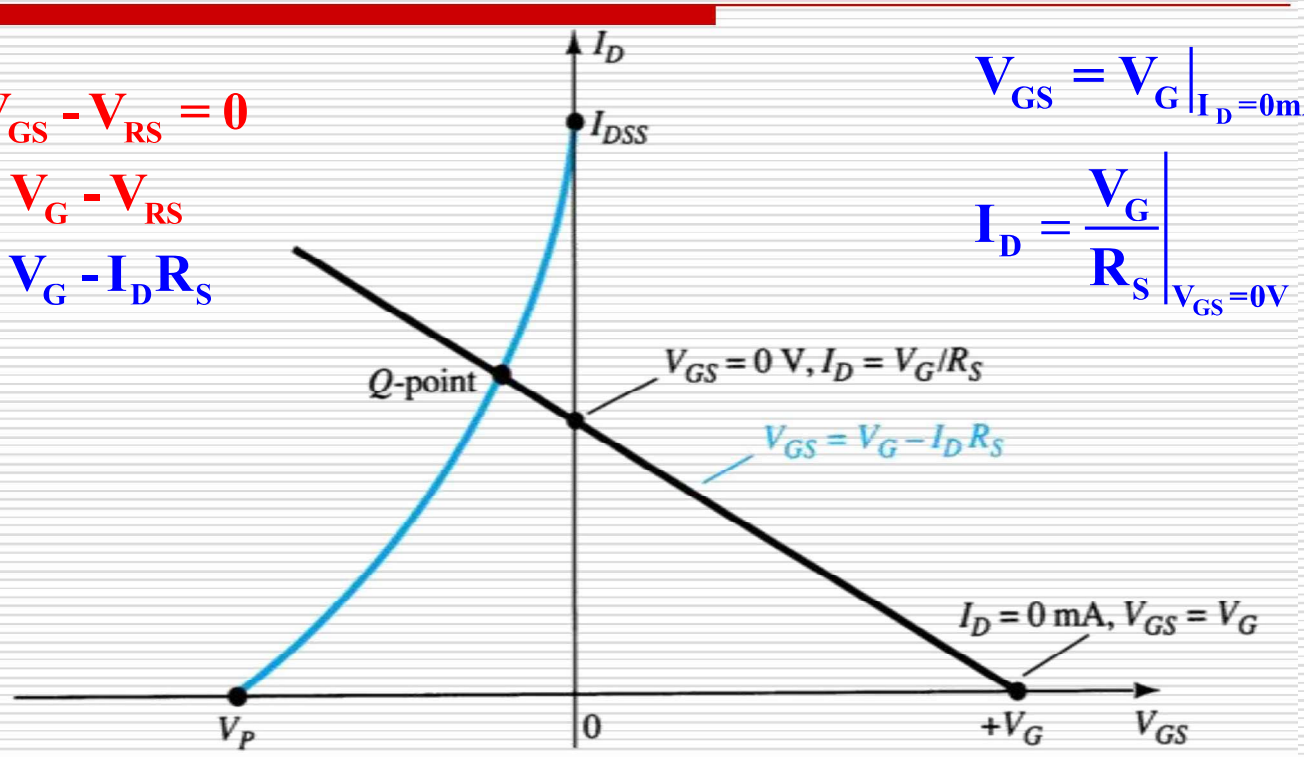
$$V_G - V_{GS} - V_{RS} = 0$$

$$V_{GS} = V_G - V_{RS}$$

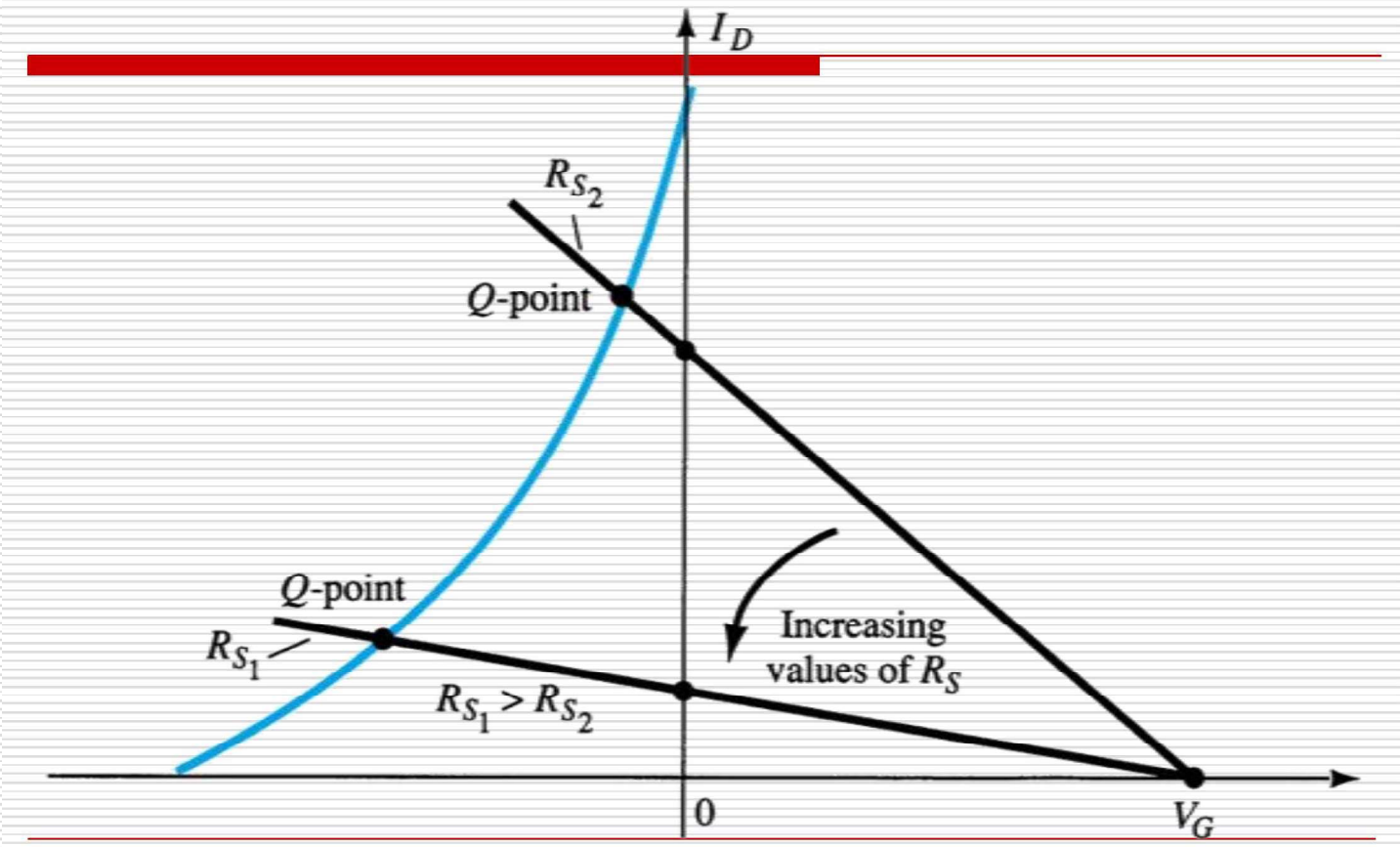
$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = V_G\big|_{I_D = 0\text{mA}}$$

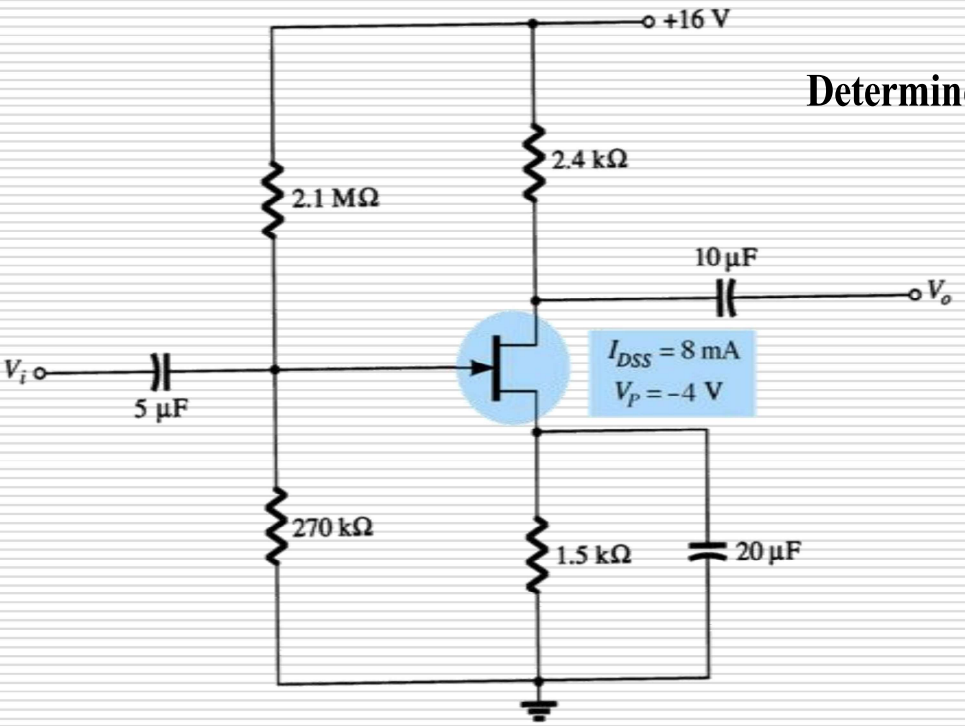
$$I_D = \frac{V_G}{R_S}\bigg|_{V_{GS} = 0\text{V}}$$



Effect of R_S on the resulting Q-point.



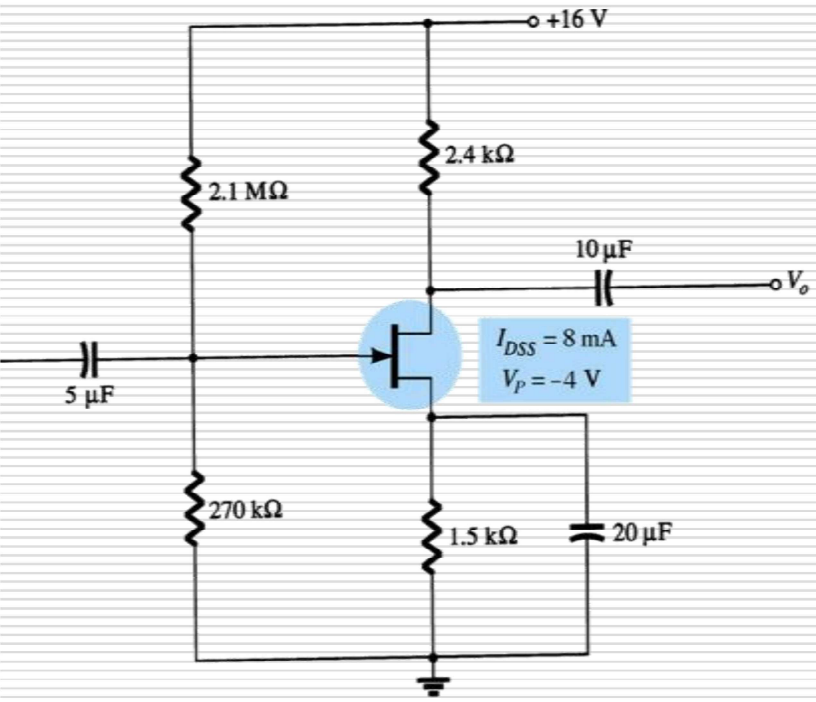
Example : Voltage-divider bias



Determine the following for the network

1. I_{DQ} and V_{GSQ}
2. V_D
3. V_S
4. V_{DS}
5. V_{DG}

Solutions



$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$= \frac{(270k\Omega)(16V)}{2.1M\Omega + 0.27M\Omega_2} V_{DD}$$

$$= 1.82V$$

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82V - I_D (1.5k\Omega)$$

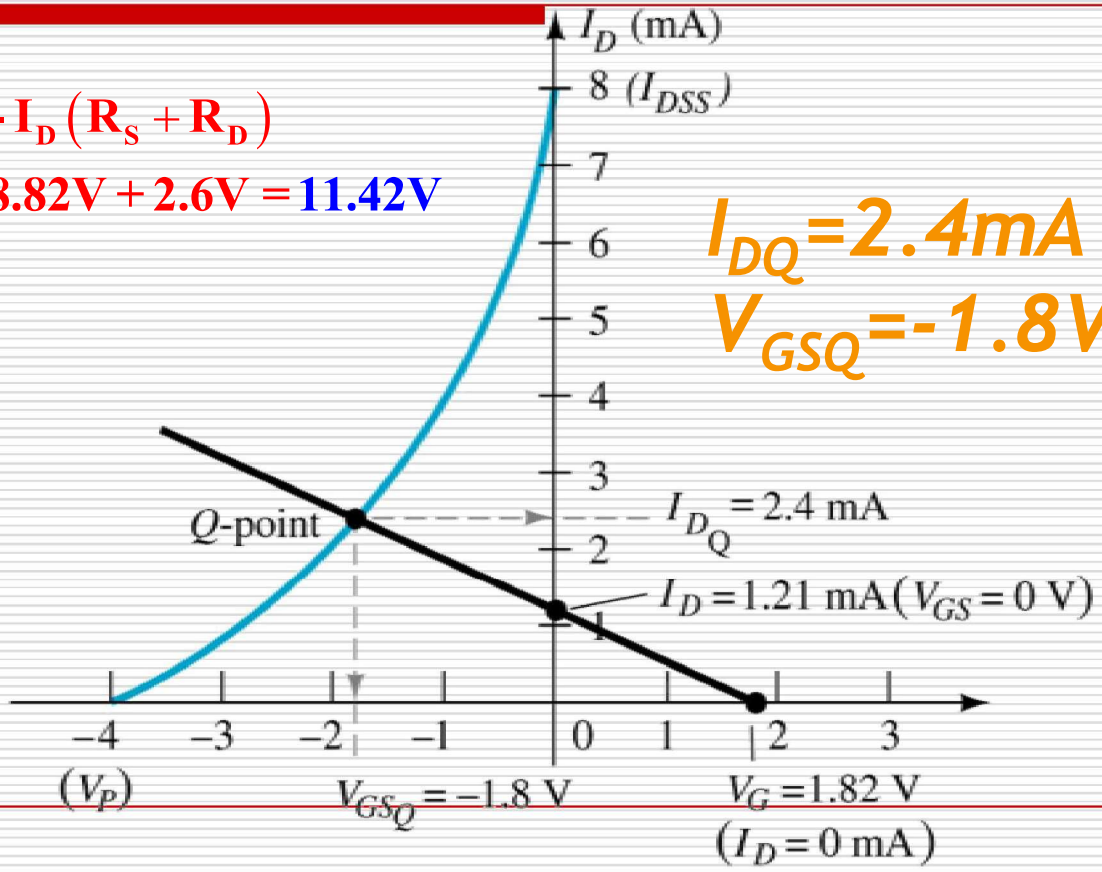
When $I_D = 0mA$, $V_{GS} = +1.82V$

When $V_{GS} = 0V$, $I_D = \frac{+1.82V}{1.5k\Omega} = 1.21mA$

Determining the *Q*-point for the network

$$V_{GS} = 1.82V - I_D(1.5k\Omega)$$

$$V_{DS} = V_{DD} + V_{SS} - I_D(R_S + R_D)$$
$$= V_{DS} + V_S = 8.82V + 2.6V = 11.42V$$

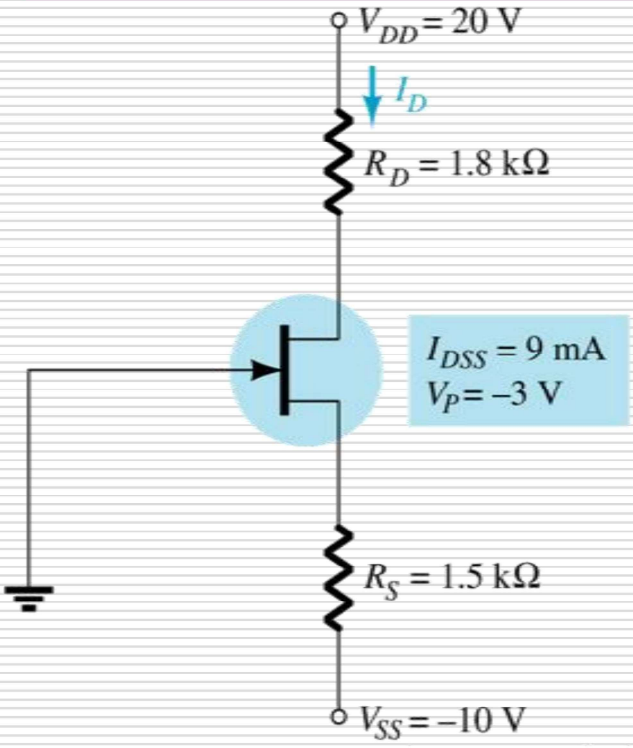


I_{DQ}=2.4mA
V_{GSQ}=-1.8V

Mathematical solutions

- How to get I_{DS}, V_{GS} and V_{DS} for voltage-divider bias configuration by using mathematical solutions?

Exercise 3:



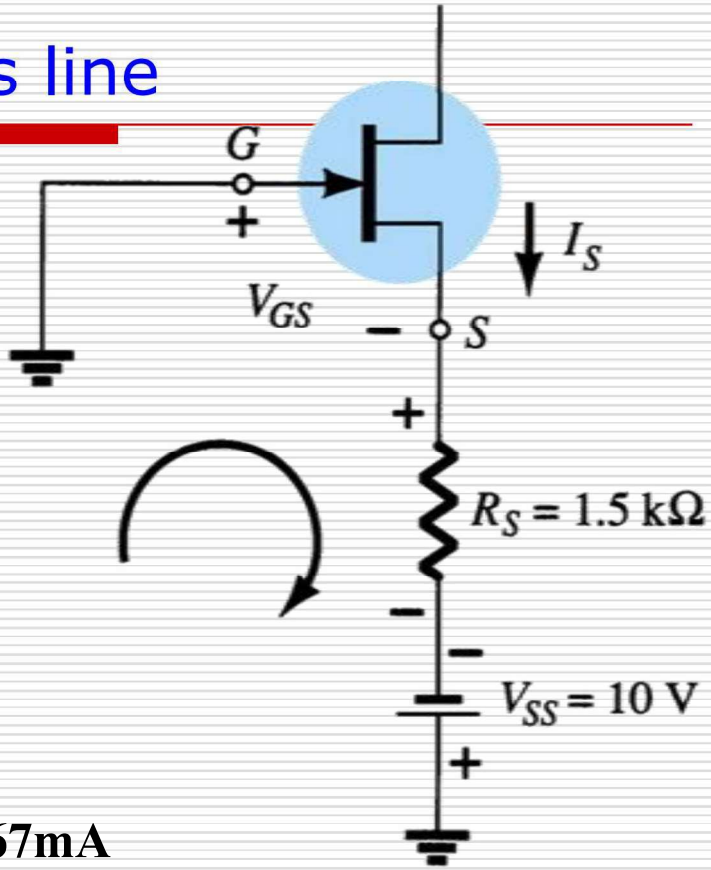
Determine the following for the network

1. I_{DQ} and V_{GSQ}
2. V_{DS}
3. V_D
4. V_S

Drawing the self bias line

$$V_{GS} + I_D R_S - 10V = 0$$

$$V_{GS} = 10V - I_D\left(1.5k\Omega\right)$$



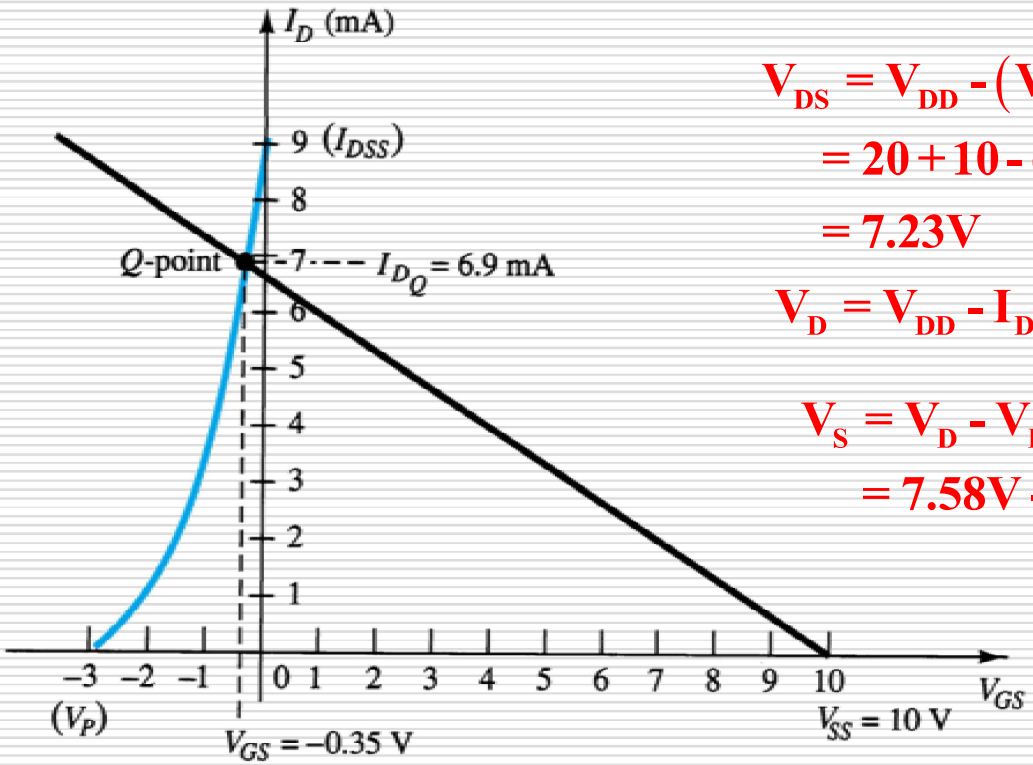
When $I_D = 0mA,\ V_{GS} = 10V$

When $V_{GS} = 0V,\ I_D = \dfrac{10V}{1.5k\Omega} = 6.67mA$

Determining the *Q*-point

$I_{DQ}=6.9mA$

$V_{GSQ}=-0.35V$

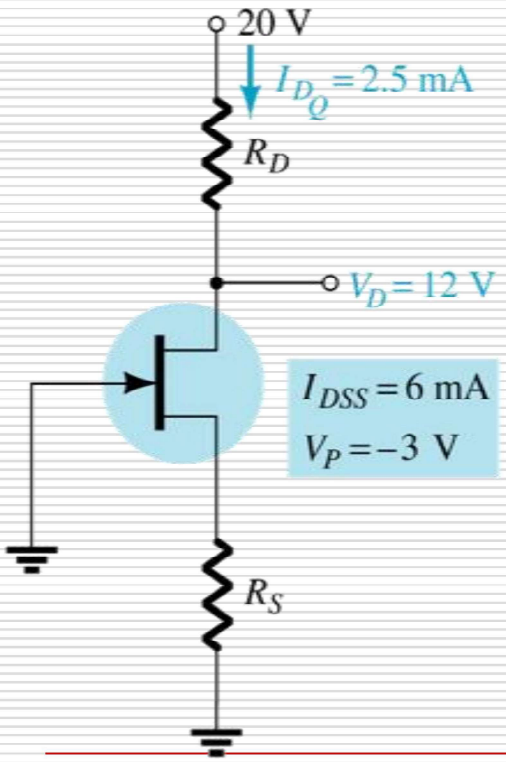


$$V_{DS} = V_{DD} - (V_{SS}) - I_D(R_S + R_D)$$
$$= 20 + 10 - (6.9mA)(1.8k\Omega + 1.5k\Omega)$$
$$= 7.23V$$

$$V_D = V_{DD} - I_D(R_D) = 7.58V$$

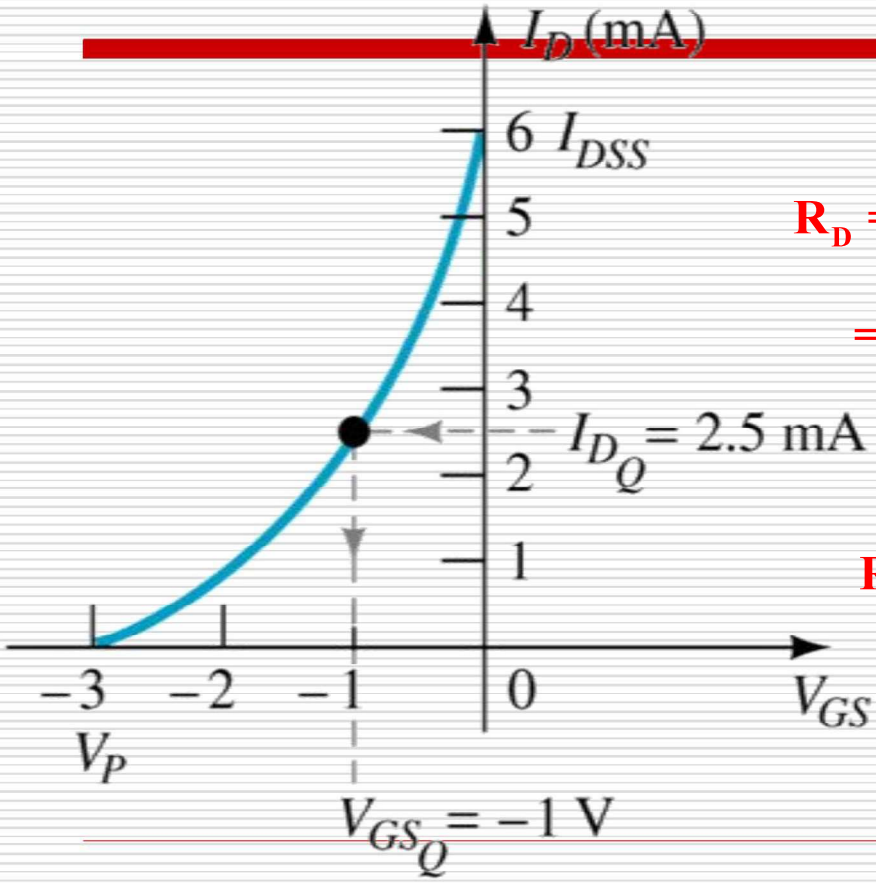
$$V_S = V_D - V_{DS}$$
$$= 7.58V - 7.23V = 0.35V$$

Exercise 4



Determine the required values of R_D and R_S

Determining V_{GS_Q} for the network.



$$R_D = \frac{V_{RD}}{I_{DQ}} = \frac{V_{DD} - V_{DQ}}{I_{DQ}} = \frac{20V - 12V}{2.5mA}$$

$$= 3.2k\Omega$$

$$R_S = \frac{-(V_{GSQ})}{I_{DQ}} = \frac{-(-1)}{2.5mA} = 0.4k\Omega$$

CONTENT COVERED BEYOND SYLLABUS

Fin-FET Technology

Introduction:

The first FinFET transistor type was called a "Depleted Lean-channel Transistor" or "DELTA" transistor, which was first fabricated in Japan by Hitachi Central Research Laboratory's Digh Hisamoto, Toru Kaga, Yoshifumi Kawamoto and Eiji Takeda in 1989.

In 1999, Chenming Hu crammed a record number of transistors onto a chip with his invention of "FinFET," short for Fin Field Effect Transistor. The FinFET – named for a vertical fin-like component (a flat thin part that sticks out of the FET strcuture)– takes up less surface area than conventional two-dimensional transistors, allowing engineers to fit more on each chip.

For decades, the IC industry has incorporated the traditional planar transistor in chip designs, but this technology is running out of gas at the 20nm logic node. This is due to short-channel effects and other factors. So to circumvent these issues, the industry is moving towards finFET transistors. Intel moved into production with finFETs at the 22nm node in 2011. The foundries ramped up finFETs at 16nm/14nm.

Definition:

A FinFET is a type of field-effect transistor (FET) that has a thin vertical fin instead of being completely planar. The gate is fully "wrapped" around the channel on three sides formed between the source and the drain.

Construction:

In finFETs, the traditional 2D planar gate is replaced with a silicon fin that rises up vertically from the silicon substrate. The control of current is accomplished by implementing a gate on each of the three sides of the fin–two on each side and one across the top. FinFET transistors, in turn, form conducting channels on three sides of a fin structure, providing a fully depleted operation. This enables chips to operate at lower voltage at lower leakage.

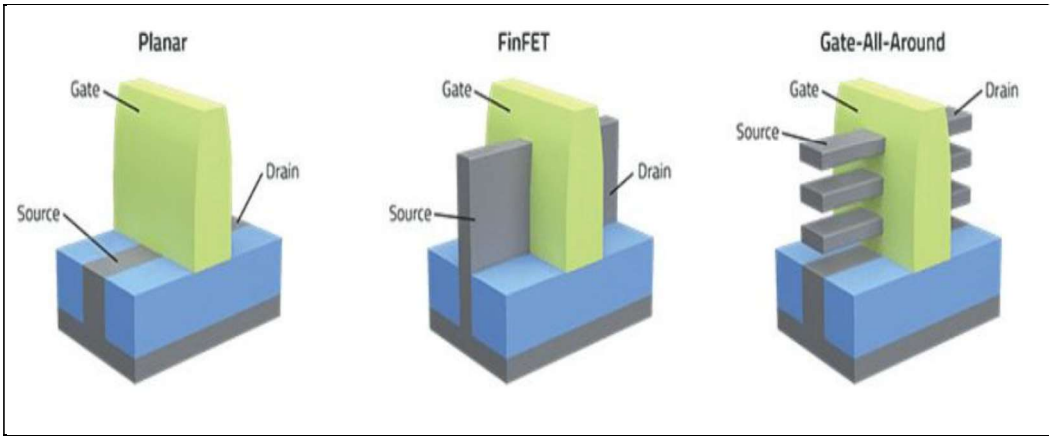


Fig. 1: Planar transistors vs. fin-FETs vs. gate-all-around

Generally, a finFET could have two to four fins in the same structure. The spacing between the individual fins is the fin pitch. Chipmakers hope to scale the fin pitch by 0.7X at each node. The lithography process determines the fin pitch.

Meanwhile, each fin has a distinct width, height and shape. The fins are developed using deposition, etch and other steps. And, of course, the gate also has various characteristics, namely the gate length.

In one finFET production flow, the substrate initially goes through various lithography steps, namely spacer-based patterning. In this process, spacer-like structures are patterned on the substrate. Then, between these structures, an etcher carves out vertical trenches down into the substrate, thereby forming fins. After that, the spaces are filled with oxide using a deposition process. The top portion is polished and then the device undergoes a recess etch step. Finally, a gate oxide is deposited, followed by the formation of the gate.

The greater surface area created between the gate and channel provides better control of the electric state and reduces leakage compared to planar FETs. Using FinFETs, results in much better electrostatic control of the channel and thus better electrical characteristics than planar FETs. FinFETs are the basis for modern nanoelectronic semiconductor device fabrication. Microchips utilizing FinFETs became commercialized in the first half of the 2010s, and became the dominant gate design at 14 nm, 10 nm and 7 nm process nodes. It is common for a single FinFET transistor to contain several fins, arranged side by side and all covered by the same gate, that act electrically as one, to increase drive strength and performance.

Working Principle:

The working principle of a FinFet is similar to that of a conventional MOSFET. The MOSFET can function in two modes: enhancement mode and deflection mode for both p-channel and n-channel MOSFETs. The channel shows maximum conductance when there is no voltage on the gate terminal.

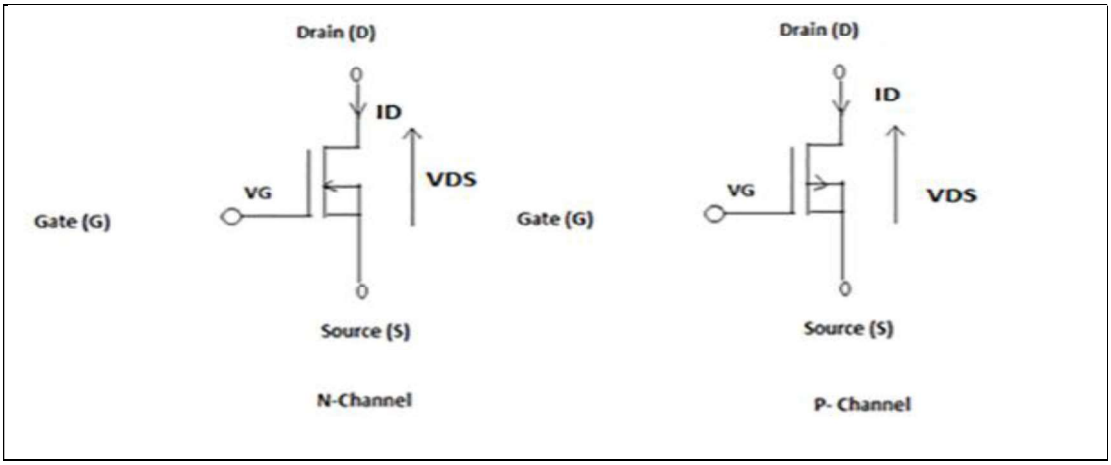


Fig.2: Working principle of FinFET

FinFET transistors, in turn, form conducting channels on three sides of a fin structure, providing a fully depleted operation. This enables chips to operate at lower voltage at lower leakage. Generally, a finFET could have two to four fins in the same structure. The spacing between the individual fins is the fin pitch.

Advantages of FinFET technology:

FinFET technology provides numerous advantages over bulk CMOS, such as:

- higher drive current for a given transistor footprint, hence higher speed,
- lower leakage, hence lower power consumption,
- no random dopant fluctuation, hence better mobility and scaling of the transistor beyond 28nm.

However, these advantages come with certain **drawbacks**, primarily related to the complexity and cost of their fabrication.

Applications:

Today, modern microprocessors, GPUs, and other high-density processors use FinFET technology as the fundamental transistor architecture. In this structure, the gate electrode can be made from polysilicon or a metal alloy, and there is a thin insulator between the channel region and the gate electrode.

The industry sees the gate-all-around FET (GAA FET) is the transistor that will succeed the finFET. The GAA and finFET are considered 3D transistors.

Advantages of FinFET over MOSFET:

FinFET structure is composed of vertical thin fin of silicon body. The gate wraps around the channel from three sides of it, thus it can control the channel in a much more effective position. One of the determining advantages FinFETs have over MOSFETs is the control of Drain Induced Barrier Lowering (DIBL).

Challenges:

Advanced geometry nodes such as FinFET pose significant design and manufacturing challenges that impact some implementation tools. In particular, complex multi-patterning lithography requirements involve:

- In-design physical verification throughout the flow to reduce time-consuming, uncertain iterations.
- Accurate higher levels of extraction and timing analysis to allow for manufacturing variability.

Rajeev Gandhi Memorial College of Engineering & Technology

Autonomous

NANDYAL-518501

Department of Electronics & Communication Engineering

Academic Year: 2022 - 23

Subject: Electronic Devices and Circuits (EDC)

Class: II B.Tech. I-Sem

Faculty member taught earlier: Dr. A. Sathish, Dr. M. Chennakesavulu.

Suggestions:

As per the course structure of the UG (R20), EDC subject is completely based on the study of physical characteristics of semiconductor devices such as diodes, bipolar junction transistors (BJTs), junction field effect transistors (JFET), metal-oxide field effect transistor (MOSFET) and their basic applications in electronic circuits. So, this subject covers theory along with derivations and numerical problem solving. Hence, following suggestions are made by subject experts:

1. As the subject comprises of theory and quantitative analysis derivations, earlier overall pass percentage was 85%. So, it is decided to solve more numerical problems to improve overall percentage further.
2. To improve the subject knowledge of students, more number of experiments in the laboratory is increased with design emphasis.
3. To improve the results, it is decide to take care of slow learners by taking extra classes and make them to practice more numerical problems from previous year question papers as assignments.
4. Regular counseling and motivation should be given to the students to avoid the lacking in the subject knowledge.
5. In addition to conventional teaching methodologies usage for the students, it is suggested that ICT tools in the class rooms are to be utilized for elaborated illustrations of the subject topics in terms of PPTs, animations, and video lectures.

Signature of the subject expert-1

Dr. A. Sathish, Ph.D

Professor, Dept. of ECE.

Signature of the subject expert-2

Dr. M. Chennakesavulu, Ph.D

Assoc. Professor, Dept. of ECE.

Assessment

Rajeev Gandhi Memorial College of Engineering & Technology

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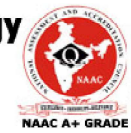
Address : Nerawada 'X' Roads,Nandyal,Kurnool Dist,Andhra Pradesh,India

Counselling Code : RGIT



M.A Vijay Kamalnath
Asst. Prof.
Dept. of ECE
Phone: 9052965365
Email: kamalmav@gmail.com

S.No.	Year (Batch)	Section	Subject	Branch	Registered	Appeared	Failed	Pass(%)	Highest
1	III B.Tech. II Sem. & 2020	B	DC Lab	ECE	65	63	0	100.00	10
2	III B.Tech. II Sem. & 2020	C	DC	ECE	60	60	10	83.33	8
3	III B.Tech. II Sem. & 2020	B	DC	ECE	65	64	3	95.31	8
4	II B.Tech. I Sem. & 2021	B	EDC Lab	ECE	74	73	4	94.52	10
5	II B.Tech. I Sem. & 2021	B	EDC	ECE	74	73	15	79.45	10

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